Analog Integrated Circuit Design
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Lecture - 34
Telescopic Cascode Opamp; Folded Cascode Opamp

Hello and welcome to lecture number 34 of Analog Integrated Circuit Design, in the precious class we improved upon the simple single stage opamp by using common gate amplifiers, with the differential pair as well as with the current mirror. The resulting topology was what we called the telescopic cascode opamp, and in this lecture we will continue with determining other characteristics of this opamp and go on to other kinds of opamps.

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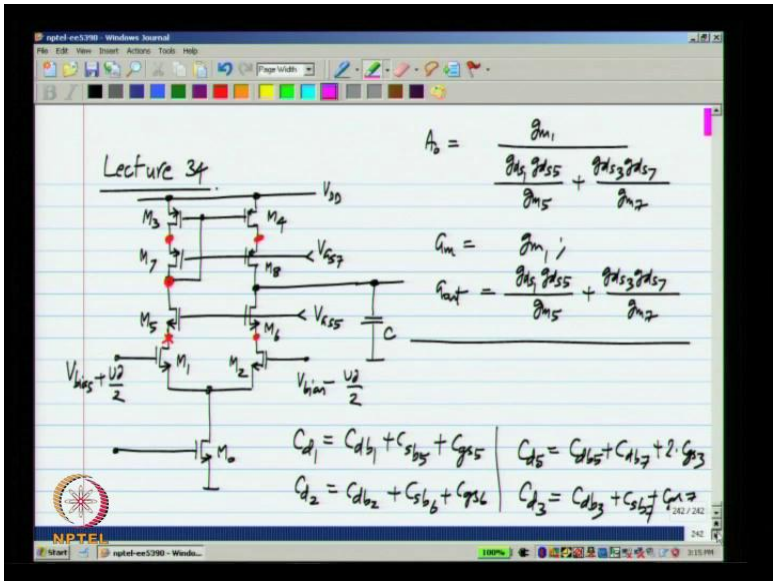

A telescopic cascode opamp consists of differential pair M 1, M 2 bias with the del current M 0 and M 1, M 2 are cascoded by M 5, M 6 which act as common gate amplifiers, their gate is tied to some fixed voltage. And we also use a cascode current mirror M 3, M 4 are the devices of the current mirror, and M 7 and M 8 are the cascode devices, the gate is again tied the some fixed value let me call it v g s 7. Now, we already determined the small signal DC gain, and the small signal high frequency characteristics of this opamp.

The DC gain is G m 1 by the total output conductance, which is this is the conductance contributed by the n most part, the differential pair which is cascoded. And this is the conductance contributed by the p most part the cascode current mirror of course, we know that the simple signal stage opamp is really a trans conductance with a trans conductance value of G m 1 and the output conductance value equal to that whole thing.

So, that is why we get the A naught to be this G m divided by that G out, now as with the single stage opamp when the trans conductance is loaded by the capacitor the poles should be at the origin. But, because of the non 0 output conductance it is shifted slightly into the left half plane, and the dominant pole will be at G out by C. Now, what is of concern for stability are the non dominant poles are 0's, at every node in the opamp there will be a parasitic capacitance.

For instance here, there will be the total capacitance C d 1 which is contributed by C d b 1 plus C s b 5 plus C g s 5. Because, this is tied to a fixed voltage C g s of appears in parallel with the other two capacitors, similarly C d 2 will be C d b 2 plus C s b 6 plus C g s 6 and these 2 will be identical. Because, each of pair transistor is matched M 1, M 2, M 5, M 6, M 7, M 8 and M 3, M 4 and we will also have parasitic capacitances from this node that node and that node. A parasitic capacitance are the drain of M 5 is similar to what we had in the signal stage opamp.

If I call that C d 5 the total equals C d b 5 plus C d b 7 plus 2 times C g s 3 we get the 2 times because, we have C g s 7 3 and C g s of M 4. Finally, we will have C d 3 which is C d b 3 plus C s b 7 plus C g s 7, and similarly we will have the exact same expression for C d 4. Now, associated with each parasitic capacitance will have a pole, and there is a minor feedback loop here around M 3 and M 7. So, that gives you some modifications of the pole values, we will not worry about calculating the exactly values of poles and 0's we will just get an estimate of where those values will be.

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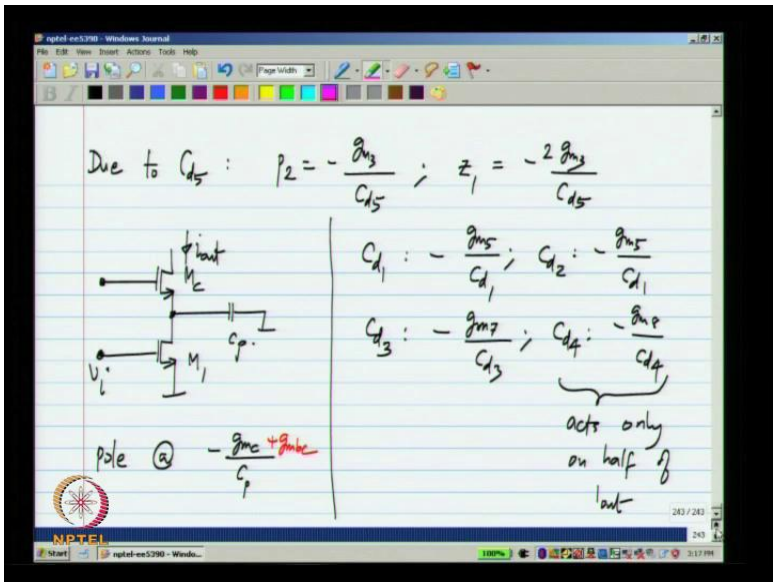

So, first of all the parasitic capacitance here at the drain of the M 5 there will be a pole at G m 3 by C d 5 and a 0 at twice that frequency, exactly same as what we had in the signal stage opamp, the signal stage opamp. And due to other capacitances we know that let us say I have a transistor M 1 cascoded by transistor M c and there is a capacitance here C p the pole associated with this, in the transferred function from V i to the output current, the pole will be at minus g m c by C p if I include the body effect I will also have g m b c.

I will write down the expression excluding body effect for simplicity, but later we can include the body effect, simply by adding g m b and g m values. So, due to those other parasitic capacitors we will have C d 1 will give a parasitic pole at minus g m 5 by C d 1, similarly C d 2 will give you a parasitic pole at minus g m 6 by C d 2 and that is the same as minus g m 5 by C d 1.

Now, this acts on the current that is coming out of M 1 that acts on from the current coming out of M 2. So, there will be a signal pole in the transfer function at minus g m 5 by C d 1, and due to C d 3 we will have a pole at the cascode node minus g m 7 by C d 3 and due to C d 4 minus g m 8 by C d 4 and what this due to the transferred function is more complicated, this acts only on half of the current it is only the current from M 1 which gets mirrored goes through this pole a current from M 2 does not.

Similarly, this the pole at this node acts only on one half of the current, so all of these will end up giving poles as well as 0's due to the mirroring effect, and acting on only one half of the current this is similar to due to C d 5 we have a pole as well as a 0. So, due to these things also we will have pole as well as 0's, for now we will just say that there will be lots of parasitic poles and 0's and roughly the frequency is given by the g m of the cascode transistors divided by the total parasitic capacitance, at the source of the cascode transistor.

So, there will be a number of parasitic poles and 0's and this will be apparent in the simulated frequency response, and the effect of all of these things must be such that, the phase margin is of adequate value say 60 degrees. So, then you have to adjust your unity gain frequency, so that happens or somehow you have to try on move the parasitic poles to higher frequencies.

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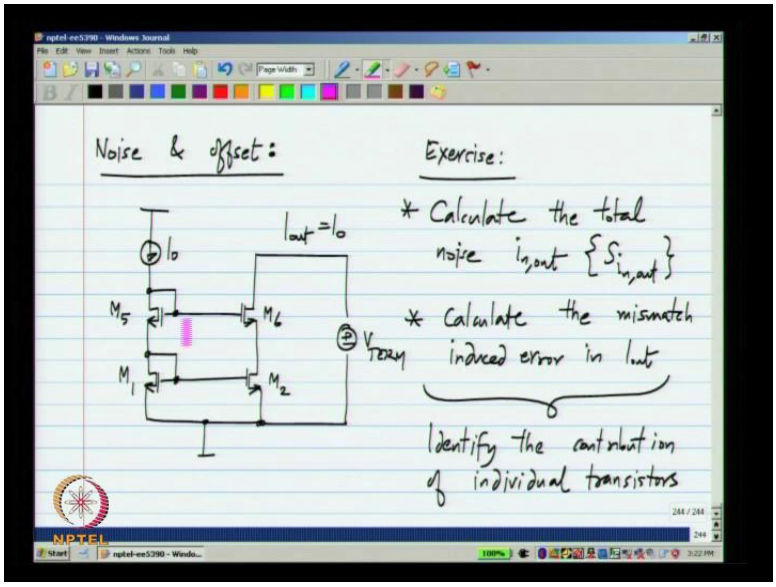

Next we have to evaluate the noise and offset, now we have lot more transistors than before. So, first we have to intuitively understand what happens to the noise and offset in cascode transistors, first let me take just a cascode current mirror I will use a slightly different biasing than what I used in the previous class, just for simplicity. This is not the optimal biasing, but it has only one reference branch and it is quite simple to understand we have V g s across this transistor let me call this M 1, M 2 and perhaps M 5 and M 6 we have V g s across M 5 v f s across m one and those will bias M 6 and M 2.

And if you compare this to the high swing cascode current mirror structure we had, in that case the drain of M 2 was bias at V d sat the minimum required. In this case it will bias at V g s 1 the voltage here and there will be the same, so it is lot more than what is required and wasteful, but our point right now is different to evaluate the offset and noise. So, please take it as an exercise and calculate the total noise in i out, let us say this is i out and nominally this equal to i naught.

And it will have some noise due to the four transistors calculate the total noise, when I say total noise I mean the spectral density of the output noise current. So, for this you have to put down the small signal model of each to the transistor, please include both of g m and g d s and find out what the noise is going to be. And also calculate the mismatch induced error in i out, now M 1 and M 2 should be matched and M 5 and M 6 should be matched.

But, they are not we know that there will be thresher voltage mismatch, and current factor mismatch. So, put down those things in the circuit and find out the mismatch induced error in i out, and in each case identify the contribution of individual transistors that is how much noise comes from the M 1, M 2, M 5 and M 6. Similarly, how much of the mismatch is due to mismatch between M 1 and M 2, how much of mismatch is due to mismatch between M 5 and M 6, so please do all of that.

Now, in this lecture I will work it out as well, but I will use a simplification I will assume that the g d s values are 0. So, whatever expressions you get you take the if you said g d s to be 0 you should get whatever I get in the lecture, also it turns out that the analysis without g d s, analysis with g d s equal to 0 is good dam to build intuition and even quantitatively it is by and large current.

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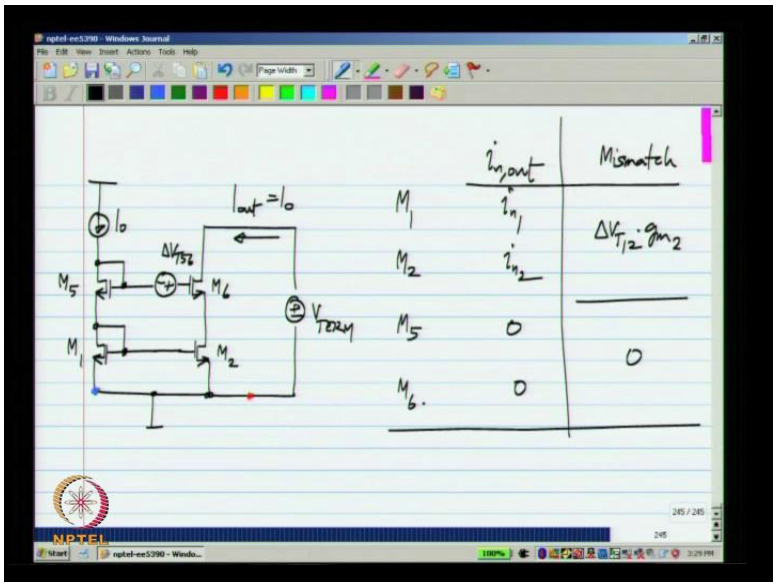

So, first let me take noise due to M 2, now what is it contribution to the output current i out, it is very easy to see that you can think of M 6 as a common gate amplifier to which a signal of i n 2 is applied, so all of i n 2 goes onto i out. So, M 2 as a noise current i n 2 and all of it appears at the output, let me take the noise current of M 1 what happens here, this noise current i n 1 flows into the divert connected transistor, clearly the current in this branch cannot change from it is value i naught.

So, all of i n 1 flows into M 1, so it is get mirrored and gets drawn into M 2 and that also contributes in it is entirety to the output current. Now, the next term the contributions from M 6 and M 5 let me call this i n 6 and remove the noise from these other transistors, what is the effect of i n 6 on the output. It is very obvious here that whatever current is delivered from M 2 must come to the output, i n 6 cannot have any role in what the output current is, the output current will be simply whatever is coming out of M 2.

And I assume that M 2 has 0 g d s, in fact, all transistors has 0 g d s, so even if this voltage changes because, of i n 6 later you will see that when you do your analysis i n 6 will change this voltage, the current here would not have changed. So, the output current due to i n 6 would be 0, now you can also use the alternative method of splitting i n 6 into two parts, and connecting the intermediate node to ground, so that it becomes easier to analyze.

And then you do the analysis find that and you will find that the output current will be 0, then what happens due to M 5, clearly the current in M 1 is still equal to i 0 whatever current goes into this must come here. So, what i n 5 will do is to change the voltage across M 5, and that will not have any effect on the current in M 1. So, since the current in M 1 is the same as before, current in M 2 is same as before, again I assume g d s to be 0, and all of the current in M 2 comes out. So, the contribution of M 5 to the output noise is also 0, so that is about the noise.

So, what we see is that the main current source devices M 1 and M 2 contribute their noise current completely to the output. And the cascode devices M 5 and M 6 do not contribute anything to the output noise, it is as though we have only the simple current mirror using M 1 and M 2. So, that is a very useful result to remember and like I said please do the analysis including g d s, you will see that the numbers here will be modified slightly, but not greatly, but you should be able to understand exactly how much comes out due to noise in each of these transistors.

Now, let us go to mismatch if I have mismatch between M 1 and M 2, what happens M 1 will have some V g s which will correspond to the V g s for current of i naught. Now, the V g s of M 2 is different it is different by this number delta V T 1 2, so the current in M 2 will be different from current in M 1, and how different it will be it will be delta V T 1 2 times the g m of the transistor M 2. Now, similarly if you have a current factor error you can modeled that as a current source in parallel with M 2 and in fact, that analysis will become the same as the noise analysis.

So, you will find that delta V T 1 2 the mismatch between M 1 and M 2 will contribute directly to the output. Similarly, you can calculate the effect of the current factor mismatch between M 1 and M 2 I am not going to do it here, now let us assume that only M 5 and M 6 are mismatched. Now, what happens in this case the current in M 1 is still i 0 I assume 0 g d s and, so on, so the current in M 2 which depends in only it is V g s will also be i 0.

So, the output current will be i 0 what will be delta V T 5 6 do it will make the drain voltage of M 1 different from drain voltage of M 2. But, since I have assumed g d s to be 0 that has no effect on the current in M 2, and the output current is still i 0, so the effect of mismatch between M 5 and M 6 is 0. So, as you see both the noise and mismatch are

contributed by the main current mirror devices, and there is 0 contribution from the noise and mismatch of the cascode devices. So, this simplifies the analysis greatly what matters for the output noise and mismatch is only the noise from the current mirror the main current mirror devices, as well as from the differential pair.

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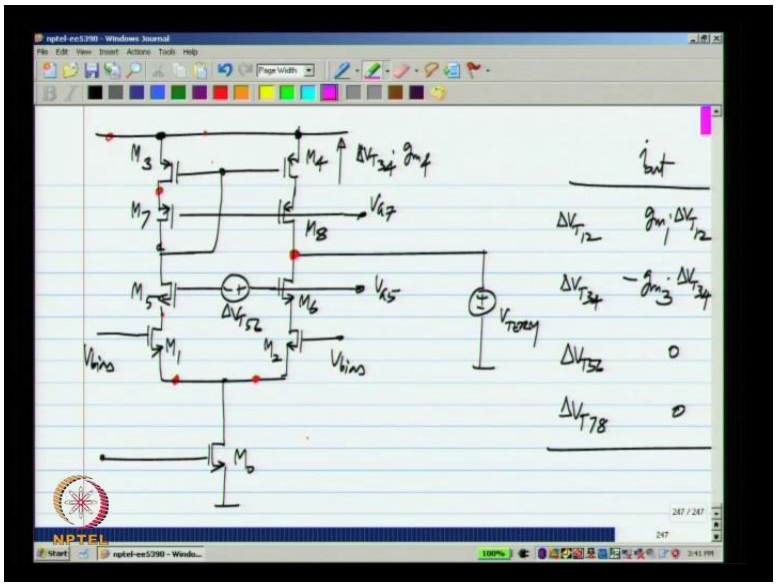

So, from what we analyze, so far just for the simple cascode current mirror can be extended to the entire telescopic cascode opamp. As can be expected from that analysis only the main transistors M 1 and M 2, and transistors M 3 and 4 contribute to the output noise. I would encourage you to put a noise current source in parallel with all these eight transistors, and also the ninth transistor m 0 and then see what comes to the output. Now, if we have a noise current source i n 0 what happens to it, it divides equally between M 1 and M 2.

Because, looking up the source of M 1 we have an incremental resistance of 1 over g m 1 looking up the source of M 2, we also have an incremental resistance of 1 over g m 1. So, it divides equally, so we will have i n 0 by 2 and i n 0 by 2, now the part that goes into M 3 and M 7 will get mirror and we will have i n 0 by 2 over there. Now, this and this will cancel and at the output we will have 0 contribution, this is exactly the case that we had for the simple differential pair opamp without the cascoding as well.

So, in general anything that you inject into the tail node, here we split equally and we will have 0 contribution to the output. If you take the noise M 1 again there are different

ways of doing it, you can split it into two parts I split it into two identical current sources i n 1 and i n 1. And now we can superpose here we have to superpose the currents not just the spectral density, it is clear that i n 1 the lower one is being injected into the tail node and it is contribution to the output is 0.

And this other i n 1 will go through M 5 which is a common gate amplifier through the current mirror and contributes i n 1 to the output. So, that is what happens to the noise from M 1, and in a exactly similar way you can work out that the noise from M 2 also appears completely at the output. If I have a noise current i n 2 that will be drawn out here, so a polarity here should be minus i n 2, but it does not matter because, the noise of each transistor is uncorrelated from noise of other transistors.

Now, let us consider what happens to M 3 a noise from M 3, now what happens to this particular noise, what it does is you can analyze this exactly what happens here it is a little in molt. But, you will that i n 3 will flow into M 3, and the voltage here the gates source voltage of M 3 will be change, so the gates source voltage of M 3 would be i n 3 divided by g m 3, and that causes a current i n 3 in the drain of M 4 because, the g m of M 4 is the same as g m of M 3, and this goes through M 8 and goes to the output.

So, the contribution of M 3 again is full and it is i n 3, and the contribution of M 4 which is quite simple to calculate lie on 4 and that is simply goes through M 8, which is a common gate amplifier and is drawn from the output voltage source V term, so this will be minus i n 4. Now, these M 5, M 6, M 7 and M 8 you can work out in a similar way, so as I said you could split it into two parts, and connect the intermediate node to ground or used a previous result that we had that cascode devices, do not contribute noise to the output.

I would strongly encourage you to work it out individually each of these 4 cases, and then convinced yourselves that that is indeed the case. So, the contributions from these 4 transistors will be 0, so the resulting noise is exactly the same as what we would find in a simple differential pair opamp without cascodes. There also we had M 1, M 2, M 3, M 4 and all 4 will be contributing to the output noise, here we have 4 extra transistors, but they contribute nothing to the output noise.

Now, let us take mismatch between each pair of identical transistors M 1 2, M 5 6, 7 8 and 3 4 there will be mismatch. And for simplicity I will assume only thrasher voltage

mismatch, although there will be current factor mismatch as well, if you have delta V T 1 2 that is mismatch between M 1 and M 2. Let me reduce the input to 0, if I have mismatch between these as usual it is easy to modulate as a change in V g s instead of change in V T.

So, it is like applying a voltage delta V T 1 2 to the input, and if the input is delta V T 1 2 the output will; obviously, be g m 1 delta V T 1 2. Now, if you consider the mismatch between M 3 and M 4 this is delta V T 3 4, now in absence of any other mismatch, the current in each of these arms will be i naught by 2 if there is no mismatch at all. Now, if you have a mismatch the V g s of M 3 will be different from the V g s of M 4, and the difference is given by delta V T 3 4 it is exactly like applying incremental voltage delta V T 3 4 to the case that we had before.

So, the incremental current here will be delta V T 3 4 times g m 4 and all of that is drawn from the output. So, delta V T 3 4 causes in output current minus g m 4 which is the same as g m 3 delta V T 3 4, so these results are exactly identical to what we had earlier, we had delta V T 1 2 contributing delta V T 1 2 times g m 1, and delta V T 3 4 contributing minus g m 3 times delta V T 3 4. Now, what about the mismatch between M 5 and M 6 our analysis of the cascode current mirror says that it should not have any effect, and that is indeed the case.

I will take the simpler case of a g d s being 0, now what this delta V T 5 6 will do is to change the drain voltages of M 1 and M 2 from the gate of M 6 to the source of M 6 it acts like a source follower, but the gate of M 6 and M 5 are now at different voltages. So, the sources of M 5 and M 6 will also be at different voltages this changes the V d s of M 1 and M 2, but if g d s is 0 it means that the current in M 1 and M 2 do not response to V d s and the currents will be exactly the same as before, and exactly the same argument also holds for M 7 and M 8. So, delta V T 5 6 and delta V T 7 8 have 0 contributions to the output, again exactly behavior as noise. So, the analysis while the circuit has many transistors is actually really simple it, in fact, the results are exactly same as what we got a simpler case without the cascode transistors.

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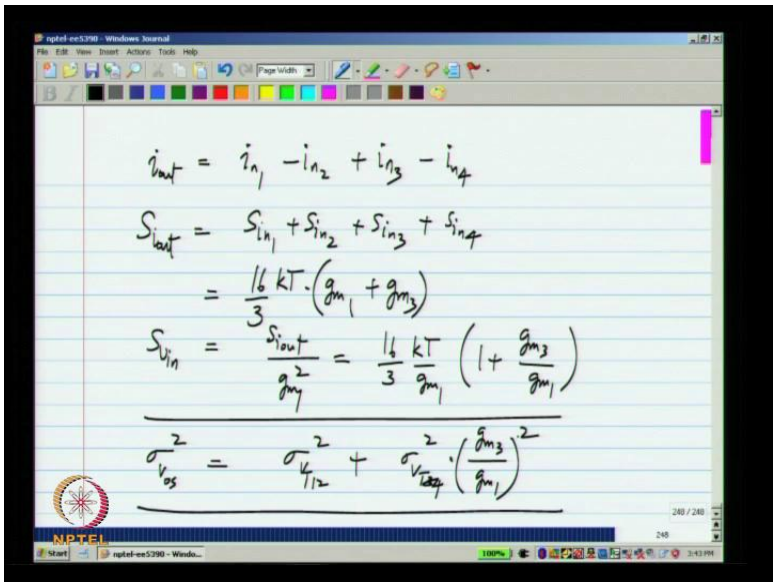

Since i out is i n 1 minus i n 2 plus i n 3 minus i n 4, S i out is simply the sum of the spectral density S i n 1 plus S i n 2 plus S i n 3 plus S i n 4, which gives you 16 by 3 k T times g m 1 we get 16 by 3 because, we have two transistors with a trans conductance of g m 1 and 2 transistors 3 and 4 with a trans conductance of g m 3. And as usual we calculate the input referred noise, by dividing the output noise spectral density by g m 1 square it is a trans conductance of this particular stage times g m 1 plus g m 3.

And as we had expressed it sorry which is equal to 16 by 3 k T by g m 1 1 plus g m 3 by g m 1. And similarly, the mismatch when referred to the input you can calculate this yourself will be the mismatch of the first stage, the variance of that plus the mismatch of the load stage times g m 3 by g m 1 square, you will recall that this is exactly the result we had for the simple differential pair opamp.

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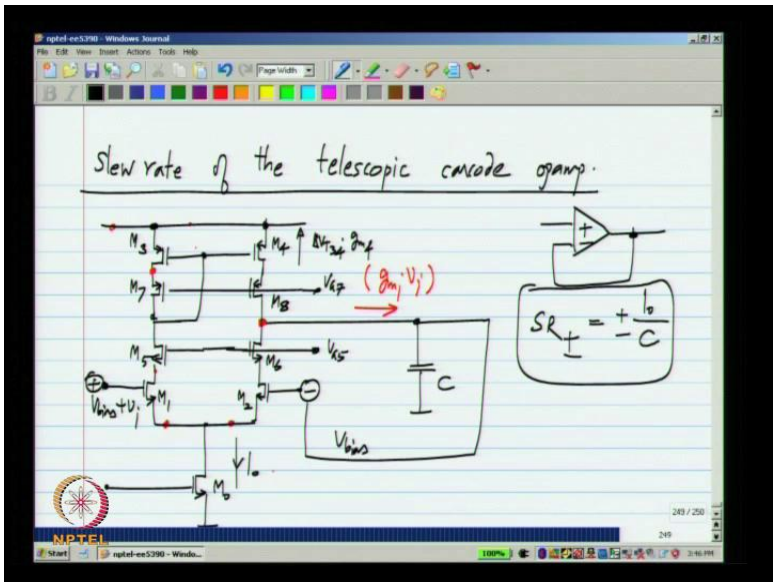

Now, there are other things that we need to calculate the one of the things is slew rate, so to measure this slew rate we make the opamp that is below the trans conductance with the capacitor. And let me assume a unity feedback configuration as I did earlier, we know that this is the plus terminal to each I will apply V bias plus V i and the minus terminal is used to complete the feedback loop. If the input is V bias and we allow the circuit to reach the steady state, this voltage will also be at V bias.

And if we apply an input step what happens is, this voltage does not change suddenly because, of this capacitor. But, because there is a step they across the differential pair we have an input of V i, which generates the differential current of g m 1 times V i flowing into the capacitor. Now, as we increase the magnitude of V i what happens is that this magnitude goes on increasing, but as with the differential pair we know that it cannot never be more than, the tail current of i naught.

There will be a value of V i for which all of i naught will flow through M 1 and nothing will flow through M 2. And it flows through this current mirror M 3, M 7, M 4, M 8 and we will get pose thing to the capacitor, now any V i larger than that will not resulting in the larger current, the current will be still be i naught. So, the maximum rate of change in the positive direction is i naught divided by C and it is very easy to work out that if V i is large in negative all of this i naught flows through M 2 and M 6 and we will be drawn from the capacitor.

So, the negative slew rate will be simply minus i naught by C, so this result is also exactly identical to what we had with the simple differential pair opamp. Now, the last thing that we have to calculate a large signal quantity is the signal swing, we know that the opamp has 2 swing limits, one at the input which imposes limit on the input bias voltage or the common mode voltage and one at the output which imposes limit on the output swing.

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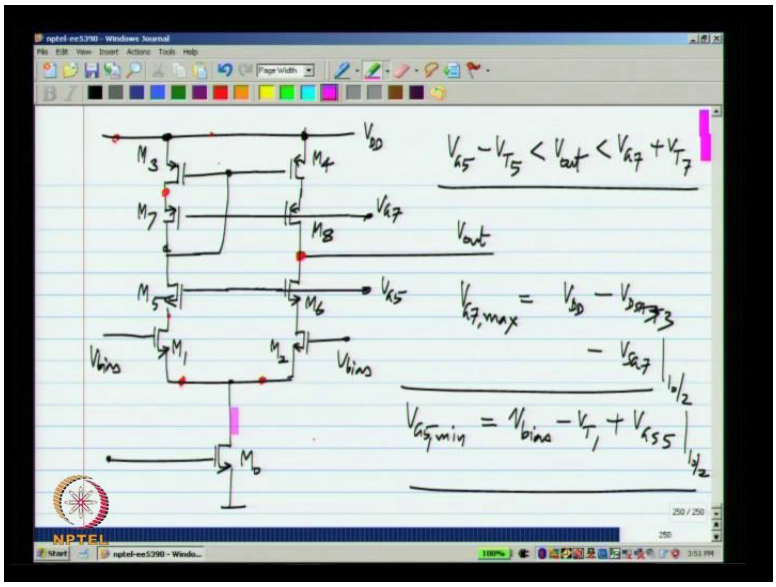

Now, first let us consider what can happen to the transistors, if the output becomes too large too small. The output becomes very large, then the drain voltage of M 8 will go above the gate voltage of M 8, now it can do that, but not by more than 1 V t, so the maximum of V out is simply V g 7 plus V T 8 which is also V T 7. And as V out reduces it can go below V g 5, but not more than one thrasher voltage, if it does that M 6 will go into triode region. So, the minimum value of V out can be very simply written as V g 5 minus V T 5.

Now, you have to adjust the value of V g 7 and V g 5, so that we get the maximum swing limit that is possible. Now, V g 7 should be maximize, so that the upper limit as large as possible, but what happens is if V g 7 is increased beyond the certain value, the source of M 8 and M 7 will increase beyond the certain value that will push M 3 and M 4 into triode regions. What is the maximum value of V g 7, it is where this transistor M 4 and

transistor M 3 are on the verge of saturation, just about going into triode region and you need a V g s across M 8.

So, the maximum value of V g 7 is given by v D D the supply voltage minus V D sat 3 which is the limit for these transistors going into triode region minus V s g 7 which is also V s g 8 at the current of i naught by 2. This is the maximum value, and we can sated to be equal to this maximum value using the i swing cascode biasing technique that we discussed in the previous lecture. In fact, you see that what we have there is a current mirror, and we can maximize the compliance of the current mirror by using the i swing biasing technique for the cascode.

Now, what about V g 5 we would like to minimize V g 5, so that lower limit is as low as possible, if we go on lowering the V g 5 what happens is the source of M 5 and M 6 will go on decreasing, and M 1 and M 2 can be pushed into the triode region. So, what is the minimum value of V g 5 it is the minimum value of the source on M 5 and M 6 plus the V g s of M 5 and M 6. Now, what is the minimum value of the source of M 5 and M 6 that is equal to v bias minus V T, the drain of M 1 can go below the gate, but not by more than 1 V T.

So, V g 5 the minimum value of it is V bias minus V T 1 plus V g s 5 at the current of i naught by 2. So, there are many variables here these bias voltages, but the output a swing limit is dependent on the bias voltages V g 7 and V g 5 to optimize that we should maximize V g 7 and minimize V g 5. The maximum value of V g 7 is dependent on these transistor parameters, and minimum value of V g 5 depends on these transistors as well as the value chosen for V bias. So, just that we did in the last lecture we can maximize the swing limit by adjusting the bias voltages appropriately. Now, we also need to compute the limit on V bias itself, now as usual as in the previous case V bias when it becomes very small, the tail node will follow V bias and eventually it will push M 0 into the triode region.

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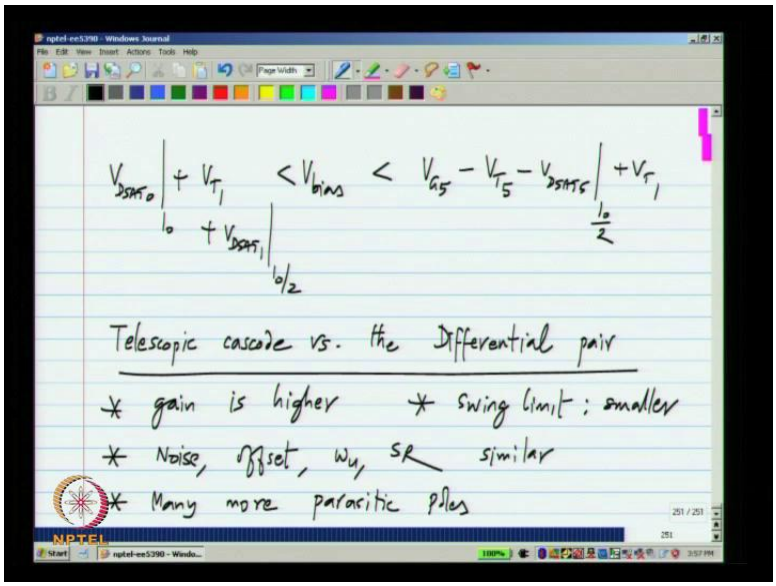

So, V bias has to be greater than the saturation voltage of M 0 at the current of i 0 plus V g s of M 1 or M 2 which is V T 1 plus V d sat 1 at the current of i naught by 2, what happens if V bias goes on increasing, the current in M 1 and M 2 are i naught by 2. So, V g s of M 5 and M 6 are fixed to some values, so the drain voltages of M 1 and M 2 are V g 5 minus V g s 5. The gate of M 1 can go above the drain of M 1, but not by more than one thrasher voltage.

So, the upper limit will be V g 5 minus V g s 5 plus V T 1 and V g s 5 itself can be written as minus V T 5 minus V D sat 5 at the current of i naught by 2 plus V T 1, the thrasher voltages are equal that part will cancel and we will have V g 5 minus V D sat 5. So, you will have to arrange all these bias voltages, in fact, when you start designing circuit you will see that, from the basic schematic there will be a lot of addition for providing all these bias voltages.

So, that said about the telescopic cascode amplifier it performances by and large the same as the single stage amplifier with the differential pair loaded by current mirror. The predominant difference is in the DC gain, mainly this happens because, we are increasing the output resistance nothing else has changed that trans conductance is same as in the differential pair. The output resistance can be an order of magnitude higher or even a little more, so the DC gain go this opamp is of the order of g m by g d s square.

Now, the other things like noise and offset remain the same, the parasitic poles will be different in that as far as the frequency response is concern, it still behaves like an integrator, but there will be lot more parasitic poles. Simply because, we have lot more nodes in the circuit, and all these parasitic poles are non dominant poles of the order of g m divided by the source of parasitic capacitance of these cascode transistors. And they will create some complicated poles and 0's, and the phase margin due to all of these things should be greater than the desired value.

Other thing we see is that slew rate is also exactly same as in the simple differential pair case, now one other difference is in the swing limit. We see that, we have two transistors between V D D and the output, previously we had the single transistor M 4, so this output voltage could go within 1 V D sat of V D D. Now, even if we adjust V g 7 to be it is optimum value, we need to have 1 V D sat across M 4 another V D sat across M 8. So, where will be 2 V D sat away from V D D.

Similarly V out could be one thrasher voltage below V bias, but now it can be one thrasher voltage below V g 5. And we know that V g 5 has to be slightly higher than V bias by one gate over voltage or saturation voltage, so both the upper limit and lower limit have changed, upper limit has reduced and the lower limit has increased. So, the swing limit has reduced compare to the simple single stage opamp, the gain is higher this was a purpose with which we made the telescopic cascode.

Noise, offset, unity gain frequency, slew rate are all similar there will be many more parasitic poles. And finally, the swing limit is smaller this is simply a consequence of stacking more transistors between the ground and power supply, a more transistors you stack the less room there will be for the signal to swing, this is a very common limitation, so that is what we had with the telescopic cascode.

Now, the way we came up with the telescopic cascode was to take the current from the differential pair, and put it through a common gate amplifier. So, that the output resistance looks much higher than what is originally was, we choose to use an n mos common gate amplifier with the n mos differential pair. But, there is no need to do this, we could de equally use a p mos common gate amplifier with the n mos differential pair and that gives us a different opamp topology.

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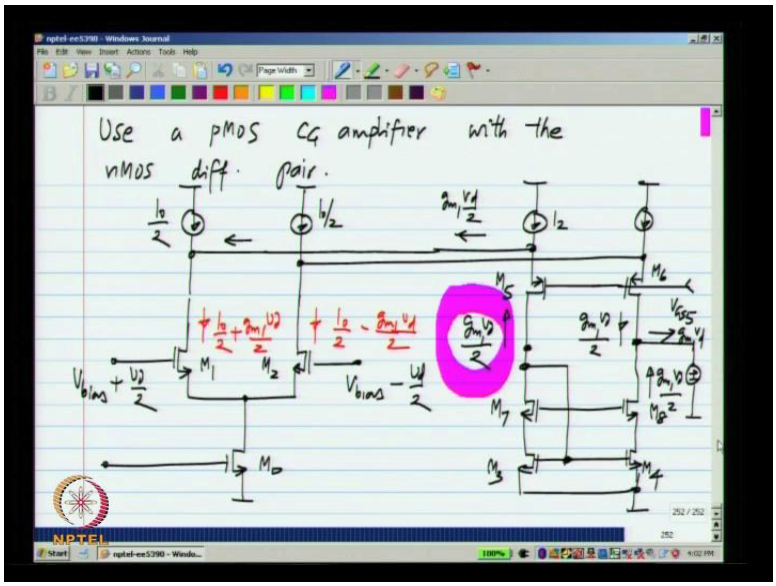

So, that is what we are going to discuss here on let us say we use a p mos common gate amplifier or a p mos current buffer with the n mos differential pair, here is my differential pair same what I have had a long M 0, M 1 and M 2. Now, if I apply a differential voltage of V d the current here will be i naught by 2 plus g m 1 V d by 2 and in this case on in M 2 it will be i naught by 2 minus g m 1 V d by 2. The g m 1 V d by 2 is the signal part of the current.

And that is what has go through the current buffer that is the signal that we want to deliver to the output, if that part goes through the current buffer it will become a much better signal current source of the same value. As I said I want to use a p mos common gate amplifier, I will bias the p mos common gate amplifier with some current source at the source node, let me just call this i 2. And let me call this M 5, now if I inject the current g m 1 V d by 2 the signal current in the drain of M 5 will be the same.

But, looking in here we have a much higher resistance, now to get the signal part of the current what I have to do is to have a current i naught by 2 and, so that the biases subtracted. So, in this wire we will have only g m 1 V d by 2, so that is what I am going to have similarly I can do it for the other output, and I will connected to another common gate amplifier M 6, which is bias at a fixed gate voltage of V g 5. So, looking in here I will have much higher output resistance, due to the common gate amplifiers, but the same incremental currents.

I will have an increment of g m 1 V d by 2 flowing there, and I will have an increment of g m 1 V d by 2 flowing that way. So, what should I do next I should mirror one side of the current to the other side, and I have to use cascode current mirror because, there is no point improving the output resistance of only the differential pair side, without improving the output resistance to the current mirror side. We have to improve both side because, they will contribute equally to the output conductance or output resistance.

So, what happens now, here I have shown only the incremental parts this incremental current g m 1 V d by 2 will get mirrored into M 4 and M 8 in the same direction. The total current of course, will be downwards, but the incremental current here will be g m 1 V d by 2. And if we have a load connected let me assume a voltage source load there will be a current g m 1 V d flowing into that voltage source.

So, what I have now is a trans conductor which is also a cascode type of trans conductor, the only difference from the previous one to this one is that with an n mos differential pair I have used the p mos a cascode device or a p mos a common gate amplifier device. Now, because of this my current mirror has to change from being a p mos type to being an n mos type, but incrementally we can easily see that the operation is the same, the output current will be g m one times V d.

Now, this topology because, the current flows upwards in the n mos and then gets folded down by the p mos is known as the folded cascode opamp, we will analyze this in detail in the next lecture.

Thank you.