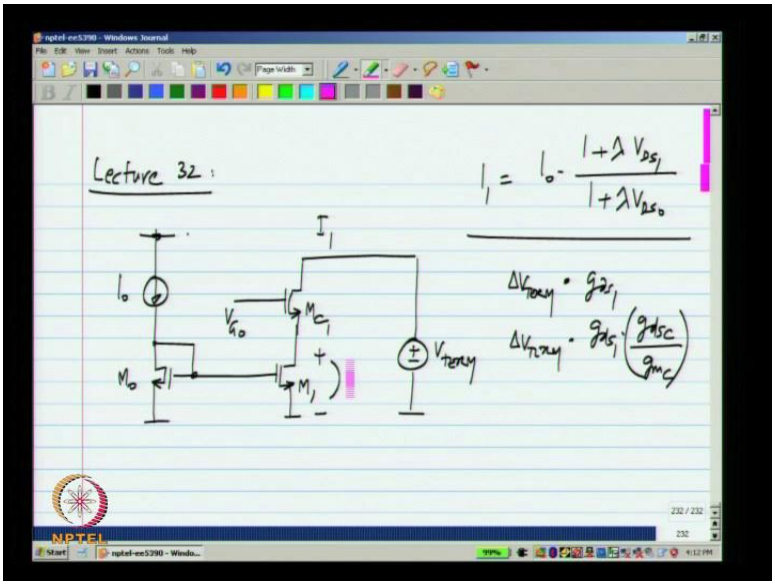
Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture No - 33
Telescopic Cascode Opamp

Hello and welcome to lecture number 33 of analog integrated circuit design, at the end of the previous lecture we looked at cascoding that is using a common gate amplifier as a possible way of increasing the output resistance of trans conductor, and thereby increasing the DC gain. So, we will start with analyzing this cascode combination in little more detail, and then apply to our single stage op amp to come up with a op amp that has a higher DC gain.

(Refer Slide Time: 00:38)



A cascode is combination of common source and common gate amplifiers, now the lower device does not have to common source, it can just be current source a fixed current source. Even then the output resistance would be improved, this could be let us say V bias, if it is just V bias it is a current source, and if it has V bias plus V i it is a common source amplifier.

And the output resistance in either case would be g m C r d s C r d s 1 plus r d s c plus r d s 1 it is dominated by this term and we will frequently use that as an approximate value of the output resistance because, it is going to be definitely much more than either of

these two terms. Now, the advantage with this is that you can get an order of magnitude increase in the output resistance, without in increasing length, increasing the transistor length would slow down the circuit. Whereas, this does not appreciatively change the circuit.

Now, where can we use this cascodes they are actually used in widely in integrated circuits, let us start with a current mirror which is used as current source. If I have a current I naught, the output current nominally is also I naught, let me terminate the output with a voltage source V term and this current is also I naught. Now, we know that the current is also influenced by the drain source voltages of the transistors.

So, the drain source voltage of M 0 and M 1 could be different, and this current I 1 will really be equal to I naught times 1 plus lambda V D s 1 which is lambda V term divided by 1 plus lambda V D s 0. And also you see that this V D s one is nothing, but V term, so as the terminating voltage changes the current here changes as well, now this is undesirable if I want the output to be closer to the ideal current source, I would like times have a higher incremental output resistance for the current source.

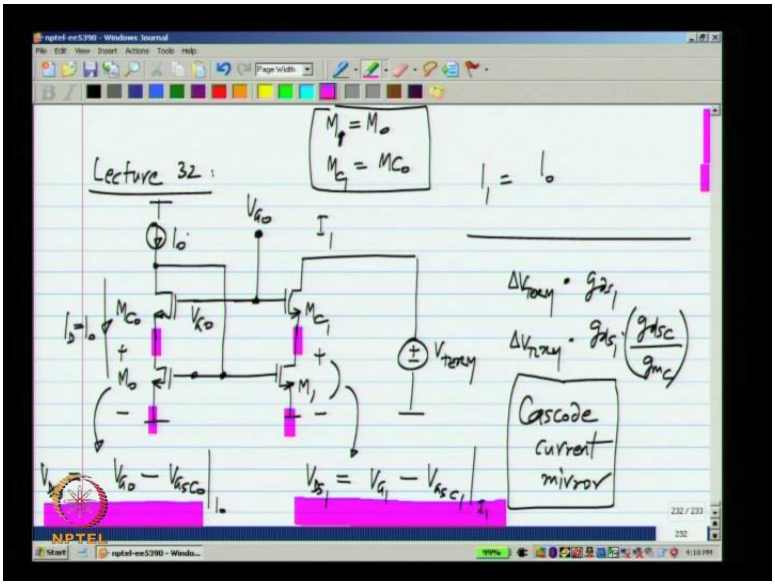
In fact, the current source would ideally have an incremental resistance of infinity, now I know my cascode trick. So, what I will do is take this current and I have a common gate structure on top of it, let me bias it with some V G 0, which will maintain all transistors in saturation region. Let me call this M C 1, now I do know that the current here will not be affected significantly by V term. If I change V term by let us say some delta V term, originally I would got a change out delta V term times g d s 1.

Now, I will get delta V term divided by the output resistance of the combination, and if I write it in terms of g d s 1 it will be g d s 1 times g d s c divided by g m c. Now, this g d s c by g m c is number that is much smaller than one, so the change in current due to the change in output voltages much smaller than before. So, this is a better current source, but the uncertainty in this value of the currents still remains because, this current I 1 is related to the V d s of M 1 and the V d s of M 0 it is given by the same formula, where this is not V term anymore, but it is V d s 1.

So, this is a better current source in that it is not significantly affected by changes in V term, but it is not equal to I 0. Now, how would I make it equal to I 0, I already know that the current would depend both on V d s and V g s. So, I have to make sure that the V

d s of M 0 and V d s of M 1 are exactly the same, then the two currents would be exactly identical to each other.

(Refer Slide Time: 06:02)



Now, how do I arrange for that let us go back to how we came up with the divert connected arrangement, the way to think about this is that you are subtracting the current I D from the desired current I 0. And apply a negative feedback to the transistor, and the transistor is a trans conductor, if the gate voltage increases, if the voltage at this node increases the current here increases. And that tends to lower the voltage and finally, the circuit reaches equilibrium when I D is exactly equal to I naught.

Now, let us say that I have a transistor and I use a cascode transistor on top of it, if you look at the behavior between these two points. How it responds to voltages here, what happens now if I have an increment V g s apply to the gate of the M 0, I will have an increment g m 0 times V g s. It is exactly the same as what I would have here, if I had an increment V g s here I would have an increment of g m 0 times V g s.

The only difference is that this M c 0 will improve the output resistance of this combination, this is as same V G 0. Now, I can use exactly the same structure with the cascode combination, I subtract whatever current is flowing here I D from reference current source I naught, and I know that the current I D is controlled by this V g s. So, if I D is more than I naught this voltage is smaller if I D is less than I naught this voltage becomes larger.

So, I complete the feedback look like this, and this feedback loop also is stable when I D is exactly equal to I naught. Otherwise this voltage will be either increasing or decreasing, and the circuit will not reach steady state. So, what is the difference between this circuit and that circuit, in the circuit on the left side I D equals I naught and the V D s of M 0 equals the V G s of M 0. Whereas, in the circuit on the right side what is the value of V D s of M 0 that is equal to the gate voltage of M c 0 that is V g 0 minus gate source voltage of M c 0.

Now, the key point here is that this V D s is independent of V D s of m 0, so therefore, it can be independently adjusted. And earlier I said that I wanted to make the V D s of M 0 equal to the V d s of M 1 because, I have an independent nub to adjust the V D s of M 0, I will adjusted such that I have a exactly the same V D s for the two transistors. So, let us go back to that circuit, let us say I connect some V g 0 over here, and I do biasing by connecting a feedback to the gate of M 0.

The current here will be I D equal to I 0, and also the V D s of M 0 will be V g 0 minus V G s of M c 0. Now, let us say here to the gate of M c 1 I connect a voltage V G 1, what will be the V D s of M 1 this is V D s of M 0 V D s of M 1 will be V G 1 minus V G s of C 1 by the way I have to add the currents here V G s depends on the current. So, this is V G s c 0 at a current of I 0, and this is V G s c 1 at a current of I 1.

Now, let us say I want a one to one current mirror that is M 0 and M 1 are identical and I want I one to be equal to I naught. So, then it is very obvious that if I make M c 0 and M c identical, they will have the same V G s at a given current, so I will bias these two voltages from a common voltage V G 0 that I will obtain from somewhere. And now M 1 and M 0 are identical to each other M c 1 and M c 0 also identical to each other.

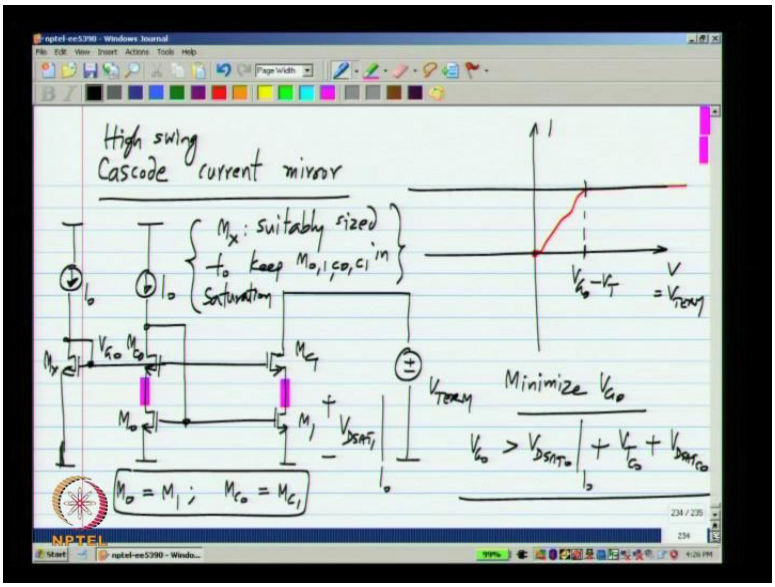
So, under these conditions you can work out that the V D s of M 0 and V D s of M 1 are exactly equal to each other. So, I 1 will be equal to I 0 V D s 1 and V D s 0 are equal to each other. So, I 1 simply equals I 0 also M c 1 is a cascode transistor for M 1, so any change in this output voltage V term will cause only a very small change in the current. So, it is a better current source as well, so this is known as a cascode current mirror, this structure is a cascode current mirror.

And it has a great of accuracy because, the V D s of M 0 and M 1 are match to each other, it also has a higher output resistance. So, overall it is a much better current mirror

than the conventional current mirror that we had been using along, this is also very widely used circuit to be generate accurately mirror currents. The only thing now is to determine the value of V G 0, such that all transistors remain saturation.

This is a precondition because, M 0 and M 1 have to remain in saturation, they have to behave like current sources. And M c 0 and M c 1 also have to be in saturation because, if the cascoding has to be effective it is g m times R d s product has to be a much larger number than one, and for that to happen it has to remain in saturation region, so all transistors have to remain in saturation.

(Refer Slide Time: 13:24)



This is my cascode current mirror instead of a single transistor I will use two transistors in each path, and this is connected to some bias voltage V G 0, M 0, M 1, M c 0, M c 1, I am talking about one to one current mirror. So, M 0 and M 1 are identical to each other, and M c 0 and M c 1 are identical to each other, now what should be the value of V G 0 first of all, the current source in reality will provide a constant current regardless of a voltage across it, the I V characteristic of current source would be something like this.

In reality it will have some voltage range beyond which it will not be behave like a current source. In this case what is the value of V term beyond which this will not behave like a current source that will be when M c 1 enters triode region that is V term goes below V G 0 by 1 V T. So, if you look at V G 0 minus V T and the voltages below

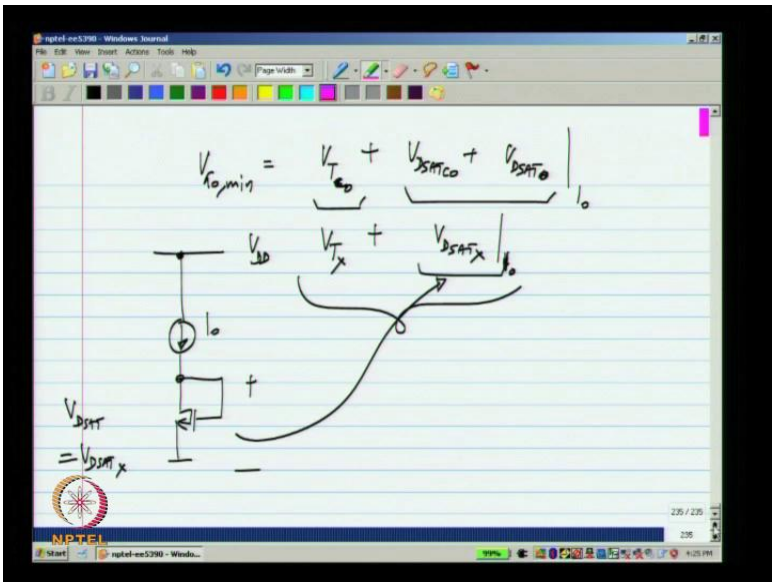
that what happens is at above this it behaves like a current source, and below it will do something and the current will go of to 0 when V term is 0.

In our case V term equals V term, we would like to this circuit of behave as a current source over as a wider range as possible. So that means, that we should keep this V G naught by V T to be as small as possible, which is basically V G naught to be as small as possible. Now, how small can V G naught be as V G naught reduces these two voltages follow V G naught, if you think of this circuit I have with V G naught as input and the source of M c 1 as output it is a source follower or a common drain amplifier.

So, this voltage will be below V G naught by 1 V G s, so if V G naught keeps reducing the V d s of M 0 and V d s of M 1 keep on reducing, and they will enter triode region. So, we know that we have to have at least some V D sat 1 at a current of I 0 across these transistors, these numbers are equal because, they give the identical transistors and identical currents are flowing through them.

So, V G naught has to greater than V D sat 0 at a current of I 0 plus the V G s of M c 0, which intern can be written as V T of M c 0 plus V D sat of M c 0. So, that is the minimum value possible for V G naught without driving and transistor into the triode region. And that is the value we must use if we want to maximize the range of the current source, this range usually called the compliance current source, so to maximize the compliant should bias V G naught at the lowest value as possible, and the lowest value equals one thrasher voltage plus 2 saturation voltages.

(Refer Slide Time: 17:42)

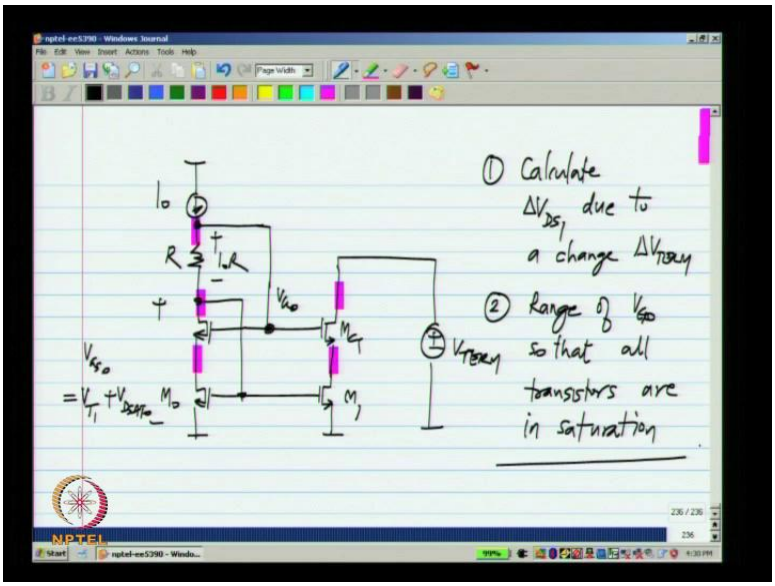


And how can we generate this because, the optimum value is a thrasher voltage plus 2 saturation voltages, they can be obtained by using a mos transistor. In fact, you see that this is the form of some let me call it V T x plus V D sat x at some bias current, so I pass a bias current I naught through a transistor which is size. So, that it is V D sat equals this V D sat x, in such a case the voltage across this would be V T x plus V D sat x and that is suitable way of generating V G 0.

Here I will simply say that M x is suitably sized to keep M 0, M 1, M c 0 and M c 1 in saturation, now you can figure out the size based on square law you can calculate the size, now transistor do not necessarily follows square law. So, in that case you have to maybe with little bit trial and error at the size of M x, so that you get the voltage that you want for V G 0. And such a structure is also known as a high swing cascode because, the compliance is the maximum that it can be, you can choose a larger value of V G 0 and the circuit can operate properly.

But, the compliance of the current source would be smaller than what it could be, so this is known as the high swing cascode current mirror.

(Refer Slide Time: 20:16)



Now, this is not the only way to generate the bias V G 0 there are many ways which you can look up in the literature I will just illustrate another way of doing the same, this is my cascode mirror and this voltage is nothing, but the V G s of M 0, which is of the form of the thrasher voltage plus V D sat of M 0. Now, what we need for V G 0 is a thrasher voltage plus 2 V D sates, so V D sat of this transistor plus V D sat of that transistor.

So, another possible way of getting the biasing arrangement is to connect the resistance R, so that there is some drop I naught R I will adjusted to be a sufficient value that it is equal to the V D sat of the upper transistor. So, the total voltage that we get at this node will be the thrasher voltage plus V D sat of this transistor plus some voltage which is roughly equal to the V D sat of the transistor.

So, if I have connected of like that I can have my cascode biasing without using an extra branch, previously I used an extra branch to generate the V G 0, so this is better. Now, the disadvantage is of course, is that the drop between these two voltages is given by I naught R and it relates to the absolute value of the resistance, and that is not very precisely fixed on a integrated circuit. Because, of that there is some uncertainty you have to make sure that overall possible variation of this voltage, node I naught R the transistor remain in saturation region.

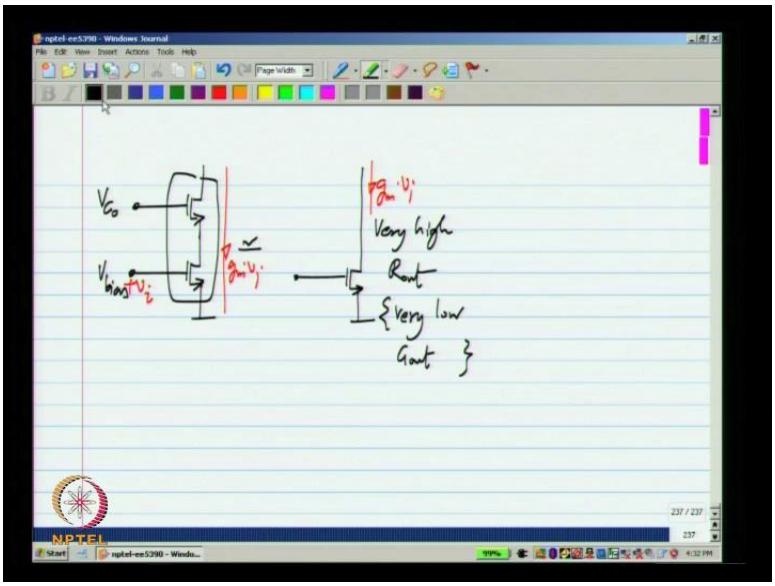
So, there are many other biasing techniques that you can think of to bias the cascode, but the main tech homes is that you can bias, it such that the compliance of the current

source is maximum. And that the cascode current source offers a very high output resistance, now a couple of exercises for you I earlier said that the V D s here and there will be exactly the same, and will be independent of V term. The V D s of M 0 will be; obviously, independent of V term, but what about the V D s of M 1.

So, calculate the change in V D s one due to a change in V term change delta V term, this is a quite a simple calculation you should be able to use small signal techniques to do this. And you can see whether my assumption of this V D s is being exactly the same as that is justify or not because, in reality the current in the left side and right side will be exactly equal, only when this voltage and that voltages are equal, and this and that are equal.

Now, what we are made sure is that the V D s of the bottom transistors are more or less equal to each other, what happens due to change in V D s of the upper transistor that you calculate from this one. The second thing is please calculate the range of V G 0, so that all transistors are in saturation, we already partialed on this you can also calculate the upper limit for V G 0. So, that is about the cascode current mirror it offers a very high output resistance, and we can use it in conjunction with common source amplifier as well to obtained a high resistances.

(Refer Slide Time: 24:26)

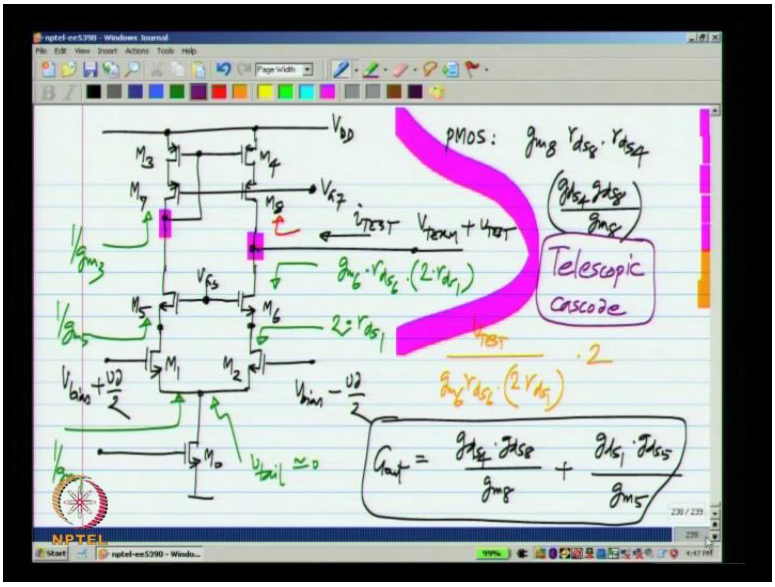


In general if you have a common source structure by that what I mean is we have the source to be grounded, and I can apply some voltage to the gate whether it is signal

voltage or a bias voltage. And I use another common gate transistor on top of it, this compound transistor can be thought of approximately as a single transistor with a very high R out, very high output resistance or equivalently a very low output conductance. This is a very useful view while synthesizing circuits because, we are putting more transistors at it look like a very different circuit from before.

But, you can think of this combination as a transistor by itself, we know that the transistor is a voltage controlled current source. If I apply V i here I get g m times V i over there, now we also know that now this is the same as what we would have with the single transistor, the incremental current here is g m times V i, the only difference is that the output resistance is very high. So, in some way it is reasonable to think of as a single device while synthesizing circuits, after we have the circuits we can analyze the complete circuit including the effect of these different transistors.

(Refer Slide Time: 26:25)



So, how is this useful for our single stage op amp I have my differential pair, and that contributes a resistance of G d s 1 to the output resistance. So, as I said earlier we can think of the cascode combination as a compound transistor with a high output resistance, so I pass the currents of both M 1 and M 2, we know that if I have V bias plus V d by 2 and V bias minus V d by 2 I will have an incremental current g m V d by 2 here, and g m V d by 2 in the upward direction, in the other transistor I use cascode transistor with both M 1 and M 2 let me call them M 5 and M 6.

And the gate is bias to some voltage I will not worry about how to generate that, but it is bias to some fixed voltage I will call that V g 5. Now, it is very clear that the same incremental currents will flow in M 5 and M 6, the only difference will be that the resistance looking into the drains of M 5 and M 6 would be much more than what would be looking into the drains of M 1 and M 2. So, this is also a differential trans conductor which gives an incremental current of g m V d by 2, but with a much higher output resistance.

Earlier I had a current mirror, the current mirror contributed an output resistance of g d s 3 I could used a same current mirror. But, we know that the output resistance of the differential pair, and the output resistance of the current mirror appear in parallel or the output conductance is added up, we had g d s 1 plus g d s 3 there is no point improving only one of them without improving the other one. So, we will use the cascode combination for both the load transistors, and the differential pair transistors.

We know how to make the cascode current mirror I have to add two more transistors, let me call them M 7 and M 8, and this is the current mirror and this is V G 7 which I will connect to some voltage, for now I will just say that the V G 7 is such that all these transistors are in saturation. Similarly V G 5 is such that all these transistors are in saturation, so now, I connect the two things together and take my output from there, I could connected to a capacitor.

So, this is my new single stage op amp with an improved output resistance, what I have done is to use cascode transistors in place of M 1, M 2, M 3, M 4 that improves the output resistance of each of those stages. The operation is exactly the same as before, you can go head and analyze it completely, and you will find that essentially all we have done is to replace each transistor by cascode. So; that means, that any place we had an output conductance, now we have a much smaller output conductance.

So, I am not going to do the analysis further separately for this op amp, like before though the circuit is asymmetrical. If we terminate the output with a voltage source V term, the impedance looking up here and looking here will become very small, so the tail node voltage will almost 0. So, with that condition we can analyze the circuit very easily, exactly like we did for the single stage op amp with a simple differential pair in the current mirror.

So, using that you can analyze the circuit and then find out everything about this particular circuit. Now, in the quiescent condition when the two inputs are at V bias because, of a symmetry this voltage and that voltage will be exactly the same that is the drain of M 6 and M 8 will be the same as the drain of M 7. And we can use the arguments that we used earlier with the other circuit, if we assume that it is any different will come up with the contradiction. So, this voltage will be exactly the same in absence of any mismatch.

So, this voltage will be at V D D minus V s g 3 just V D D minus V s g of transistor M 3, now I terminate that with a voltage V term as V D D minus V s g 3. So, in the quiescent condition the current here will be 0, and if we apply an increment some current will flow them. So, if I apply plus V D by 2 minus V D by 2 over here, the tail node voltage will be almost equal to 0, so the two currents will be g m V D by 2 in opposite directions. So, the total current, in fact, will be g m 1 times V D exactly the same as before.

So, as usual I will use g m 1 to denote the small signal trans conductance of both M 1 and M 2, similarly g m 3 for M 3 and M 4 and, so on. So, the trans conductance is exactly the same as before, the output conductance is a different story analyze again as similar to what we did earlier. If I apply an incremental test voltage, and measure the current i test I am taking the ratio of V test by i test I can find out the output resistance.

Again it is useful to imagine that the n mos transistors for ideal that is they had 0 g d s, and calculate the contribution of p mos transistors. And similarly assume p mos transistors are ideal and calculate the contribution of n mos transistors, now it turns out that the resulting output conductance is a sum of these two, you can do the analysis separately and then do the analysis together. So, that you do not get work done by complexity.

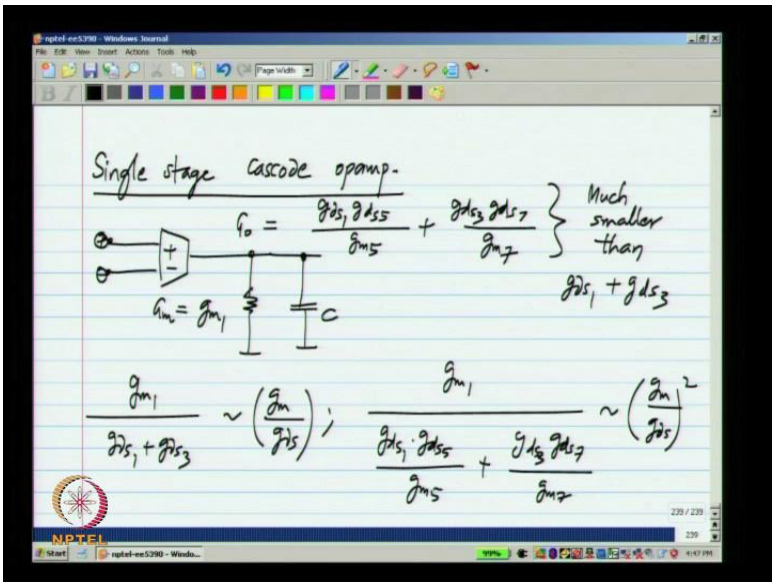
If I have a voltage V test here, now this cascode combination presents an output resistance equal to g m 8 r d s 8 r d s 4, it also has plus r d s 8 plus r d s 4, but I am going to ignore that. If I had to denote the output conductance it would be g d s 4 g d s 8 divided by g m 8, now what happens on the n mos side, n mos side it is a similar story to before. First of all looking from the source of M 5, the drain of M 5 is terminated by a low resistance.

You can easily verify that the incremental resistance of this combination because, of this feedback connection around M 3 will be 1 over g m 3. And the incremental resistance looking into the source of the M 5 will be 1 over g m 5, the incremental resistance looking into the source of M 1 will be 1 over g m 1. So, the incremental resistance looking into the drain of M 2 by arguments that we used earlier is approximately 2 times r d s 1.

And the incremental resistance looking in there would be g m 6 r d s 6 times 2 times r d s 1, again I ignore plus r d s 6 plus 2 r d s one terms, they are much smaller than this one. So, if I apply V test the current that flows into the m mos would be V test divided by g m 6 r d s 6 times 2 r d s 1. As before this current gets mirrored in M 3 and M 7, and also gets drawn into M 8 and M 4, so the total current drawn will be 2 times that half of it goes into the n mos side, half goes into the p mos side.

And the total current including the output conductance of the p mos transistors, will give a total output conductance of g d s 4 g d s 8 by g m 8 plus g d s 1 g d s 5 divided by g m 5 g m 5 and g m 6 are the same, g d s 5 and g d s 6 are the same. Compare this to what we had earlier we had g d s 1 plus g d s 3 now we have numbers they are much smaller than g d s 1 and g d s 3 adding up. So, our output conductance is much smaller, the trans conductance is exactly the same as before. So, this is simply a way of making a trans conductance whose output resistance much higher consequently the DC gain will be much higher.

(Refer Slide Time: 37:58)



This is known as a single stage cascode op amp, now it is called single stage because, it is still consist of a single trans conductor, and whose trans conductance equals g m 1 and its loaded by the capacitor we have an op amp the difference is that, the output conductance is much smaller than before. Now, if you connect the resistive load to this it will not be any better than our simple single stage op amp, assuming that the resistance is smaller than the output conductance of the single transistor.

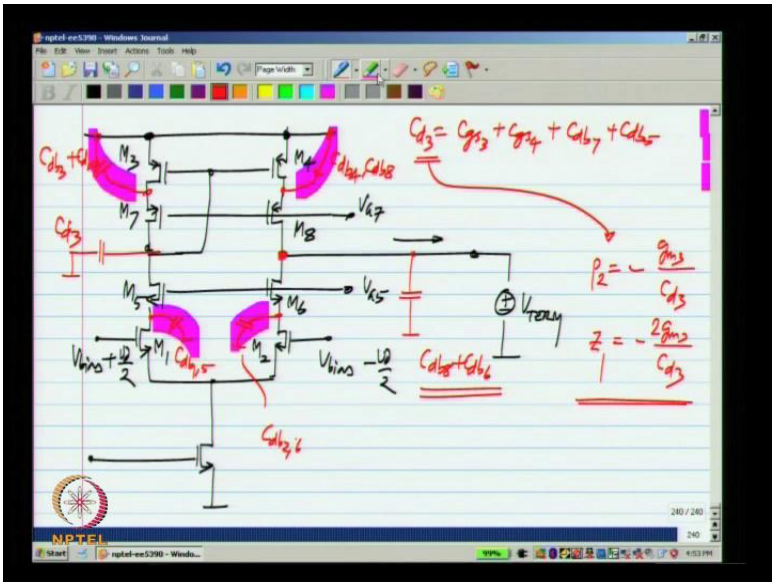
Whether the use a cascode op amp or whether use the simple op amp, you will get the same gain because, the output load resistance should be dominated by the load that you connect. So, this circuits still cannot be used with resistive loads, but if you used it with a purely capacitive loads that the DC gain will be a lot higher, earlier the DC gain was g m 1 by g d s 1 plus g d s 3 which is of the order of g m by g d s of a single transistor.

Now, we will have g m 1 by this entire thing g d s 1 g d s 5 by g m 5 plus g d s 3 g d s 7 by g m 7 and this is of the order of g m by g d s square. So, if you get a gain up to 100 with a simple stage op amp, you could gain up to 10,000 with this cascode op amp, now this type of cascode op amp where things are stacked on each other, if you look at the cascode structure, you have the differential pair on top of that you have the cascode, on top of that you have the cascode of the current mirror.

And on top of that you have the current mirror itself, such a structure is known as the telescopic cascode op amp, this thing is known as the, so it has an improved DC gain.

Now, we have to evaluate other things as well just like we did for the simple single stage op amp, like the frequency response, the non dominant poles and 0's and, so on, we will do that in a approximate way because, already you see that the circuit has become quite complicated. If we put down the small signal equivalent circuit of all these transistors together, and then write the eight equations and eight unknowns or something we will not get anywhere. So, we will use approximate calculations, and our intuition to simple circuits to come up with and answers to those questions.

(Refer Slide Time: 41:36)



So. Firstly, the non dominant poles and 0's of this op amp V g 7 and V g 5 are such that all transistors in saturation region. As usual we will evaluate the small signal trans admittance by terminating it with a voltage source, now with every node we will have parasitic capacitors, and this circuit has lot more nodes than before. But, the primary parasitic was this one which we call C d 3 which consists of C g s 3 plus C g s 4 plus c d b 7 plus c d b 5, it is similar to what was before.

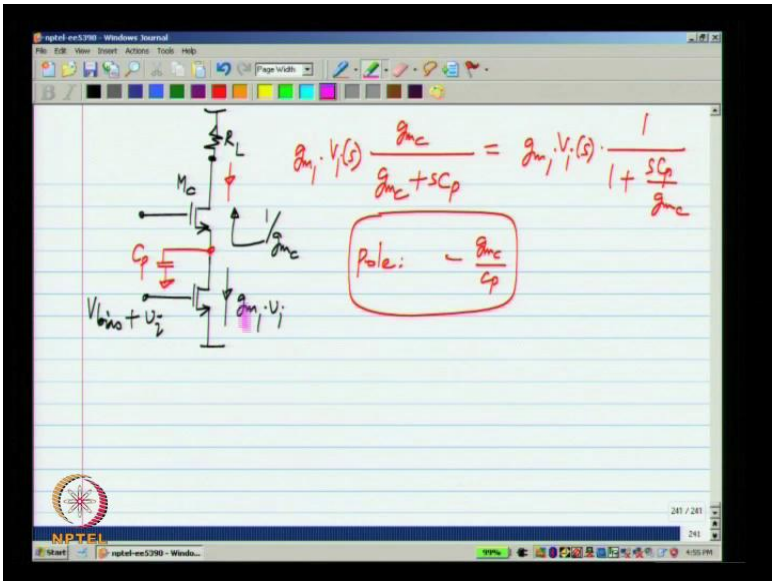
And any parasitic at the output of the op amp such as C d b 8 plus C d b 6 this could observe into the load. So, this primary parasitic capacitance still remains, in addition to that we will have parasitic capacitances at these other junctions for instance this will be C d b 3 plus C d b 7 this will be consist of C d b 1 and C d b 5 this will be C d b 2 and 6 and, so on, this will be C d b 4 and C d b 8.

Now, what I will do is to ignore all of these parasitics this that and that and consider only C d 3. Now, as you guess from the structure the effect of C d 3 is exactly the same as before, if I apply a differential increment to M 1 and M 2 what I get is a current of g m 1 times V D by 2 and M 1 minus g m 1 V D by 2 and M 2. Now, the current in M 1 gets mirrored by the current mirror, and it is driven to the output, the current in M 2 goes directly to the output.

This was exactly the case that we had with the simple differential pair, as you can see at high frequencies the current in M 1 goes into the capacitor and none of it gets mirrored. So, we will have the pole and 0 doublet exactly as we had before, we have a pole at g m 3 by C d 3, and we will have a 0 at twice that frequency, the 0 happens to be at twice the frequency.

Because, this pole affects only one half of the signal the part of the current that is coming from M 1, though the effect of C d 3 is that we will have a non dominant pole at minus g m 3 by C d 3 and a non dominant 0 at twice that frequency. The dominant pole can be calculated from the output resistance of the trans conductor, and the integrating capacitor that you have C. Now, what about this other parasitic capacitors that we want do the exactly analysis, but we will try to get of feel for what their contribution will be by looking at a simple cascode stage.

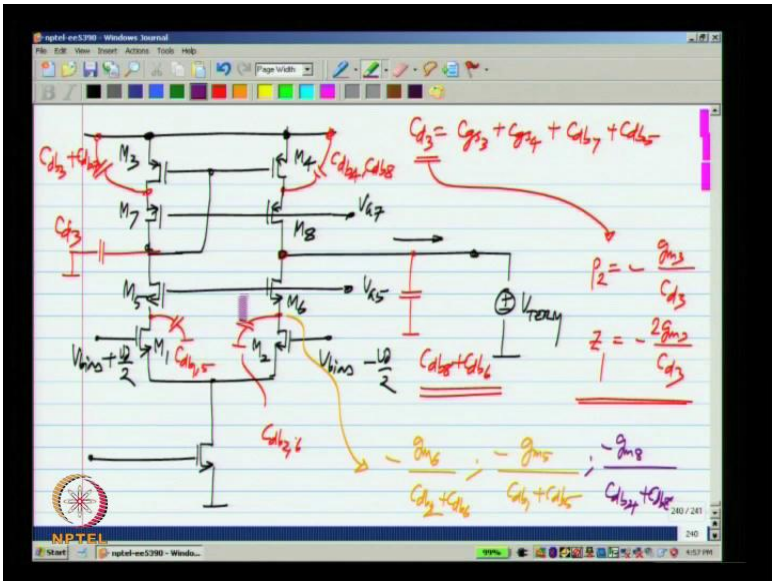
(Refer Slide Time: 46:20)



So, let me take the common source amplifier which has some V bias plus V i, so it has an incremental current of g m 1 times V i, it goes into the cascode device and I will assume that this is terminated by some low impedance load. So, the incremental resistance looking up would be if I call this M c 1 over g m c.

Now, let us say I have some parasitic capacitance from this node to ground, what will happen the current gets divided between the input resistance of the cascode, and this parasitic capacitance C p. So, the part that comes out of M c would be g m 1 V i of s which is the total current times the ratio given by impedance division, which is g m c by g m c plus s C p which can also be written as g m 1 V i of s times 1 by 1 plus s C p by g m g m c. So, there is a pole at minus g m c by C p due to this parasitic capacitance C p, now this is expected because, at high frequencies all of this current will go there, and at low frequencies all of it will go to the output. So, there will be the pole somewhere in the middle and the pole happens to at minus g m c by C p.

(Refer Slide Time: 48:10)



Now, what happens in our cascode op amp, the current from M 2 goes through M 6, but there is a capacitance here which is C d b 2 plus C d b 6. So, from here at this node we will get a pole which is minus g m 6 divided by C d b 2 plus C d b 6, similarly the current from M 1 goes through M 5 and that has the same a behavior. So, we have a pole at g m 5 by C d b 1 plus c d b 5, by the way the small signal parameters of M 1and M 2 are the same M 5 and M 6 are the same, so these two poles will be at the same frequency.

Now, the current in M 1 gets mirrored and then comes out of the M 4 again encountered the same behavior there is a current division between the g m of a M 8 and this parasitic capacitance. So, we will have g m 8 by C d b 4 plus C d b 8 as another pole now the effect of this is a little more complicated because, it is inside a feedback loop of it is own, but it turns out or it creates a pole and some 0, which is related to a similar number it is g m 7 by C d b 3 plus C d b 7.

Now, in this case I have used C d b instead of c s b, but in a given transistor C d b and C s b are almost equal to each other. So, for instance in this case it should be C s b 5 plus C d b 1, but I have used the some capacitance here, so there will be lots of poles and 0's one for each cascode node, and all of those have to be taken into the account while designing the op amp.

So, in practice what you do is you simulate the circuit, and the simulator will taken into the account the effect of all of these things, and give you the magnitude and phase and by looking at the phase margin you can decide whether these parasitic poles are at a sufficiently high frequency or not.

Thank you we will continue this further in the next lecture.