Analog Integrated Circuit Design
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Lecture - 32
Opamp with Single and Dual Supplies; Single Stage Opamp Tradeoffs

Hello and welcome to lecture 32 of Analog Integrated Circuit Design. In the previous class, we looked at the design of single stage opamp at the transistor level. We used differential pair loaded by current mirror as a trans conductor and that, when loaded by capacitor, gives us the opamp.

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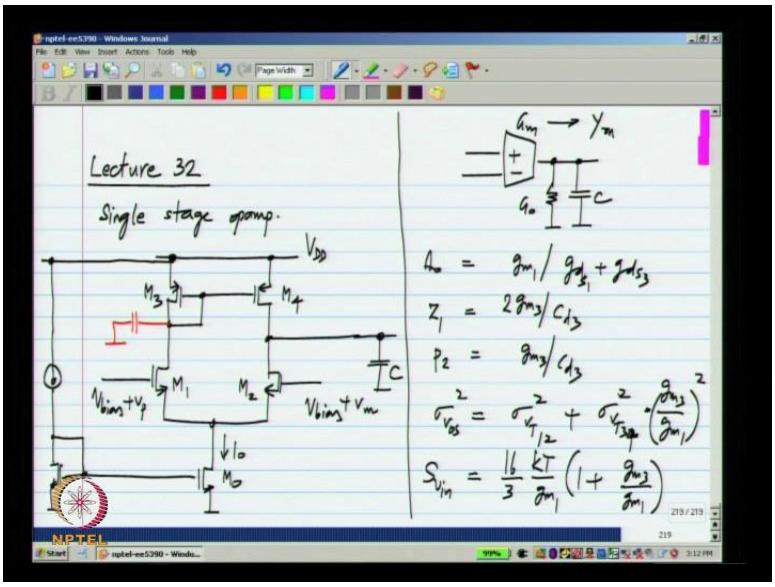

This is the tail current source and it will be biased from a current mirror, let us say that tailed current is I naught, this is the output and the output when loaded by capacitor becomes an integrator. Even if the capacitor is not expressively loading the output of the opamp, we will have the parasite capacitors, which will limit the unity again frequency. The drained parasitic of M 4 and M 2 will be part of the load capacitance or the integrating capacitance.

Now, this is equivalent to basic circuit that we started with, a trans conductor G m loaded by capacitor, the trans conductor will have some output conductance G o. So, in our case, the dc gain A naught is g m 1 by g d s 1 plus g d s 3, the trans conductor it turns out is trans impedance with zero and the pole. So, it will be 0 at 2 times g m 3 by C d 3, where

C d 3 is the parasitic capacitance loading this node, it consist of per capacitances from M 3 M 4 and M 1.

And the non dominant pole P 2 is g m 3 by C d 3 I mean, both of these are in the left half plane, I am just showing it as both the pole and zero are in the left half plane. So, that means that, the actual pole and the zero are at minus P 2 and minus Z 1, those are the small signal characteristics of the opamp. We also know that, the input refer offset as a variance, given by variance of the offset between the input pair transistors and the mismatch variance between the load transistor times g m 3 by g m 1 square.

And the input refer noise spectacle density is given by 16 by 3 K T divided by g m 1, which is the noise due to M 1 and M 2 times 1 plus g m 3 by g m 1. The second term here is the noise due to the load, both the offset and noise contribution of the load can be reduced by reducing the trans conductance of M 3 and M 4. So, we are able to evaluate all this and then, we can decide, whether it is suitable for our application or not by looking at the value of the noise and offset, etcetera.

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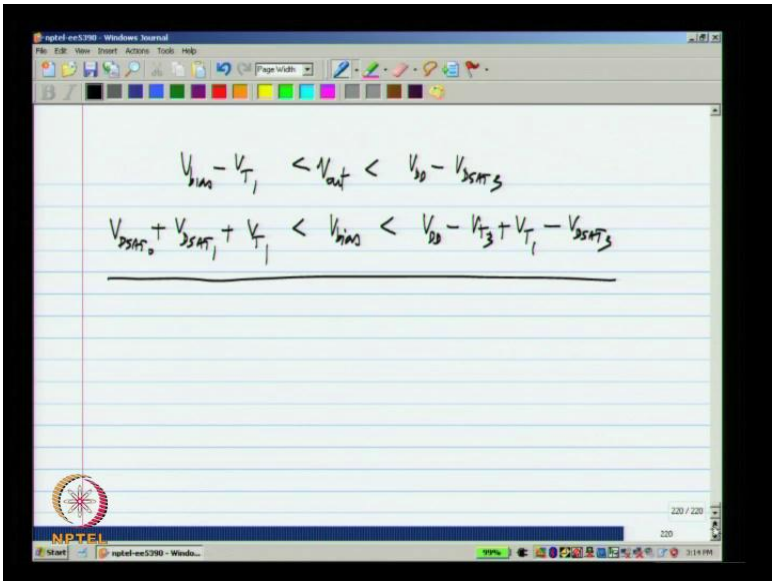

We also evaluated that, the output voltage has swing limits of, we decide 3 below V D D and at threshold voltage, below V bias and V bias itself has V bias plus V T 1 and a lower limit of V D sat 0 plus V D sat 1 plus V T 1. Both these ranges are skewed towards the upper side, they are lot closer to V D D than to ground and this is a consequence of using

NMOS input transistors with PMOS input transistors, the ranges could be lot closer took the round than to V D D.

Now, we know that, in the cohesion condition, in absence of any mismatch, this node voltage will be exactly same as that, so the operating point of this will also be add V D D minus V g s of M 3. Now, what should be the value of this V bias, that depends on the circuit that we use. Now, to clarify that, let us look at the operation of the opamp with the dual rail and single rail voltages.

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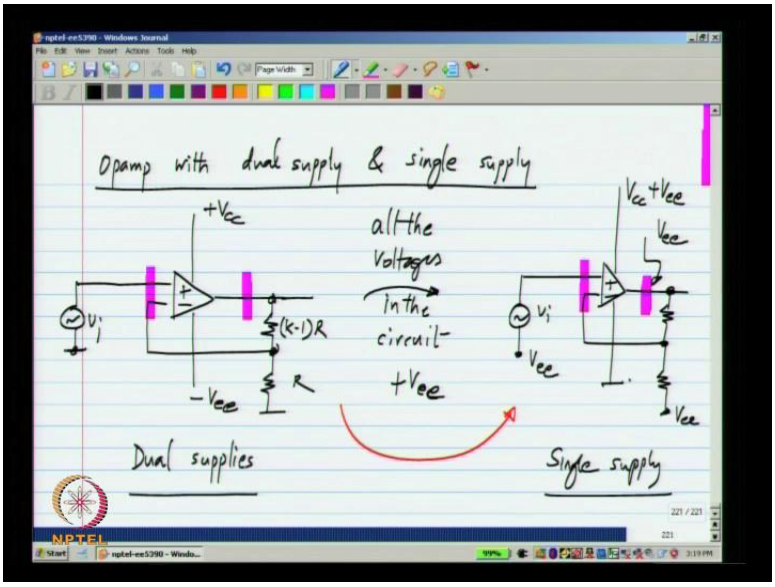

Now, normally when you see the text book introduction to the opamp, it will be operated with dual supplies and the input is just shown as, having a quotient value of 0, this is an example circuit. So, the quotient value of the output is also 0 and the quotient value of the input is 0, but this does not necessarily have to be the case, the quotient value of the input could be anywhere within the input common mode range of the circuit.

So, for instance to this, I could add some V bias and that means that, I could also add V bias to this one. So, in this case, basically all the quotient voltages at the input and the output get shifted by V bias. Now, V bias can be any value that I want, that will fall within the foot common mode range of the opamp. Now, the way we have designed the opamp, we are representing the opamp, we do not have these two supplies, plus V c c and minus V c c with respect to some ground.

What we have are, single supply of V D D and the bottom rail is what we called ground, how does it make a difference to the opamp, it does not. It turns out that, any opamp can be operated with single supply or dual supplies, it just the matter of, what we called ground. So, let me remove this V bias, first of all I will do one thing, I will simply shift up all the voltages in the circuit by V c c. To all of this, I will add V c c, by the way one more thing to keep in mind is that, the upper and lower rails need not be at the same voltage.

So, in fact let me make them different, let me call them V c c and minus V e e and I will shift all the voltages in the circuit by plus V e e. What happens then, the V e e over there, 0 and this will be V c c plus V e e, now the quotient operating point of the output will be V e e of both the input and output and there is absolutely no difference between this circuit and that circuit. So, it is just that we called the bottom rail, the ground here and here we call some point between V c c and V e e, the ground.

What is important is that, the input common mode of the opamp be within the input common mode range and the output of the opamp be in the output range. So, similarly here, the same thing is the case, in fact as I mentioned, there is no difference between the two circuits, only change that has happen is that, all the voltage shifted up by plus V e e. So, this is the opamp with the dual supplies and this is the opamp with the single supply, so any opamp can be operated either with dual supplies or a single supply.

Now, the range of the opamps are related to the upper supply rail and the lower supply rail. Now, what we called the upper and the lower supply rail is upto us, we can call them to be some positive voltage, some negative voltage and some intermediate point to be ground. Now, when we do that, usually that ground falls within the input and output ranges of the opamp. So, we can choose that ground to be the operating point of the input and output. When we choose the lower rail to be ground and upper rail to be some positive voltage then, the operating range will not include ground. So, we have to bias the input as well as the output at some intermediate value.

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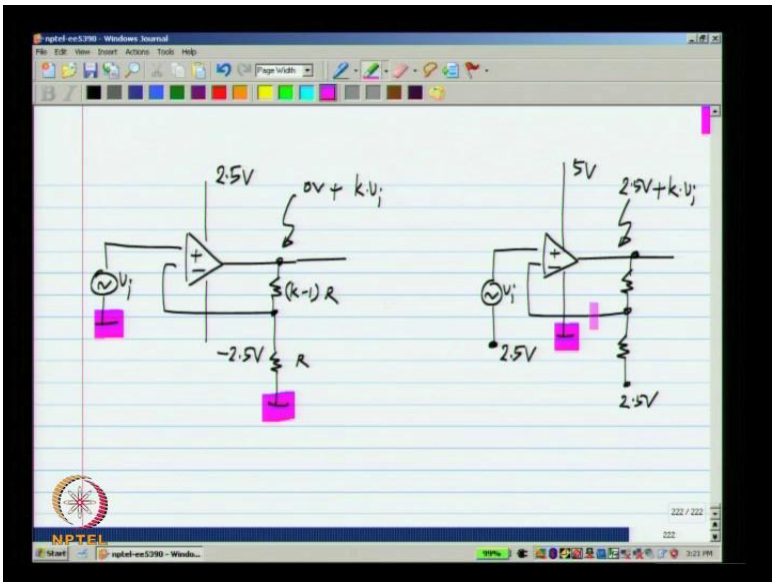

So, just to give an example, so let us have an opamp operating with plus and minus 2.5 volts, this is an non inverting amplifier of gain K. The output will have quotient value of 0 volts and on top of that, we will have K times V i, which is the incremental output, it will be K times the input increment. Now, exactly equivalent to this circuit is, if we have the opamp operating with the single 5 volt rail and v i terminated to 2.5 volts and this resistive divider also terminated to 2.5 volts.

So, in this case, the operating point here will be 2.5 volts and on top of that, we will have K times V i. As you can see, if you take any two nodes in this circuit and in this circuit and measured the voltage difference between them, they will be exactly the same. What is different is, what you called 0 volts, this point is what we call 0 volts in the circuit on the left side and this point is what we called 0 volts in the circuit on the right side let two are different by 2.5 volts.

So, as you know, the absolute value of the voltage reference does not mean anything, it is the voltage differences nodes, that matter, so all opamps can be operated with single and dual rails. Now, in CMOS IC design, it is very common to use a single rail for all the representations, the single stage opamp that we have, could very well be operated from this being a positive voltage and the lower rail being a negative voltage. In that case, their input V bias and the output could be at ground, that is possible, but we will follow the usual convection and show single supply voltages.

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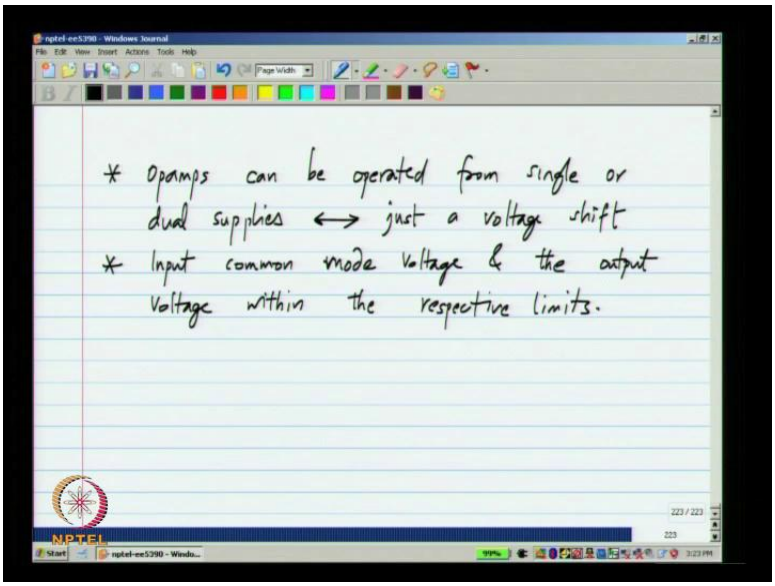

The really relevant thing is to have the input common mode voltage and the output voltage within the respective limits. Now, usually to maximize the voltage swing, you need to keep the operating point in the middle of the range. So, let us say we have some upper limit for V out and the lower limit for V out. In the quotient condition, if you keep the output voltage to be exactly in the middle of these two limits then, you will have the maximum swing. So, that is a general rule, not applicable to all circuits, so sometimes the optimum may be different, depending on which stage limits first and so on. But, usually you would like to keep the quotient point in the middle of the range.

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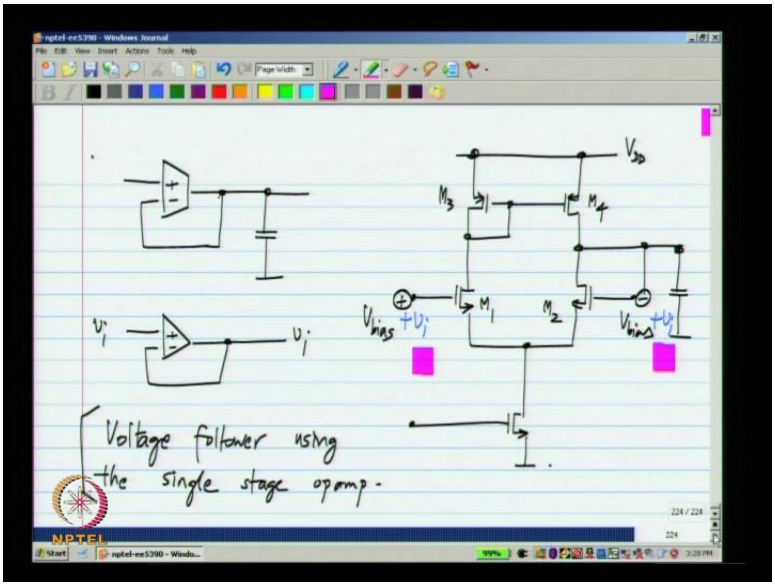

Just an example circuit with our single stage opamp, let us consider the voltage follower circuit with the opamp. So, this you may have seen in this particular form. Now, as we discussed earlier while discussing the opamp at the trans conductor level, we will not use the single stage opamp with a resistive load, because the dc gain becomes very small and then, the opamp will be useless. So, this kind of single stage opamp are used to only with a capacitive load, when we have resistive load, we have to do something more elaborate, we will come to that later.

So, when I have an input increment of V i, the output will also have an increment of V i, what does it mean, let me put on the transistor level circuit. This is my opamp, that is the output and these are the plus and minus inputs, I have the output terminal connected to the negative input so that means, I have to connect this here. Now, let us have some bias voltage V bias then, this will also be at a bias voltage V bias, this is because the current in M 1 and M 2 have to be equal due to the current mirror.

First imagine that, you have a case where transistors have no output conductance, so the opamp has an infinite dc gain. Now, M 3 and M 4 form a perfect current mirror, so this current and that current have to be equal and the sum of those two currents has to be equal to the tail current. So, equal current I naught by 2, I naught by 2 flows through M 1 and M 2 that means, that their V g s s will be the same and that means that, the output voltage will be equal to V bias.

Now, this is true as long as all the transistors are in saturation region, let us say if M 4 goes into triode region, clearly the current in M 3 and M 4 do not have to be equal. Now, let us have an increment V i, exactly the same principle holds and the output will also have the same increment V i. So, it is very clear that, it is a voltage follower and that is what we expected, because what we have made is the opamp voltage follower using our single stage opamp.

So, in this particular case, v i the input refers to the increment over V bias, we think of some V bias as the bias voltage of the input. The lower rail is at ground, so V bias will be somewhere within the input common mode range and v i is the input. Now, this circuit also serves as a useful vehicle to illustrate the swing limits in an opamp.

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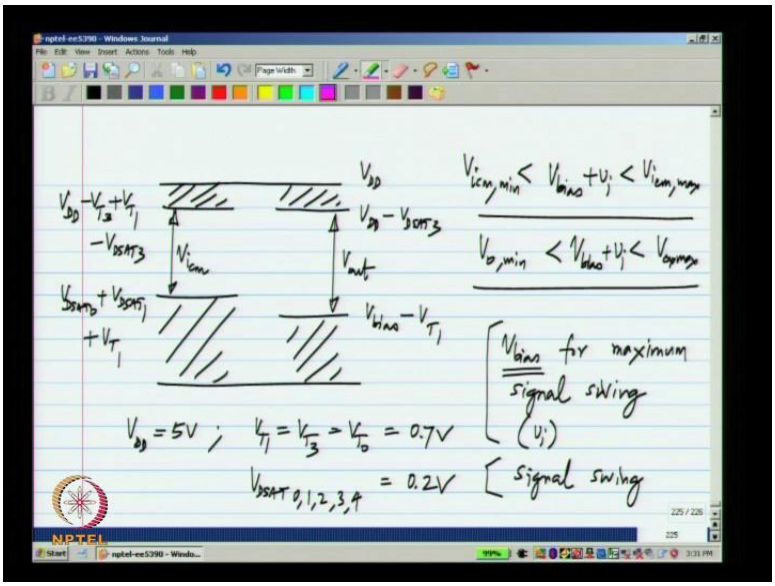

We know that, for this particular opamp, we have V D D, the limit turn the input common mode as V D D minus V T 3 plus V T 1 minus V D sat 3, some voltage close to V D D. And the lower limit is V D sat 0 plus V D sat 1 plus V T 1, this is the range for the input common mode voltage of the opamp. The output range of the opamp will be between V D D minus V D sat 3 and on the lower side, V bias minus V T 1, so it depends on the value of V bias that we choose, this is the range for V out.

Now, in this particular circuit, the output is connected to the input and you can very easily see that, the output voltage is the same as the input common mode voltage. So, the output voltage or the input voltage swing will be restricted by both the input common mode range and the output range, so whichever is smaller, will take effect. So, the input common mode voltage V bias plus v i must be between the limits for input common mode voltage and that should also be within the limits for the output voltage.

So, from these, we can choose the optimum value of V bias so that, the signal swing is maximize, so please take it as an exercise and do that. For simplicity let us assume that, V D D is 5 volts, V T 1 and V T 3 and V T 0, so all V T's are equal to 0.7 volts and again for simplicity let us assume that, all V D sat are 0.2 volts. So, under these conditions, you can calculate the value of V bias for maximum signal swing, where signal refers to v i and you can also calculate the value of the maximum signal swing and the value of the signal swing itself.

So, it is quite easy, you put these constants together and then, find out which value of V bias will give you the maximum. Now, there is a slight complication, not the great deal, introduce by the fact that, the minimum limit for the output is also dependent on V bias, but you can include everything and then, calculate the limits. So, that is how, a single stage opamp is used, you have a trans conductance loaded by capacitor, you have a non dominant pole and the zero, which you tried to keep beyond the unity gain frequency so that, your stability is not affected at all.

And you have some noise and offset, which you can take care off or adjust to any value why, appropriately seizing in the currents and the devices. You also have to respect the signal swing limits of the opamp and I have just showed you for an example circuit of a voltage follower, how to do that. For any other circuit, you can do exactly the same, you can choose the value of the input bias so that, you can get the maximum swing limit that you want, you can also compute the swing limit that you will get. If you want to increase the swing, there are a couple of options, but given a power supply voltage, you will not be able to increase it a great deal.

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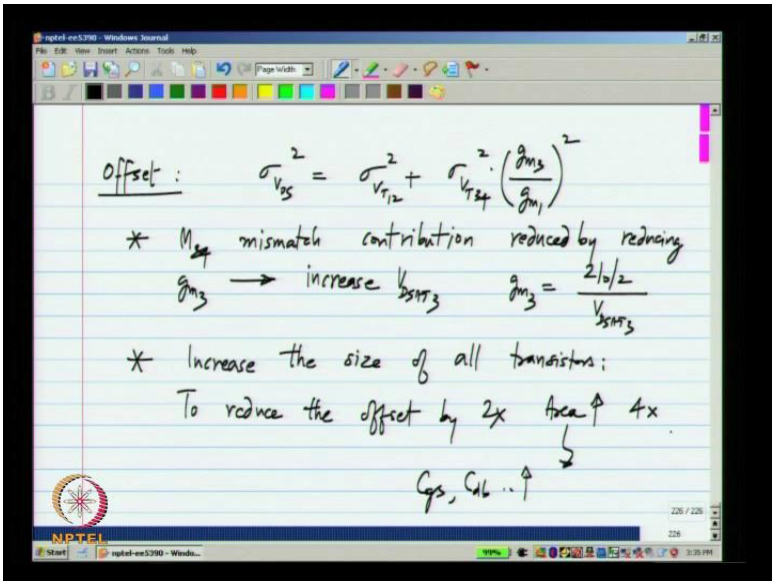

Let us quickly look at, how to optimize the offset and the noise, obviously the offset which is related to mismatch in the input differential pair and the load can be reduced by increasing the size of the transistors. So, first of all, the contribution from M 3 4 reduced by reducing g m 3, now let us say you want to reduce g m 3 alone and you do not want to

effect g m 1, in fact you do not want to effect the differential pair. That means, you keep the tail current and the differential pair devices exactly the same as before.

So, the only way to do that is to increase V D sat 3, because after all what is g m 3, g m 3 is 2 times I naught by 2, the quotient current in those transistors divided by V D sat 3. You have to increase V D sat 3, now what does this mean, this will reduce the swing limit. So, this is a very common trade of that you see, you try to optimize one particular parameter, you will end up having adverse effects on some other parameter. You want to reduce the total offset to increase the size of all transistors.

What happens is, that offset will reduce, so to reduce the offset voltage by factor of 2, you have to increase the area by the factor of 4. When I say reduce the offset voltage I mean, reduce the offset variance by factor of 4 and that means, the area has to go up by a factor of 4. Now, what is the bad consequence of this, this will increase parasitic capacitances C g s, C d b, etcetera will go up and that means that, the non dominance pole and zero will move into lower frequencies, so that will affect the speed of the opamp.

If the non dominant pole and zero move within the unity gain frequency, the only way to maintain stability would be to further reduce the unity gain frequency. This we have seen earlier that, if you have larger delay that means, the pole is of lower frequency, the only way to stabilize it, is by slowing by the integrator.

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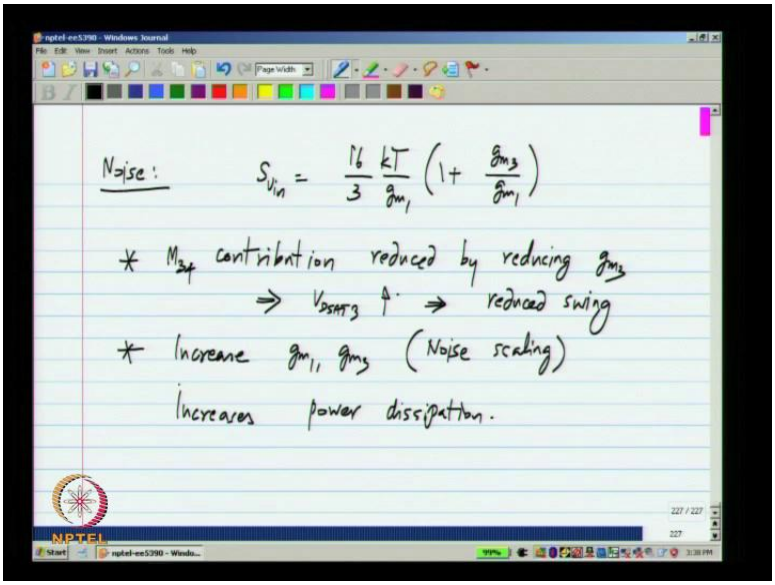

So, again you try to optimize the offset, you will end up with a slower opamp, let us look at noise, you calculated only the thermal noise. The input referred noise is 16 by 3 K T by g m 1 1 plus g m 3 by g m 1, as before you can reduce only the loads contribution by reducing g m 3, which can be done by increasing the V D sat of those transistors, but if you do that, you adversely affect the swing limit.

Now, you can reduce the noise by increasing the g m of all transistors, but if you do that, you will end up with a larger power dissipation. And this is something that we are familiar with, this is basically noise scaling or impedance scaling. If we doubled the widths of all transistors in the circuit, the currents everywhere will double and the g m's will double and the input refer noise spectacle density will go down by factor of 2, when expressed in whole square per hertz, but this will also increase the power dissipation.

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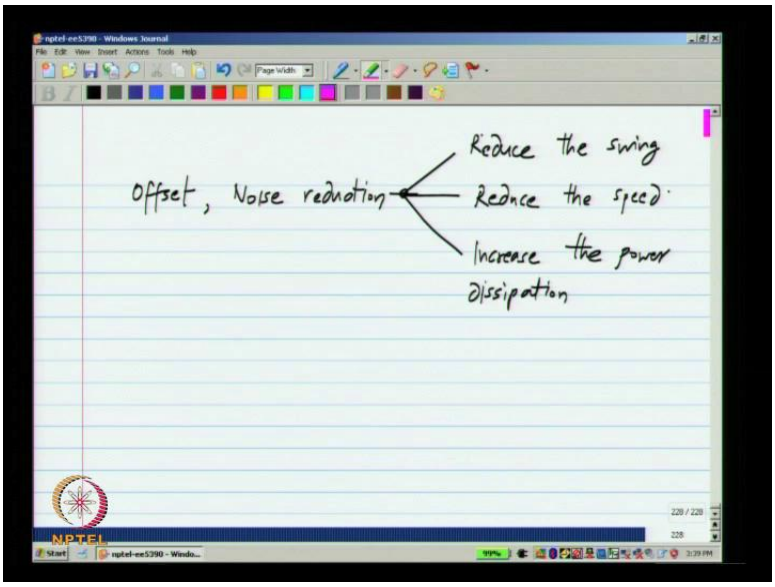

So, we can quickly list the tradeoffs, reducing noise and offset can you do one of few things that, it can reduce the swing, reduce the speed, when you increase the size of the devices. By the way, increasing the size of the devices is also required to reduce 1 over F noise, again that will end up having an adverse effect on speed or increase the power dissipation. And from these, the other tradeoffs can also be worked out, let us say you want to increase the swing, now let us say you are also not allowed to increase the supply voltage.

So, what can you do, you look at the expressions for the swing limits, you see that, it is supply voltage minus M saturation voltages. So, the only way to increase the swing is by reducing the saturation voltages and if you want to keep the same current or the same trans conductance and reduce the saturation voltages, you will have to use larger and larger transistors.

So that means that, you will end up affecting the speed of the device, because parasitic poles and zeros will move to lower frequencies which means that, we have to also move your unity gain frequency to a lower value. So, these are tradeoffs that every analog design are results with, with every circuit practically. So, if you want to optimize everything, you have to do it iteratively, you start with something, now it would not satisfy all the constraints then, you go on optimizing one by one. While trying not to affect anything else, many times that is not possible, so you have to iterate many times to arrive at the final design. We have looked at the characteristics of this opamp, basically we have come up with the data sheet for this opamp. The one thing that we have not yet calculated is the slew rate.

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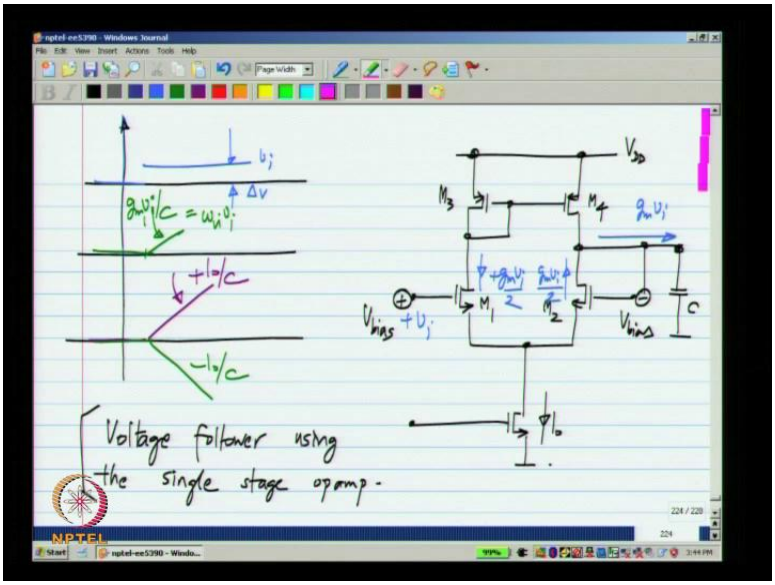

That is, the maximum rate of change of output, that is best illustrated by looking at circuit like this. Let us imagine that, the circuit has reached steady state with V bias at the input and V bias at the output. Now, let us say we apply a small step v i, some small value let me call it delta V, now what happens, the current in M 1 will increase by g m v i

by 2. Remember, as soon as we apply the input step, the capacitors still holds the initial voltage, so this voltage does not change, so it is like applying step v i to the differential pair.

Now, we have a step current of g m v i by 2 in this transistors and g m v i by 2 in the other transistor in the opposite direction, so a total of g m v i plus into the capacitor. So, let us not worry about parasitic effects here, so what happens to the output, it will start rising at a rate g m 1 v i by C. What is this after all, this is equal to the unity gain frequency times v i, this is exactly what we expect from the opamp. If you have an opamp with the unity gain frequency omega u and you apply unit step to it, the slope will be omega u, if you apply the step of v i, the slope will be omega u times v i.

Now, let us say, you go on increasing the magnitude of v i, I will keep applying larger and largest steps. What happens is, the current in this increases by larger and larger amount and the current their decreases by larger and larger amount. But, soon you will reach a point, where the step value is greater than the saturation voltage of the differential pair. We calculated that as the over drive required for M 1 to carry the current i naught, there is some voltage beyond which all of this I naught flows through M 1 and nothing flows through M 2.

And if you increase the step size beyond that value, nothing further happens, all of I naught will flow through M 1 and nothing will flow through M 2. So, what will be the current through the capacitor, I naught is flowing here, it will get mirrored into M 4 and flows into the capacitor. So, there is maximum rate of change of the output and that is equal to plus I naught by C when you apply a positive step. In this particular circuit, when you apply a negative step, the current in M 1 will reduce.

Again if you apply very large negative step, the current in M 1 becomes 0 and in M 2, it will become I naught and that will be drawn out of the capacitor. So, the maximum rate of change in the negative direction is also the same value, it will be minus I naught by C. Now, this may or may not be true in general, it could be that on the positive side, the maximum rate of change of the output is different from that on the negative side that is, the slew rates on the positive and negative sites are different. But, in this opamp, they happen to be the same and they are equal to I naught by C.

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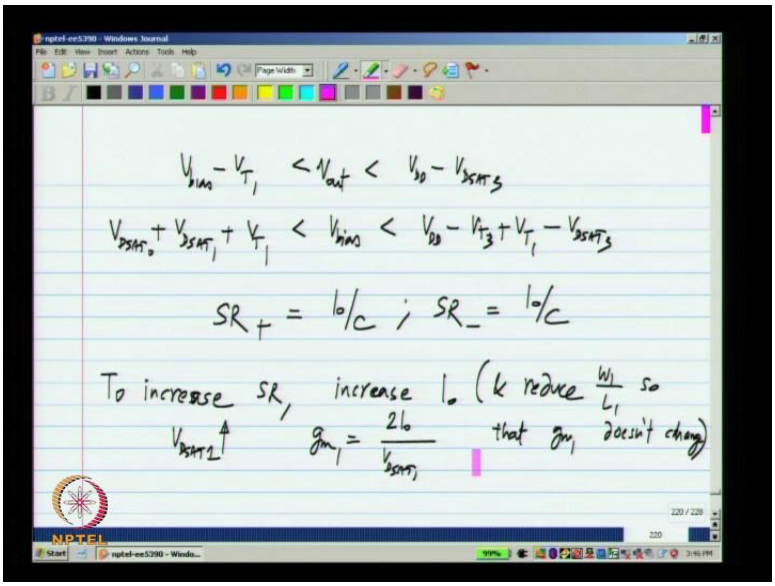

So, just to complete the data sheet, we will have positive and negative slew rates also and they are equal to I naught by C. Now, again you can illustrate the tradeoffs with this, let us say you want to increase the slew rate, but you do not want to affect any other parameter of the opamp like the unity gain frequency. So, what should you do, clearly the slew rate is affected only by current I naught, so you have to increase the current I naught.

But, if you do that, the trans conductance and those thing change, so you have to reduce the W by L ratio of M 1 and M 2 so that, g m 1 will reduce and retain it is original value. In other words, you have to increase V D sat 1, because after all g m 1 is 2 I naught by V D sat 1, we want to increase I naught while keeping g m 1 the same, V D sat 1 has to increase. So, if you do this, again you will see that, the swing limit reduces, it is in direct conflict with the swing limit.

So, as usual, you see some tradeoffs, now in general you see that, also if you want to work at higher and higher speeds, we would operate the transistors at higher and higher saturation voltages that is, higher and higher values of V g s minus V T. So, this we saw from the formula for the transit frequency of the transistor. Now, that frequency in absolute terms does not mean anything, but it was directly proportional to V g s minus V T and that is what we see here as well.

So, if you want the high slew rate, if you want the maximum rate of a output, maximum rate of change of the output to be very large, you have to operate with a large V D sat. And if you want the low power operation, what you have to do is, to have small current and very large transistors, this will increase the parasitic capacitances. So, in the small signal picture, the non dominant poles and zeros move to lower frequencies, it will slow down the circuit.

And also when you have a large transistors with a small current, you have a small V g s minus V T so that means that, the slew rate is small as well. So, the constraints for high speed and low power are opposite to each other, generally high speed demands higher power and lower power will constrain you to lower speeds. We have a single stage opamp, it works, first of all it has some limitations that we already knew when we discuss opamp at the level of the control sources. You cannot operate this with resistive loads, because that will limit the dc gain and increase the steady state error, that is one problem and also dc gain itself is limited. So, the dc gain that we get from this is g m 1 by g d s 1 plus g d s 3 and that has the limited value, that is like the gain of a single transistor.

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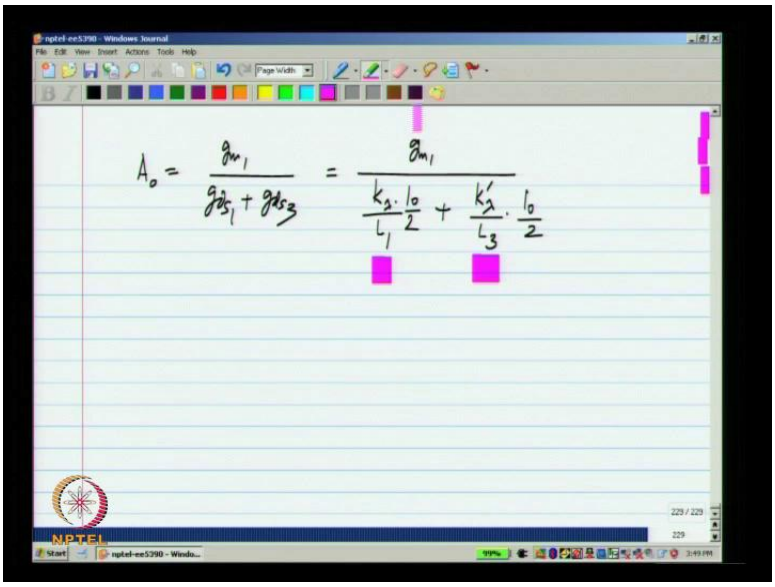

Now, how would you improve that, g m 1 divide by, we know that g d s 1 is lambda 1 times I naught by 2 and lambda 1 itself is proportional to some constant and inversely proportional to the length of M 1 and M 2. And similarly, g d s 3 has a different K

lambda, because it is PMOS transistor, I will call it K lambda prime divided by L 3 times I naught by 2. So, as a designer, you have freedom only over L 1 and L 3, again I am assuming that, you will not change g m 1.

Because, you do not want to change the unity gain frequency of the opamp, you want to keep everything the same, but you tried to increase only the dc gain. The only way to do that, is to increase the length of the transistor, which inherently gives you higher output resistance. That make sense, because we know that, the finite output resistance r d s is a result of channel length modulation. So, if you increase the length of the transistor, the channel length modulation will be a smaller fraction of the total length and the effect will be reduced.

Now, this will also require that, to increase the width so that, your g m's remain the same, so over all you will end up increasing the size of the transistors and this again affects the speed. So, you can increase the gain by a small amount using this technique of using a longer transistor, but let us say, you want the gain of 100 times what you have, you cannot do this realistically. Because, L 1 increases by so much, first of all the area becomes so large and the circuit will slow down so much, that it is useless. We have to find other ways of doing that, so that is what, we are going to discuss now.

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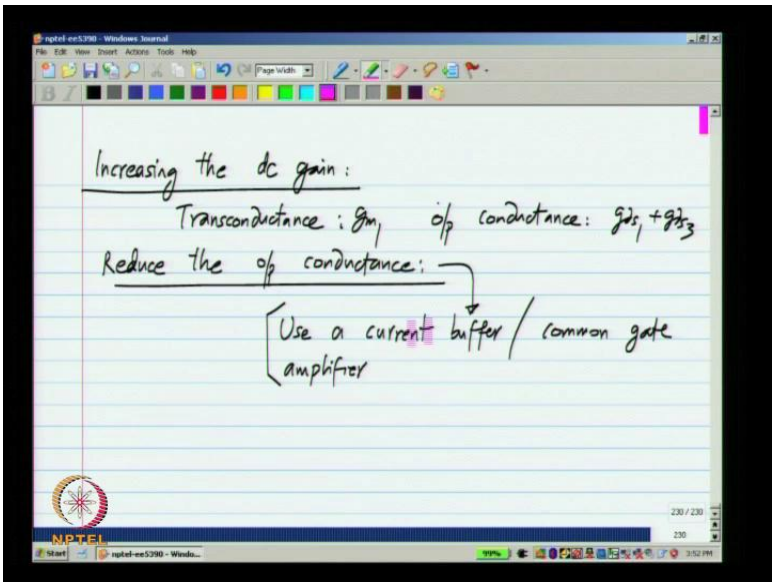

Now, first of all, why is the dc gain limited, we have a trans conductance g m 1 and an output conductance g d s 1 plus g d s 3, what we have is a voltage control current source

with this trans conductance and that output conductance. So, the way of increasing the dc gain is to reduce the output conductance, so this is one of the ways of doing that or increase the output resistance. How do we do this, we know that, if you have a current source of a given output resistance, you can improve it is quality by using a current buffer after that.

So, that is using a current buffer or a common gate amplifier or we can try to do the same, so we can use this to try and increase the gain of our circuit. And we also know that, the output conductance is a combination of the output conductance contributed by the differential pair and the output conductance contributed by the current mirror load. So, each of these looks like a current source, a current mirror looks like a current source, so we have to use a current buffer for that and differential pair also looks like incremental current source and we have to use a current buffer for that as well. Now, we are already familiar with this circuit that is, we are already familiar with the common gate amplifier, all we have to do is, to apply it in the right way to our opamp.

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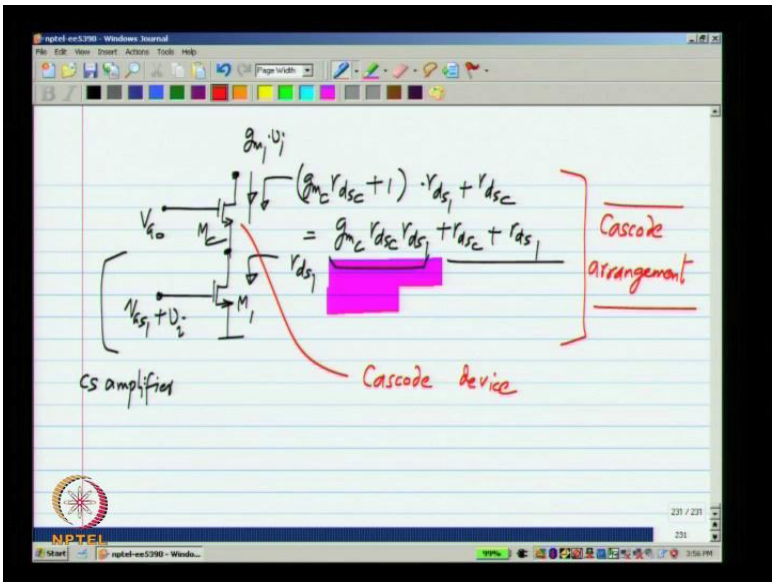

So, first let me discuss the output resistance of a single transistor, let us say it is biased with some voltage V g s 1, let me call this M 1. So, looking in here, I have resistance r d s 1 or a conductance g d s 1 and let us say, I use a common gate amplifier on top of this one. So, the lower one, I could think of as common source amplifier if I was going to

apply an increment v i over there. It would give me a current g m 1 times v i and that I could push into load resistance or wherever I want to.

Now, on top of that, I use a current buffer, so the current that appears here, the incremental current is still g m 1 times v i`. But, looking into this, what I have is, an output resistance of g m c, r d s c, let me call this m c, g m c r d s c plus 1 times r d s 1 plus r d s c. Basically, the sum of the output resistances of the two transistors plus g m c r d s c r d s 1. Now, these are negligible compare to this, this is the dominant contributor to the output resistance and that increases the output resistance by an order of magnitude or even more.

Because, we had r d s 1 and that is boosted up by a factor g m c times r d s c, which could be as high as 50 or 100 even. So, this is a very easy way of increasing the output conductance and making it a better current source. When we had a single transistor, it was an incremental current source of value g m 1 v i and when we have this transistor M C on top of it, it is also an incremental current source of value g m 1 V i, but it has a much higher output resistance.

So, this is a very common technique to improve the output resistance of a current sources, this device is called the cascade device and this combination is known as the cascade arrangement. So, we will use this for both the differential pair and the current mirror in the next lecture to come up with the opamp, which has the much higher dc gain.

Thank you, I will see you in the next lecture.