Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture No - 31
Single Stage Opamp Characteristics

Hello and welcome to lecture 31 of Analog Integrated Circuit Design. In the previous class, we analyze the differential pair loaded by current mirror active load in great detail. We saw how to analyze it conveniently and that was by terminating it with a voltage source so that, we see small impedances as loads and then, calculating the trans impedance or trans conductance of the differential pair.

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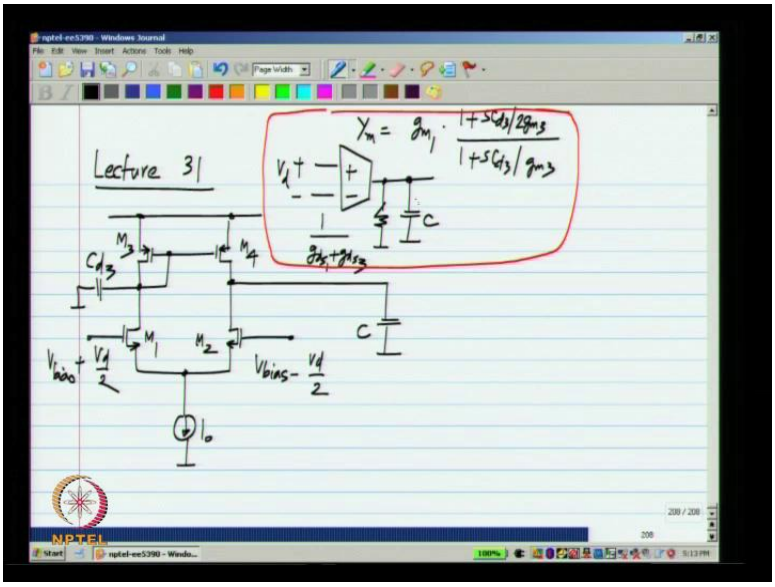

We have purely differential input and this is loaded by a capacitor, we have really only one parasitic capacitance of consequence, because the tail node incrementally is not swinging, it has a tail node incremental 0. So, we have only the C d 3, which consist of parasitic capacitances from all the transistors connected to that node. Now, under this conditions we saw that, we could model the entire opamp with a trans admittance Y m, which was g m 1 times 1 plus S C d 3 by 2 g m 3 divided by 1 plus S C d 3 by z m 3. It also has an output resistance, which is equal to 1 over g d s 1 plus g d s 3, so this is the model corresponding to this opamp. So, it has parasitic pole and zero in addition to the pole at origin or close to the origin due to the integrating capacitor.

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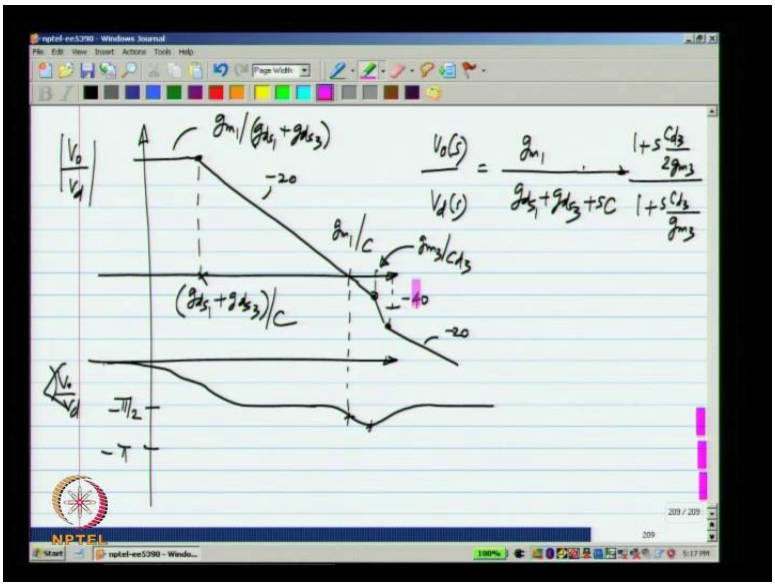

So, when we have such frequency response, what will the magnitude on phase look like, this is the transfer function from the difference input V d of the opamp to the output voltage V o. Now, this is a relevant thing, as we have used it in various loop gain calculations and stability considerations. So, the magnitude of the voltage gain will be g m 1 by g d s 1 plus g d s 3 at dc or low frequencies, the dominant pole will be at g d s 1 plus g d s 3 divided by C.

Now, this would be at the origin or 0 if g d s 1 and g d s 3 are 0 then, it follows an integrating type of behavior, it has a slope of minus 20 dB per decade. Let me assume that, the parasitic pole and zero occur beyond the unity gain frequency of the opamp, the unity gain frequency is given by g m 1 by C. Please remember that, with the parasitic pole and so on, the point where the magnitude plot crosses unity is not exactly g m 1 by C. But, if we assume that the parasitic effects happened beyond this as we usually need for stability, the unity gain frequency can be assumed to be g m 1 by C.

There is the another pole at g m 3 by C d 3, so the slope changes to the minus 40 dB per decade and then, at twice that frequency, there will be 0 and it changes back to minus 20, that is what the magnitude respond look like. And the phase response, angle of V naught and V d will start from small phase lags and go to minus 90 degrees. And here, because of the pole, it will dip down below minus 90 and because of the zero, it will come back up and then finally, settle to minus 90.

You can calculate the maximum phase lag that occurs, because the zero frequency is at twice the pole frequency, this is at minus pi by 2 and this is at minus pi, the phase never reaches minus pi really. Now, for stability, it would be best if you have the parasitic pole and zero beyond the unity gain frequency, assuming that the opamp is in unity feedback. Otherwise of course, you look at the unity looping frequency of, whatever feedback loop that you have, instead of the unity gain frequency.

So, this is the frequency response of the single stage opamp, it is very simple and it is unconditionally stable, because the phase lag never reaches minus 180 degrees. So, we have evaluated the gain of the opamp and the frequency response of the opamp and from this of course, we can ascertain the stability. What we still have to do, is to calculate other characteristic like the large signal limits of the opamp as well as non ideal features like the noise and offset of the opamp.

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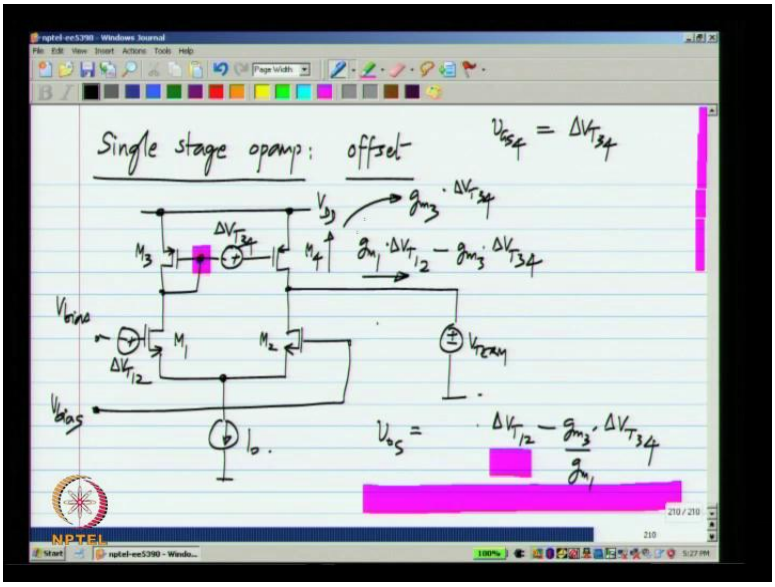

So, let us calculate the offset of the opamp, now the transistors M 1 and M 2 are supposed to be identical to each other and M 3 and M 4 are supposed to be identical to each other, but there will be mismatch between them. So, we have to add appropriate sources to the circuit that represent the mismatch, find the output and from there, calculate the offset. The input referred offset is the useful representation of the offset in an opamp that is, the input voltage for which the output will be 0.

Now, as before while calculating the dc gain and so on, what we did was, we did not calculate the output voltage directly, we calculated the output current going into a voltage source, multiplied that by whatever impedances connected to the output to get the voltage. Similarly, here what we will do is, calculate the output current knowing into a voltage source, because that is lot easier to do than calculating the output voltage. Now, because these offsets will be not necessarily symmetrically injected into the circuit, the circuit analysis will become very complicated.

So, usually while calculating the offsets and so on, we will assume that, the g d s values are very small. Now, they would not affect the answer very much, but will give you, will simplify the analysis sufficiently so that, we do not get bogged down with details. So, what I will also do to further simplify the calculations are demonstrated here, is that, I will assume that, there is only a threshold voltage mismatch between MOS transistors, we very well know that, there is threshold voltage as well as current factor mismatch.

As an exercise, you please add the current factor mismatches, it is not very difficult, all you have to do is, if you have a pair of identical transistors, to one of them, you add current source in parallel, that represents the mismatch. Now, if the inputs are identical and we have this the terminating voltage, which is equal to V D D minus V s d 3, the current here is 0. Because of mismatch between transistors, it will be non zero so that means that, if I have a tans conductor with offset, if I apply 0 volts here, I will have some current there, which I call offset current.

I want to represent this as an equivalent input voltage and that will simply be equal to i o s divided by g m. Clearly you see that, if I apply 0 volts here, i o s by g m is applied to the trans conductor and the output current will be i o s. So, as before I will first calculate this current divided by the trans conductance of the circuit to get the input referred offset. So, first of all, I will have two mismatches, one between M 3 and M 4, and one between M 1 and M 2.

To represent the offset between M 1 and M 2, mismatch between M 1 and M 2, I can represent the threshold voltage mismatch as a voltage source in series with the gate. So, we already did this earlier in the exercise involving the current mirror, the threshold voltage mismatch, any change in the threshold voltage can be represented as equivalently a change in the gate source voltage. So, the mismatch threshold voltage between M 1 and

M 2, I will represent equivalently as a mismatch in the gate source voltage between M 1 M 2.

In other words, a series voltage source with the gate of M 1, let me call that delta V T 1 2, as with noise, the polarity of this is not important, because we know that, it is a random quantity. Finally, what we will calculate will be the standard deviation or the variance of this quantity. Now, what is the output current due to this voltage source is very easy, you can see that, delta V T is simply the differential input voltage to the opamp.

So, this is where we normally would apply the differential input between V d, so the output current is simply g m 1 times delta V T 1 2, the trans conductance times the delta V T 1 2. Now, this is a very common feature, usually you have the input signal applied to some transistors, any offset due to the input transistors will directly affect the circuit. This will be more obvious when we calculate the input referred offset, but it also clear from this example, the offset between M 1 and M 2 appears directly as an input signal to the circuit.

Now, I also have to calculate the effect of offset between M 3 and M 4, as with noise, the affect each of these is very small, these are small signals and we simply add up the results. Now, for this analysis, delta V T 1 2, 0 of course, so we would not have this, now because these are at 0 and we assume that, the transistors do not have any g d s and so on. So, the currents M 1 and M 2 will also be 0, because of that, the incremental voltage here will be 0, again you can conform this with analysis, if you wish.

So, the gate source voltage of M 4, the small signal gate source voltage of M 4 will be delta V T 3 4. So, the incremental current in M 4 will be g m 3, which is the same as g m 4 times delta V T 3 4 and that will go into the terminating voltage source. So, the total output current will be some simply del g m 1 times delta V T 1 2 minus g m 3 minus delta V T 3 4. This minus sign is simply, because of the way we have chosen the polarity, it is of no significant, whatsoever and we put in both mismatches, that is the current that we are going to have it the output.

So, the offset current is g m 1 times delta V T 1 2 minus g m 3 times delta V T 3 4, as I explained before, we would like to represent this as an input referred offset voltage and that is nothing, but, i o s divided by g m 1. So, V o s will be delta V T 1 2 minus g m 3

by g m 1 delta V T 3 4, this is what I meant by the offset of the input differential pair appears directly as input offset. Now, this is in general true of offset and noise, you apply the input directly to some devices and the offset or noise of the devices directly appears in the input referred offset or noise.

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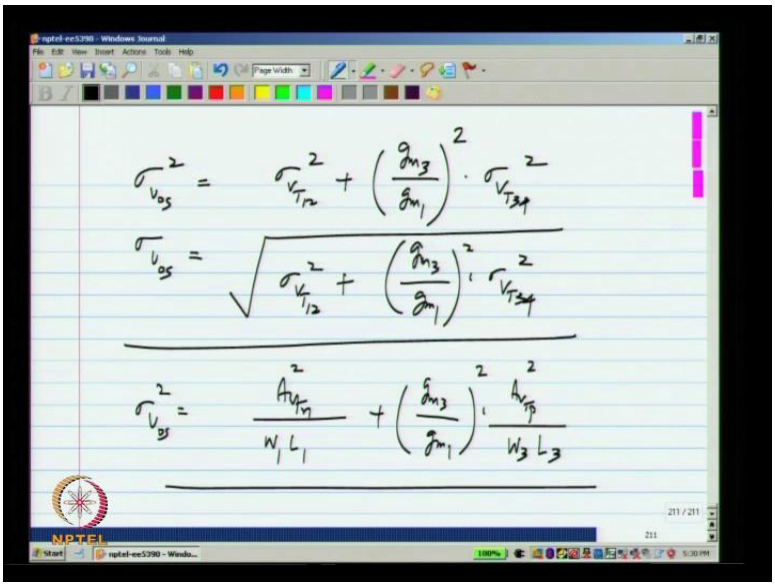

Now, as usual, I am not interested in the exact value of offset for each device, what I really want is, the mean square value of the offset or the standard deviation of the offset. Mean square of the offset is nothing but, let me represent it as sigma V o s square, sigma V T 1 2 square plus ratio g m 3 by g m 1 square times sigma V T 3 4 square and sigma V o s is nothing but, the square root of this whole thing. The effect of M 1 and M 2 is simply cannot avoid and effect of M 3 and M 4, the offset between them is multiplied by the ratio g m 3 by g m 1.

And if you have small g m 3 and large g m 1, it will be divided by a large number and will be negligible. Now, the way to think about this is that, the input transistors M 1 and M 2 convert the input voltage to a current. Now, the low transistors M 3 and M 4 will add an offset current of their own, which is proportional to g m 3 times delta V T 3 4, when referred to the input, that will get divided by g m one. So, if you make the offset current added by the load devices small and trans conductance of the input devices large, the effective offset due to the load at the input will be small.

So, there is some room to play as far as the offset of the load is concerned, as far as the offset to input is concerned, there is nothing you can do, it appears directly at the input. The only way to reduce that, is to increase the array of the devices, so while making the input devices bigger and bigger, you can reduce the offset. And if you want to make the overall offset small, you have to make both the input devices large and the load devices large.

And this can be further calculated from the process data, here it is A V T square by W 1 L 1. By the way, this is the A V T of the NMOS transistors, which could be different from the A V T of the PMOS transistors. So, with this, you can calculate the standard deviation or variants of the input offset, what it really means is, let us say this sigma V o s is comes out to be 2 millivolts.

So, if you make a million opamps like this and then, measure all their offsets, 99 percent of them will have an offsets less than 3 millivolts that is, plus minus 3 milli volts. So, from this and a kind of guarantee that you want that, the offset be less than a certain a value. You can figure out, how much sigma V o s you have to design for and whether the opamp sizes that you have chosen, the transistor that you have chosen are adequate or not.

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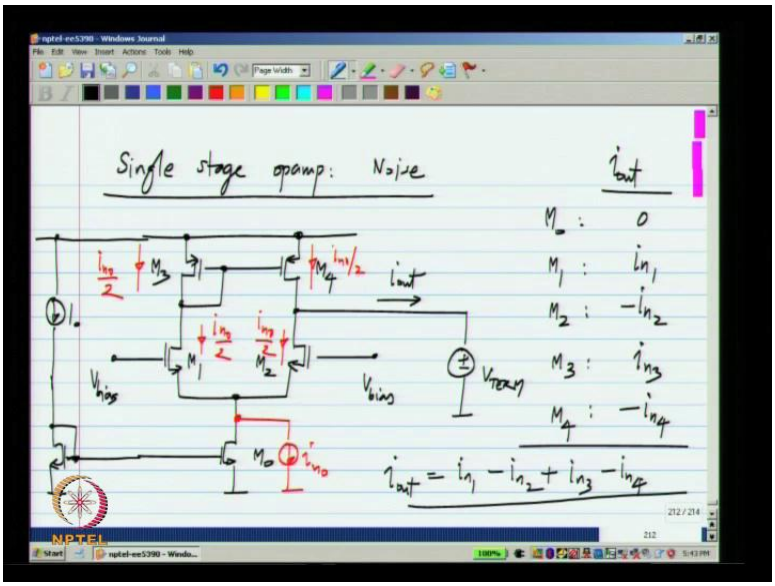

Now, the next thing to be calculated is the noise, so we will again finally calculate the input referred noise of the circuit. As before, we will calculate the output current going

into a terminating source V term, as with offset, we will calculate the output current and from that, calculate the input referred noise. We know that, the equivalent input referred noise will be the output noise current divided by the g m. In earlier examples, we were calculating the output noise voltage, but it is exactly the same here, we calculate the current instead and divided by g m 1 to get the input referred noise voltage.

As we mentioned earlier, the input referred noise voltage is an equivalent representation, it is not a noise voltage that appears anywhere in the circuit, but it something that will represent the effect of all noise sources in the circuit. Now, as with offset calculations, we will by enlarge ignore g d s in the calculations, because that only lead to more cumbersome expression without any extra inside and usually it also does not quantitatively affect the results very much.

So, what should we do when calculating the noise, we have to add noise to each transistor, every noise generating device. In this case, we have only transistors and we have to find out the transfer function from every noise source to the output. And finally, add up all of them in an uncorrelated way to get the output noise spectral density divided that by g m 1 square to get the input referred noise spectral density. I also have to add the current source transistors here, M naught and the current mirror, let us assume that, this is bias from a current mirror.

So, first in cohesion condition of course, i out is 0 and let me add i current i n 0, that is due to M 0. Now, if have current i n 0 due to M 0, there will be an incremental current in both M 1 and M 2. There will be no incremental current in M 0, because it is output conductance is 0, there will be an incremental current in both M 1 and M 2. And how much will that be, we know that, the impedance looking up here is 1 over g m 1, because the drain is loaded by a relatively low resistance.

The impedance looking up here is also 1 over g m 1, because it is drain is loaded by a short circuit, which is also a small resistance. So, this current divides equally and we have i n 0 by 2 and i n 0 by 2, now i n 0 by 2 in M 1 goes through M 3 and gets mirror than M 4. So, we have i n 0 by 2 and i n 0 by 2 over that, so what is i out, we have an i n 0 by 2 here and i n 0 by 2 there, so i out due to i n 0 that is, the noise current in M 0 is 0.

Now, this is general result, if you inject something into the common mode node or the tail node of an opamp, now in the difference output, the effect will be 0. Because, it will

get symmetrically divided into M 1 and M 2 and mirrored in M 3 and M 4 and the net effect will be 0. So, the noise of the current source transistor does not appear in the output of the opamp.

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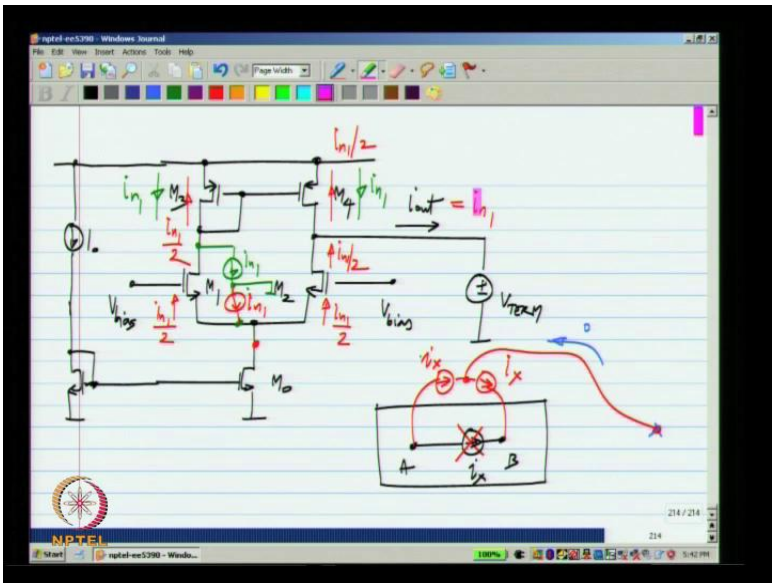

Let me copy this over, let me now calculate the noise due to M 3 and M 4, this represent the noise due to M 4 and in small signal, this is grounded and this point is also at 0, because of this constant voltage source. So, all of these current source simply goes into i out, so the effect of noise current due to M 4. Let me tabulate all the transistor here, will be that, all of i n 4 appears at i out with the polarity I have chosen, it happens to be minus i n 4.

If I look at the noise current due to M n 3 what happens, the impedance here is infinite, will assume the g d s of these transistors is 0. So, this i n 3 simply is drawn out of the diode connected transistor M 3 and we know that, M 3 and M 4 form a current mirror. So, the same current appears here as well and it has to go into the terminating voltage source, because that has 0 impedance, so i n 3 also appears directly at the output. We then have to calculate the effect of noise currents in M 1 and M 2, let us say I consider the noise current in M 1.

Now, the earlier noise sources had one of the terminals grounded, now this is connected between two nodes, the drain and source of M 1. The analysis can be little more complicated, it is not very difficult, but it can be little more cumbersome, but it is a very

need trick that makes it very easy. In any circuit, let us say I have a current source between A and B, I can replace that with the series combination of two current sources of exactly the same value.

So, let us me call this I X, this will be I X and that will also be I X, clearly KCL is satisfied here and also nothing has changed the nodes in A and B, so this is fine. Now, if I take this node and connect to any other node, again it will not affect the circuit, because these two currents are, by definition identical and the current flowing here will be 0. So, I could connect it to any other node without affecting KCL at that node and consequently, without affecting the circuit.

Now, this is a particularly convenient thing, when we have to do analysis with floating current sources that is, current sources connected would be in two nodes, neither of which is ground. In many cases, it will simplify things if we replace it as a series combination of the two current sources and connect the middle node to ground. So, that is what we are going to do here, most important thing is that, the two current sources should be identical.

And in this case, they are noise sources, but the noises are identical, now normally you are used to calculating noise from different sources and assuming they are uncorrelated. In this case, they are perfectly correlated, because we are simply replicating the current and we will connect the middle to ground and we will analyze the two separately. Now, we do not have to do further analysis, because this i n 1 is like the previous analysis we did with noise current source of M 3.

And the lower i n 1 is like the analysis we did with noise current of M 0, so let me put them on different colors just for clarity, i n 1. What will happen due to the upper i n 1, all of it will flow into M 3 and get mirrored into M 4. And what will happen due to the lower i n 1, it will split into i n 1 by 2 and i n 1 by 2 exactly as we discuss for the noise from M 0 and whatever goes through M 1, also goes through M 3 and gets mirrored. So, we have a net current of i n by 2 in M 4 and i n by 2 in M 2, so the total current flowing out will be equal to i n 1.

So, it turns out that, all of the noise current of M 1 appears at the output, it takes some complicated path, half of it goes through M 3 and M 4, and half of it through M 2, but it will come out entirely. Now, in a very similar way, the noise of M 2 can be analyzed and

it turns out that, exactly the same thing happens and all of the noise of M 2 will also appear at the output.

So, you can do the analysis just as a practice of this kind of analysis, all of i n will appear there and if you do this with polarity downwards, this will turn out to be i n minus i n 2. So, the output current will be the sum of noise of all these devices and the tail device does not contribute anything, it will contribute equal currents to the two halves and they get cancel out.

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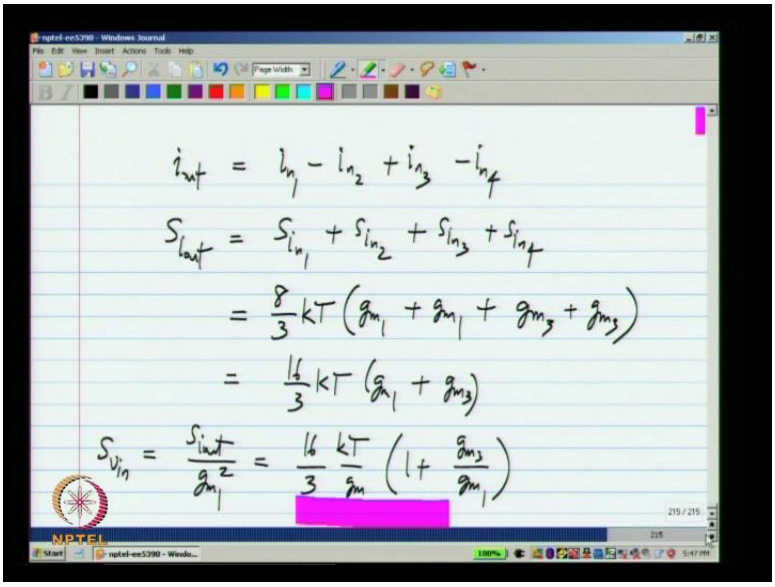

Let me rewrite it here, so the noise spectral density which is what I am interested in, is the sum of the spectral densities, because these terms are uncorrelated from each other, which is i n 1 and i n 2 are proportional to g m 1, i n 3 and i n 4 are proportional to g m 3. So, this is 16 by 3 K T g m 1 plus g m 3 and the input referred noise voltage source is nothing, but S i out divided by g m 1 square, because an output current can be represented by an equivalent input voltage by dividing i out by g m 1.

So, this is equal to 16 by 3 K T 1 over g m 1 plus g m 3 by g m 1 square, which can be rewritten as 16 by 3 K T by g m 1 1 plus g m 3 by g m 1, so that is the expression for the input voltage noise spectral density. Now, we have ignored the frequency dependence and so on, that is not so important with noise and also it lead to machine cumbersome expressions. If you do want to calculate the frequency dependence of this input and

output noise spectral densities, you go to a simulator, but this expression is good enough for us for wide variety of calculations to estimate the noise.

One thing to observe here is that, the first part of this expression is 16 by 3 K T by g m, now we know that, if we refer the noise of the MOSFET to it is input, it will be 8 by 3 K T divided by g m. That is, if we represent the noise as a noise in V g s instead of i d, it will be eight third K T divided by g m and we have two transistors, which have uncorrelated noise. So, their spectral density is add up and we end up having 16 by 3 K T divided by g m 1.

So, as I mention many times, the noise from the input transistors contribute directly to the input referred noise. Now, the second part of this is the contribution of the low transistors, just as an offset you see that, you have the expression g m 3 by g m 1 appearing there. By making the trans conductance of the load much smaller than the trans conductance of the input transistors, we can reduce the noise contribution of the load.

But, the noise contribution of the input transistors does appear directly and the only way to reduce that, is to increase g m 3. And we know that, increasing g m 3 will contribute to increase for dissipation, because we have to have more current in the transistor. So, we have calculated in detail the small signal parameters of the opamp, the dc and ac gains and frequency response and so on and also the offset and noise, what is left is to calculate the large signal limits.

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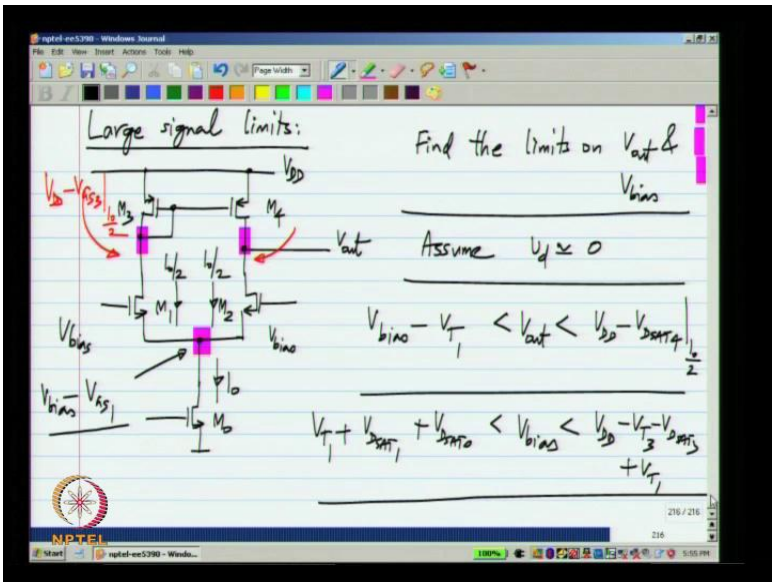

I will show the transistor here, because that is relevant to this analysis, let me call it M 0 M 1 M 2 M 3 M 4. Now, we have several things going on here, we have the input V bias and difference voltage V d and the output. Now, when the opamp is operating in a negative feedback circuit, the difference voltage V d is expected to be very small, so that is the basic idea behind using an opamp in the first place. So, what we will do is, assume that, the V d is usually so small, that it will not drive any transistor into the triode region.

So, we will not directly affect the swing limit, what will happen is that, it will affect the output and the output voltage will be limited. It is not the swing of the input voltage V d that will push any transistor into triode region, but it is the output swing that may push some transistors into triode region, so that is one thing. And secondly, this V bias so far we have not defined it, in an opamp itself we can have a different values of V bias, we will come to it when we talk about single supply and dual supply operation of opamps.

But, so far we are simply assume that, V biases are the, all transistors are in saturation, so we have to find out the limits of V bias, for which that is indeed the case that is, the transistors are in saturation. So, what we have to do, is to find the limits on V out and V bias, we will assume that, V d is 0, so I will remove V d from this picture. Now, what happens if V out increases, if V out goes on increasing, the transistor M 4 will get squeezed that is, it is V d s will reduce and that can go into the triode region.

And when will that happen, let us assume a supply voltage of V D D, so V out has to be utmost V D D minus V D sat of M 4, which is as same as V D sat of M 3. And we will assume that, this saturation voltages are calculated at the quotient operating point, by the way this definition of V D sat, I am assuming that you are familiar with. V D sat is nothing but, square root 2 i d by mu C ox W by L of the respective to transistors, this is the gate over drive or the V d s that is required for saturation.

So, V D sat 4 and we will calculate it at a current of i naught by 2 and in this particular case, this will be 2 times i naught by 2 and what we have here is, W 3 by L 3, that is the same as W 4 by L 4. Now, on the other hand, what happens if V out starts decreasing, as V out decreases you can see that, the gate of M 2 is at this voltage V bias. So, as V out reduces, M 2 will go further and further into the triode region, the output voltage V out can go below V bias, but not more than 1 V T.

So, I call this as V T 1, which is the threshold voltage of M MOS transistor and V T 2 of course, is same as V T 1, so these are the limits on V out, we yet also find the limits on V bias. Now, earlier we argued that by symmetry, this output voltage will be exactly equal to the drain voltage here, when no current is flowing out. So, that is the case that we will assume, we will assume no current is flowing out of here, in reality of course, we will have our capacitors connected here and then, some feedback network and so on.

For now, we will assume that, no current is flowing over there and that is true independently of the value of V bias. The current here will be i naught and the current there will be i naught by 2 and i naught by 2. So, what is happen is, as V bias changes, the current in M 3 and M 4 will be exactly the same and the voltage here and here will not change, we will assume that, the g d s of these transistors are very small. What will changes this voltage, that voltage will be V bias minus V g s of M 1 or M 2, I will write V g s 1 here, so the tail nodes simply follows V bias.

So, as V bias come to very small values, the transistor M 0 goes into the triode region, it is V d s becomes smaller than it is V g s minus V t, so it goes into triode region and that will limit the lower value of V bias. So, V bias has to be greater than 1 plus V D sat 0 and V g s 1 itself can be written as the threshold voltage V T 1 plus V D sat 1. So, what is important here are the ranges, so V T 1 the threshold voltage plus 2 overdrain voltages above ground that is, the lower limit on V bias.

What happens if V bias goes on increasing, as we said the drain of M 1 and M 2 do not change, they will be at a fixed value equal to V D D minus V g s of M 3 at a current of i naught by 2. These voltages will be V D D minus V g s 3 at a current of i naught by 2, the same holds here as well. So, the drain as a fixed voltage, the gate voltage is increasing for M 1 and M 2, so M 1 and M 2 will go into triode region, if the gate voltage increases beyond the drain voltage by more than 1 V T. So, V bias has to be less than the drain voltage V D D minus V g s 3, which I will write as V D D minus V T 3 minus V D sat 3 plus V T 1, so these are the limits on V bias.

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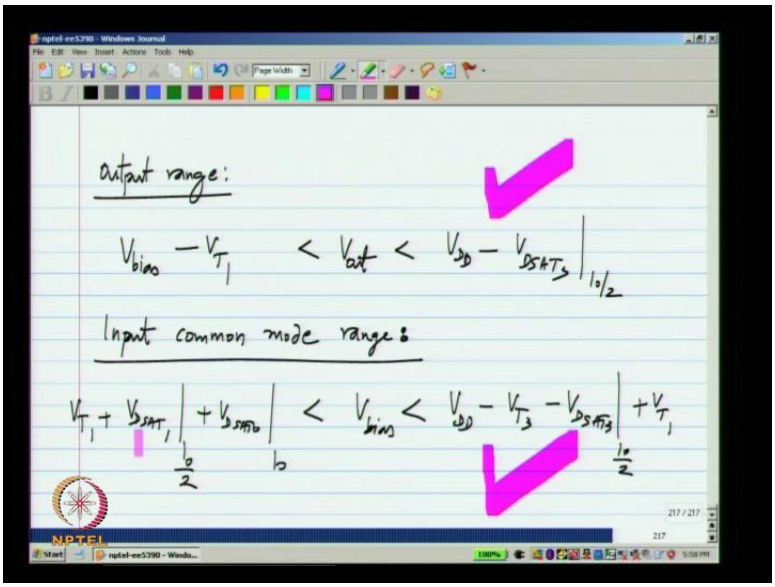

So, let me rewrite them here, the output range is given by that and the input bias range or the input common mode range, V bias is nothing but, the average value of inputs. So, input common mode range is given by that on the upper side and on the lower side, V D sat 1 at a current of i naught by 2 and V D sat 0 of a transistor M 0 at a current of i naught, so these are the ranges.

Now, of course these will give you some numbers if you calculate, but what you should particularly observe is that, the output voltage can go fairly close to V D D. The normal range of saturation voltages are may be 100 to 200 millivolts, especially in modern low voltage technologies. So, it can go close to V D D of course, not exactly equal to V D D, but within 100 or 200 millivolts of V D D. So, on upper side, the limit is quite good, but on the lower side, it depends on V bias.

So, if V bias happens to be half of the supply voltage, so this can go only a little bit below half of the supply voltage, so this is good and other one is not so good. And as far as the input common mode ranges concerned, again on the upper side, the limit is fairly close to V D D. If you assume that, the threshold voltage of NMOS and PMOS transistors is the same then, V T 3 approximately equal to V T 1 and that will cancel out. You see that, the upper limit is within one saturation voltage of V D D that is, V D D minus V D sat 3. So, again on the upper side, the input range is good, but on the lower side, it is limited to quite a bit above the rail, quite a bit above the lower supply rail, which 0 volts. So, it is equal to the threshold voltage plus the sum of V D sat 1 and V D sat 0.

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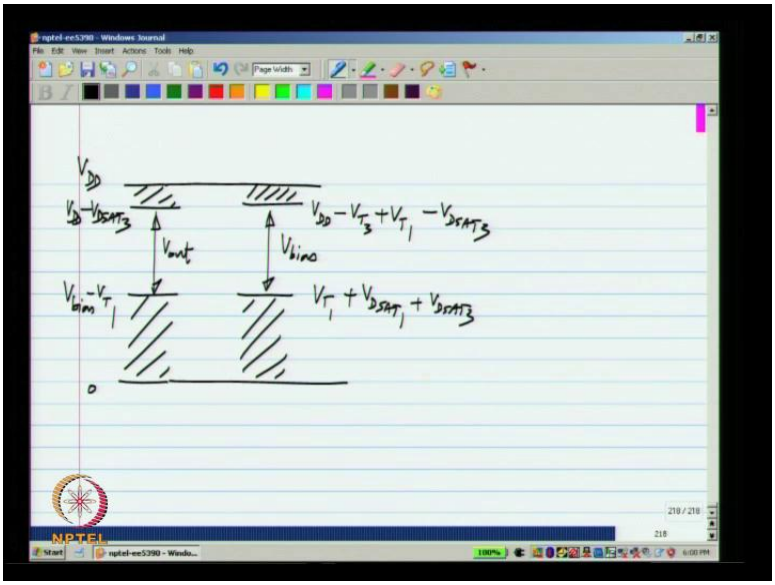

What I mean is that, we have 0 and V D D, which represent the lower and upper rails, the output voltage can go fairly close to V D D, I will represent the by this line. And on the lower side, it is limited by V bias, it has to be within this region that is, the range for V out. And V bias itself can go fairly close to V D D that is, V D D minus V T 3 plus V T 1 minus V D sat 3, it is similar to the upper limit on V out.

But, on the lower side, it is limited by V T 1 plus V D sat 1 plus V D sat 3, that is very obvious from the expressions that, this gap is lot more than gap, so that is the range for V bias. So, with the particular topology that we have chosen, limits are closer to V D D than to ground. Now, this is a property, this is a feature of having chosen NMOS

differential pair input transistors and PMOS load. If we choose PMOS input transistors and an NMOS load, the situation would be reversed, you could go lot closer to the lower rail and you could only go lot farther from the upper rail.

So, these are also some considerations, which will enable you to choose between NMOS and PMOS transistors. If you want an input common mode range very close to the lower rail, you have to use PMOS transistors. If you want input common mode range close to the upper rail, you have to use NMOS transistors. So, these are the large signal limits of the opamp, now we will elaborate a little bit further on this when we discuss single and dual supply operations of the opamp in the next class.

Thank you.