Analog Integrated Circuit Design
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Lecture No - 30
Differential Pair with Current Mirror Load

Hello and welcome to lecture 30 of Analog Integrated Circuit Design. In the previous lecture, we looked at the differential pair with active load, current mirror load as a possible candidate for realizing opamp. Now this circuit is asymmetrical and we have to be a little careful in analysis it is details; first we looked at the quiescent operating point and saw that operating point itself is symmetric, because of the symmetry of the transistor parameters the transistor widths and lengths. Today, what we will do is to analyze the small signal characteristics of this, that is we want to calculate the trans conductance or the voltage gain and output resistance and so on.

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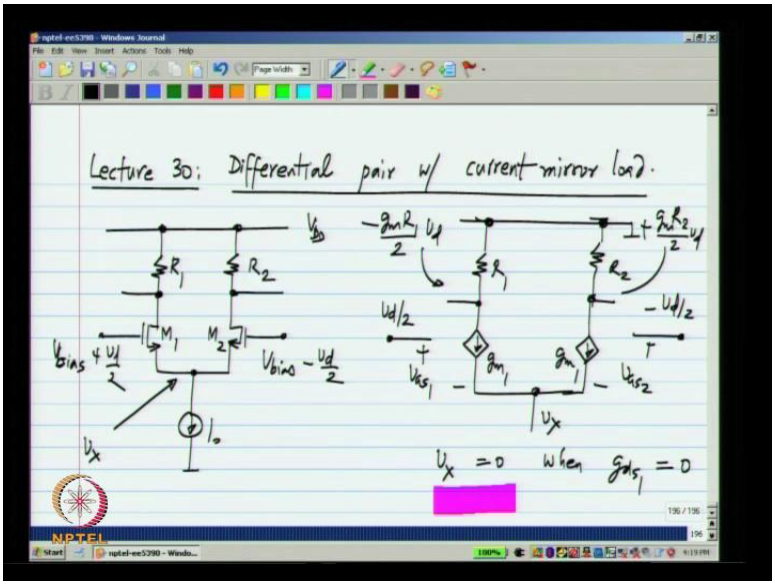

Now, as I said the circuit is asymmetrical that is we have the differential pair which is by itself symmetrical and it is loaded by some asymmetrical load. So, first what we will do is to analyze the differential pair with the asymmetric load and then carry over the those results to power circuit, which is a differential pair with an active current mirror load. Now, here the only difference between, what we have been doing, so far and this circuit is I will have R 1 and R 2, it is two different resistors.

Now, one remark I have to make here I assume that the ideal current source in the tail. Now this again is not the true in reality it will have some output resistance but, to analyze everything with finite resistance here is very complicated, in that in results in complicated expressions again without resulting in much inside. So, you can sort of take it that, this is affect only the common mode picture that is we saw that when you apply common mode input.

The output was not affected if the current source was ideal but, it was affected if the current source had an output resistance. So, that is mainly the contribution of the resistance of the current source, so for all other analyses we will act as though this current source is ideal. Now, what I want to find out is the output voltages and so on. Now, one thing is when the resistances were equal the analysis was simplified, because we know that incrementally that tail node was at 0 volts, when we have a symmetrical circuit with anti-symmetric excitation. The tail node is at the line of symmetry and it is increment is 0 and this considerably simplify the analysis.

Because, if this is at 0 we know that the incremental v g s across M 1 is v d by 2 and across M 2, it is minus v d by 2 and we can just by inspection write down the currents and find the output voltage. So, here it will be minus g m r v d by 2 and here it will be plus g m r v d by 2 and so on. Now, if we have R 1 and R 2 this is no longer true. So, what I will try to do first is to find out tail node voltage, let me just call it v x, when R1 is not equal to R2 in the general case. Now, once we know v x we will able to find the currents in M1 and M2 and write down, the expressions for the output voltages as well.

Now, first of all let me draw the small signal equivalent of this R 1 R 2 this will be a 0 volts, that is small signal ground and let us say I have v d by 2 and minus v d by 2 and this is v x, I will assume that ideal current source that. And it is g m times v g s 1, which is over there and this is g m times v g s 2 which is over there. So, notice that I have taken a transistor without an output resistance, I will assume that identical points g m for the two sides.

Now what will be v x in this case it is a very easy to see, now if your Kirchhoff's current law has to satisfied here g m times v g s 1 has to be equal to minus g m times, v g s 2, that is the current flowing this way has to flow upwards that way. And that you can work

out very easily, it means that v x equals to 0, that is when you apply v d by 2 and minus v d by 2 to the two inputs v x will be equal to 0.

So, even though the circuit asymmetrical v x will be 0, when g d s 1 is infinity let me denote by this subscript g m 1. Because, M 1 and M 2 are identical, I will use the subscript 1 for both of them. Similarly, when I include g d s, I will also denote both of them by g d s 1 but, sorry not by g d s 1 equal to infinity, but when g d s 1 equals 0. So, when r d s 1 equal to infinity or g d s 1 is 0 v x will be 0.

So, in this case also even though circuit is asymmetrical we can write down the result by inspection v g s 1 is v d by 2, v g s 2 is minus v d by 2. So, the output voltage here is minus g m r 1 by 2 v d and here, it is g m r 2 by 2 v d, so this is quite simple. Now, what happen when g d s are not 0, which is the reality in any case.

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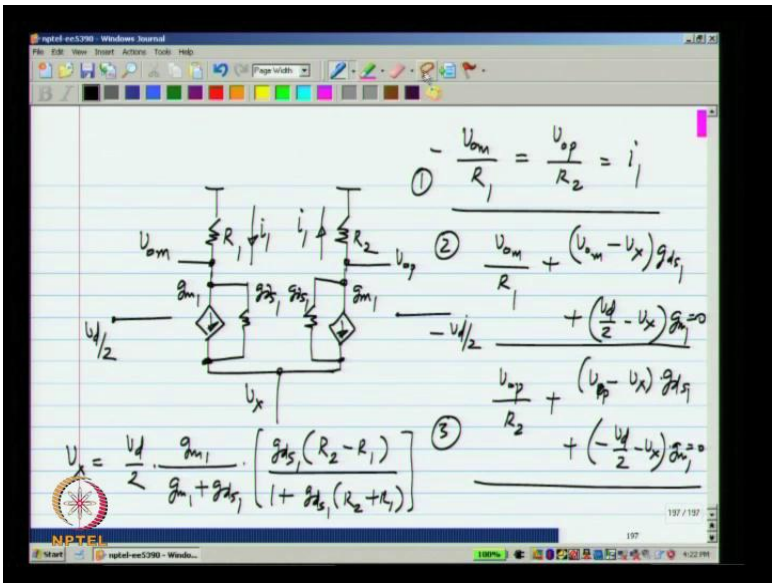

So let us see, so again I will assume anti symmetric excitation because, this is when we have only purely differential excitation. So, this is what is my concern right now and I have R 1 R 2 going to small signal ground, by I also have g d s for these transistors and let me all this V x. So, let me call this incremental current i 1 and it is very clear that the same thing has to flow all the way back into R2, so this will also be i 1 in that direction and let me call this V o m and this will be V o p.

Now, because the current is in R 1 and R 2, R equal to i 1 in opposite directions, we know that V o m by R 1 will be equal to V o p by R 2 and that is equal to this i 1 and if i write Kirchhoff's current law over here. I will get V o m by R 1 plus V o m minus v x, and g d s 1 plus v d by 2 minus v x times, g m 1 to be 0, that is the total current flowing out of this node through g m 1, g d s 1 and R 1.

And, similarly writing it as other node, we will get V o p by R2 plus V o p minus V x times g d s 1 plus minus V d by 2 minus V x times g m 1 equal 0. So, we have three equations and three unknowns V o m, V o p and V x we have to solve for V x. So, as usual please write down these equations for yourselves and solve for it solves for the value of v x and then you can interpret the result. If you do solve for this what you will find is that V x is V d by 2, g m 1 by g m 1 plus g d s 1 times, g d s R 2 minus r 1 divided by 1 plus g d s 1 times R 2 plus R 1. It is just the solution of a linear simultaneous equations quite easy to solve for, so this is what we will get.

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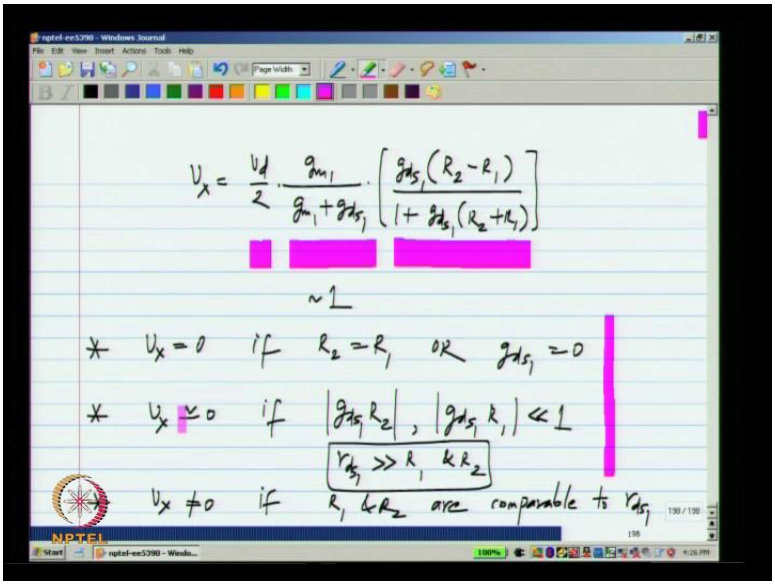

Now, what does it mean if you look at the expression first of all if R 2 equals R 1 it will be 0. That is we knew this already if you have a symmetrical situation, symmetrical circuit when R 2 equals R 1 the tail node voltage, which is a voltage along the line of symmetry will be 0, so that much is true. Now, Secondly, you also see that if g d s is 0, the expression also becomes 0 because g d s is directly multiplying the expression.

So, if g d s 1 happens to be 0, the tail node voltage v x also be 0. But, the tail node voltage will not be 0, if R 2 is not equal to R 1 and g d s is a significantly large number. So, if you look at this expression first of all, we have V d by 2, which is the input applied to each side and this number you expect g m to be much more than g d s in a transistor.

So, g m 1 by g m 1 plus g d s 1, this is of the order of 1 and this number will be something, we do not know what the relative value of g d s 1 R2 and R1 are. Now, from this we can conclude that v x is 0, if either R 2 equals R 1 or g d s 1 equals 0, either this or that becomes 0. Now v x is also approximately equal to 0, if let us say g d s 1 R 2 and g d s 1 R 1 are very small numbers.

This basically means that r d s 1 is much more than R1 and R2, so if the load resistances are much smaller than, the output resistances of the transistor. Then even if the circuit is asymmetrical R1 is different from R2, this number will be very small, because you essentially have here R2 by r d s 1 minus R1 by r d s 1. So, each of those numbers small the difference also will be small and we also know that, if V x will definitely not be equal to 0.

It can be significantly large number if R 1 and R 2 are comparable to r d s 1. So, if R 1 is significantly different from R 2 and are comparable to r d s 1, then we will have a significant voltage swing at the tail node, so this is something to be kept in mind. So, the importance things are that V x is approximately equal to 0. If r d s 1 is much more than R 1 and R 2.

Because these results we will use in later analysis, now the symmetrical case we already knew. Now if g d s 1 is 0, that is basically this is a special case of r d s 1 being infinity and obviously in that case it will be much more than R 1 and R 2. So, V x will be equal to 0. So, this is something quite important because, we can have some funny circuits in which r d s 1 is not very large compare to the load resistance and the results are not all what you expect because, V x will not be equal to 0. Now the reason we are interested in the case where v x equal to 0 is that makes the analyses very simple.

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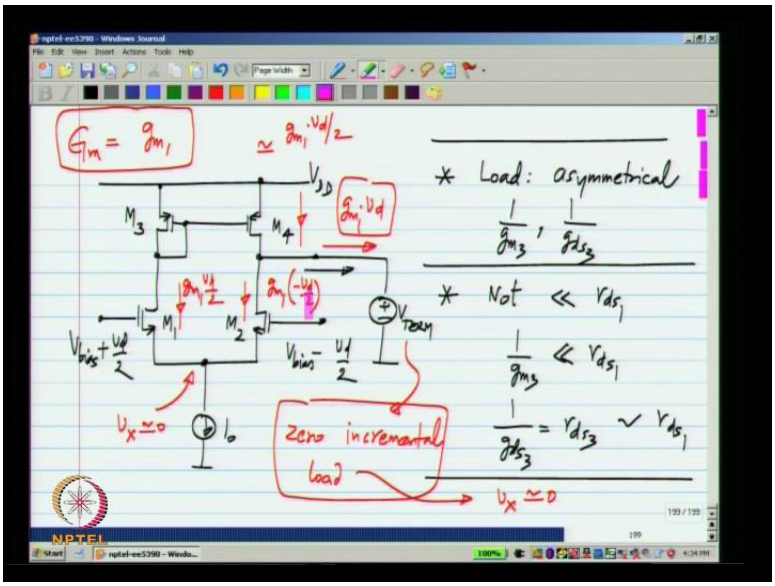

Now, let us get back to the differential pair with current mirror load what is the situation in this case to have a symmetrical load or asymmetrical load what is it, first of all the load is very clearly symmetrically. Because, the small signal resistance looking up here into divert connected M 3, we know is 1 over g m 3. Whereas, the small signal resistance looking up there into M 4, which is in saturation will be 1 over g d s 4 which is the same as 1 over g d s 3. So, the loads are basically 1 over g m 3 and 1 over g d s 3. So, they are very different from each other.

Now, are they both much smaller than r d s 1 and r d s 2 that is obvious because, 1 over g m 3 is much smaller than r d s 1. But 1 over g d s 3 or r d s 3 is not necessarily much smaller than r d s 1, it could be of the same order or even higher, it is of the same orders r d s 1. So, in this particular circuit clearly this voltage will not be equal to 0, so that makes it quite difficult to analyze and if you put down the r d s of all these transistors and analyze. It the expressions would be, so missing that we would not get any inside into the circuit.

So, what we will do instead to use a trick now in the previous lecture i mentioned that, i could connect the voltage source here equal to V d 3. The value is v d d minus v s g 3 at a current of l naught by 2. So, that is what I call is termination voltage v term if i do that nothing will change because, this quiescent output voltage was anyway equal to this

voltage and I can connected it out. But, what does change now if you look at the incremental resistance looking from here what is it.

It is a parallel combination of what is contributed by M 4 and what is contributed by this voltage source and that is obviously 0. So, in this particular case the resistance looking up here is 1 over g m 3, the resistance looking up here is 0 and both are much more smaller than r d s 1 and we can safely assume that v x equals 0, so that is the reason why i connected the voltage source to the output.

Now, how is this useful I can calculate the behavior of circuit in various ways. So, let us say i want to calculate the voltage gain, which was basically g m or naught I can do it in different ways, I can try to directly calculated alternatively. I can first calculate the current output of the trans conductor, that is the current that is going there. I can calculate the output resistance separately and multiply the 2 this viewpoint is anyway useful.

Because, first of all for the op amp we thought it has a trans conductor something that takes the input voltage converts it to current and passes it through capacitance. We have to compute the current that is flowing through the output of this the current that is flowing into the voltage source. So, for that also this viewpoint is helpful but, what I wanted to emphasize here is that, if we connect a voltage source to the output though the circuit is asymmetrical the two load resistances will be, so small that the tail node voltage can be safely assumed to be zero incrementally.

So, under this condition v x is approximately 0, so that makes the analysis very easy in the quiescent condition. We have i naught by 2 flowing that and when I apply an incremental v d by 2. The increment in the tail is almost 0, so that means that the incremental current here is g m 1 v d by 2 and there also it is g m 1 v d by 2 in the opposite direction.

Now, this incremental current flows through M 3 and comes out at M 4 now you can again put the small signal equivalent circuit M 3 and M 4 and analyze it. In fact, encourage to do that to see what happens again I will use a quick approximation. So, M 3 M 4 is a current mirror now, it turns out it is not a perfect current mirror because, of the output resistance r d s 3 and r d s 4 but, I assume that to be a perfect current mirror.

So, the current here is a approximately equal to g m 1 times v d by 2 in that direction. Because, if you have a current mirror you apply some current it mirrors it, now if i have you apply increment to that current it mirrors that increment as well here. I am looking at the incremental picture and the current mirror, mirrors the increment also. So, what will be the total current here flowing into the terminating voltage source v term that will be nothing but, g m 1 times v d where g m 1 is the trans conductance of M 1 or M 2 in the quiescent condition.

So, this expression is very simple but, we had to use the fact that v x is approximately equal to 0 in this condition. So, this differential pair with a current mirror load all works like a trans conductor whose trans conductance g m is nothing. But, g m 1 the trans conductance of transistors M 1 and M 2 which form the differential pair. So, now that we have calculated the trans conductance we have to calculate the output resistance as well, we know that the d c gain of opamp will be the trans conductance times. The output resistance it is a very important quantity because it determines the steady state error. Now, if the transistor did not have any output resistance we would simply have an ideal trans conductor. The d c gain would be infinite we know that is not the case, so we have to compute that.

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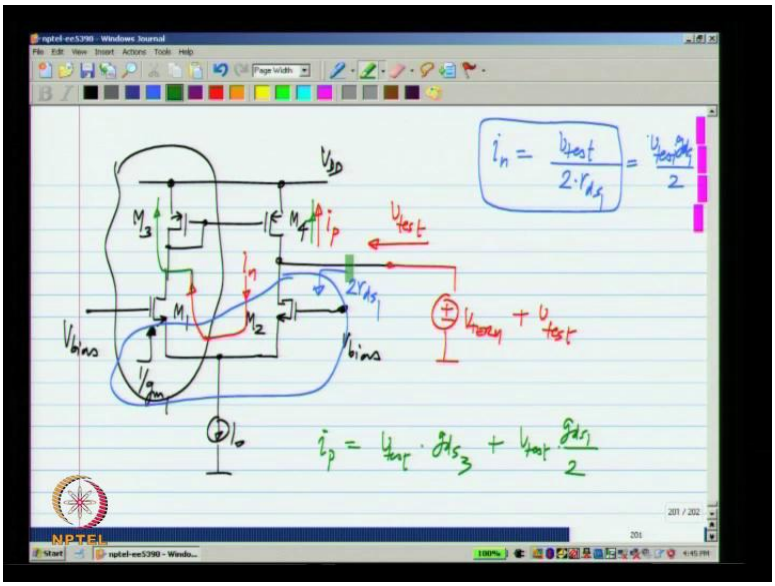

So, again let me put down my differential pair now what i want to calculate is the resistance looking there. The incremental resistance looking into the output of this circuit

and when I want to calculate the output resistance, the input is desirable. So, both the inputs are at v bias or incrementally they will be at ground. So, again you can put down the equivalent circuit of this the small signal equivalent circuit, including all the trans conductance and resistances are individual transistors and analyze.

It now because, the operating points of M 1 and M 2 are identical, they will has a same trans conductance and output conductance. Similarly, M 3 and M 4 will have the same trans conductance and output conductance. Now, again please take this as a circuit analysis exercise and workout the resistance looking in the, what I will do is to calculated based on approximate method instep and you make sure that the expression that you get under some reasonable approximation, will reduce to what i am going to calculate.

Now, how do you do this, we can either apply an incremental voltage and find the current or incremental current and find the voltage. So, I will assume that this is terminated by v term and to that I apply an incremental test voltage. So, I have to find the incremental test current, I know that when I apply v term alone the current here will be 0, this we discussed earlier, so this v test will give me some test current. Now of course this now is a completely asymmetrical circuit, as well as excitation. So, none of the half circuit concept will apply now what is I test.

I test consists of two parts one which goes into M 2 and one which goes into M 4 and I will calculate these two separately and add them up to find the output conductance or output resistance. In order to do this, we need to use some results from before mainly the input and output resistances of source follower or a common gate amplifier.

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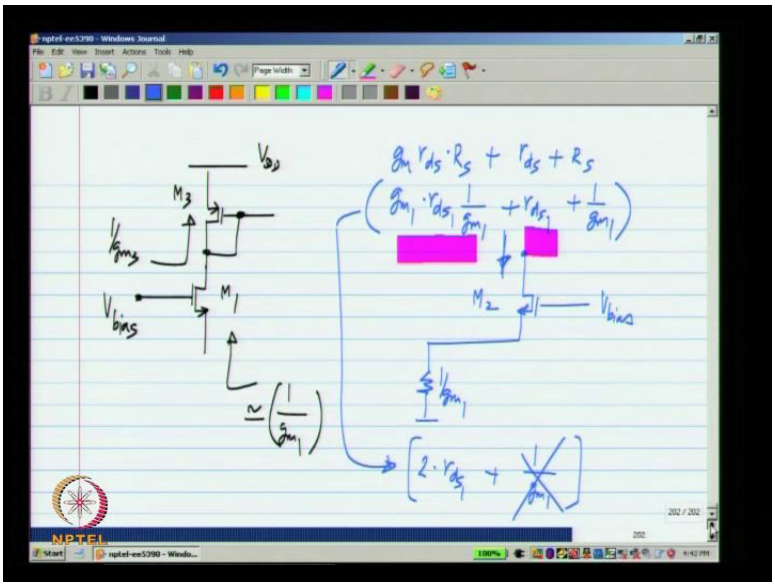

So, first of all let me take only this part of the circuit the gate is at fixed voltage and the drain is loaded by, the divert connected transistors. The small signal impedance here is 1 over g m 3, this is M 3 and that is M 1. Now you can think of this M 1 as a common gate amplifier, now you have a common gate amplifier loaded by a relatively small resistance. That is a resistance that is much smaller than it is r d s, the resistors looking in here will be approximately 1 over g m 1, so this is something that we know.

Now, we know that this is not unconditionally true if the load resistance increases a lot then this resistance will also increase but here it is loaded by a relatively small resistance. So, looking into the source of M 1, we have a resistance of 1 by g m 1, so looking in here we have a resistance of 1 by g m 1, so that is something to we kept in mind now. Secondly, what I will do is whatever circuit is to the left of this side, I can replace it by an incremental resistance 1 by g m 1.

So, as i said earlier I want to find out how much current goes there and how much current goes over here. Let me call it i p and i n the parts that are going into p mos and n mos respectively. Now to find i n, I want to see what the circuit looks like looking downwards into M 2. Now to M 2 source something complicated as connected but, I know that it looks approximately like 1 by g m 1.

So, now next I will take only this part of the circuit and that will be M 2 and it is going to something, which looks like 1 by g m 1 and looking in here what do I see. Now, recall

that this looks like the output circuit of a common gate amplifier, this circuit look like the input part of the common gate amplifier. This looks like the output part of a common gate amplifier and we know that the output resistance of a common gate amplifier will be g m r d s. R s plus r d s plus r s.

Where r d s is the output resistance, so the common gate amplifier transistor and r s is whatever is connected in the source. Now substituting the terms that, we will have g m 1 r d s is something, r d s 1 and R s will be 1 over g m 1 plus r d s 1 plus 1 over g m r. Now the first two terms here will give you 2 times r d s 1 and we will have 1 over g m 1. Now, 1 over g m 1 will it is a much smaller resistance compare to r d s. So, that can be safely neglected. So, the resistance looking in here is approximately 2 times r d s 1, it looks like a resistance 2 times r d s 1, that is if i apply v test here the current that flows there i n will be v test divided by 2 times r d s 1. So, I have to now find i p and then add them up to get the final answer.

Now, this is a somewhat non intuitive result now somewhat careless you could to say that i have an n mos transistor M 2 and it is output resistances r d s 1. So, the resistance looking downwards is r d s 1 but, it turns out it is not r d s 1 but, 2 times r d s 1. Now what is i p have an incremental v test apply here and that appears directly across the output resistance of M 4. So, i p will have a component due to the output resistance of M 4, now if you have some difficulties with this type of reasoning what you can do is imagine first that only M 1 and M 2 have a finite output resistance and only M 3 and M 4 have a finite output resistance and then see what happens. So, you will end up getting a combination of these two cases. If I have a v test here and I have the output resistance, of M 4 which i will call g d s 3.

Because, g d s 3 and g d s 4 has a same value, so i p will have v test times g d s 3 v test divided by r d s 3. Now that is not the only thing it has because, you observe what happens to this i n, if I apply v test some i n, equal to v test by 2 r d s 1 was flowing that way. Now where it flow no incremental current can go into the current source, so it has to flow through M 1 and when it flows to M 1, it also flows to M 3 and gets mirror.

So, this flows to M 3 and an equal current will get mirror there, so i p is nothing but, v test times g d s 3 plus i n and i n is, v test times g d s 1 divided by 2 this is v test g d s 1 divided by 2. So, this is a very interesting result, so the current flows into the p mos

transistor as a term containing the output resistance of p mos as I expected, but also term containing the n mos, because, of this feedback loop here the term corresponding to the n mos transistor has only g d s of the n mos transistor.

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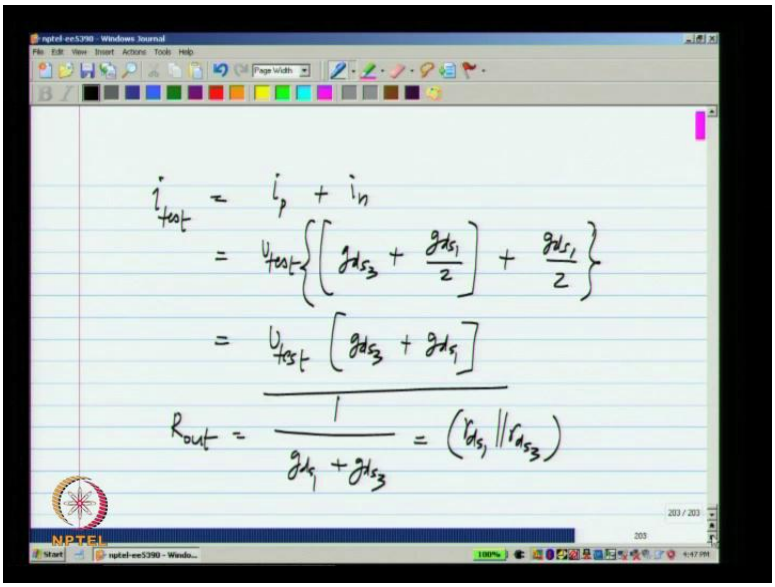

So, the output current i test is i p plus i n which is equal to v test times g d s 3 plus g d s 1 by 2, this is part due to i p plus g d s 1 by 2 due to i n and finally, the answer itself is rather simple, it is v test times g d s 3 plus g d s 1. Now, if you narrowly looked at the circuit and decided that the output conductance is the sum of n and p mos transistors output conductance. The answer would be correct but, the individual current would be wrong.

So, it is really important to understand exactly what is happening in the circuit, so the output resistance is quite simple, it is simply the parallel combination of output resistance of the n mos and p mos transistors. But, what is happening in the circuit is somewhat complicated, so there is some current that goes through n which also gets mirror, through the p and that gets added to the current that is thrown by the p mos transistors output resistance. So, r out is 1 over g d s 2 plus g d s 3 which is equal to r d s 1 parallel r d s 3.

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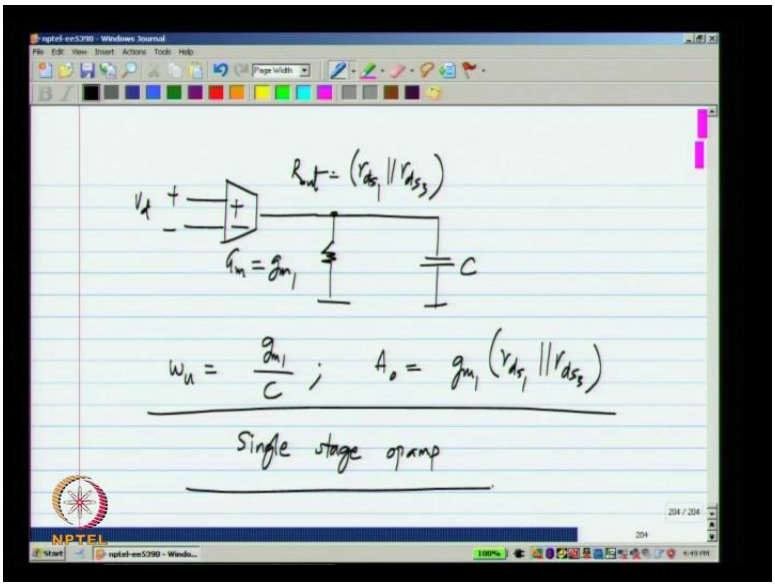

So, the differential pair with the current mirror load can be represented by a trans conductance. Whose g m is the g m of the n mos transistors and in our case and whose output resistance, is the parallel combination of p and n mos output resistances. Now to this if you attach a capacitor c, what you will get is an op amp of unity gain frequency g m 1 by c and d c gain of g m r out. Which is g m 1 r d s 1 parallel r d s 3.

Now, this is the basic op amp amplifier circuit, it works exactly as we anticipated the model that we have is that of, a trans conductance in parallel with an output resistance and the d c gain that we get is of the order of the d c gain of single transistor. What I mean that is it is like having g m times r d s, which is the d c gain of the signal transistor has the d c gain for the whole op amp. So, this is what is known as single stage op amp it is the simplest of the op amps, it will have many shortcomings and we already investigated topologies for two and three op amps, but this is the starting point for all op amps and it would be very good to understand the results pretend to this very thoroughly.

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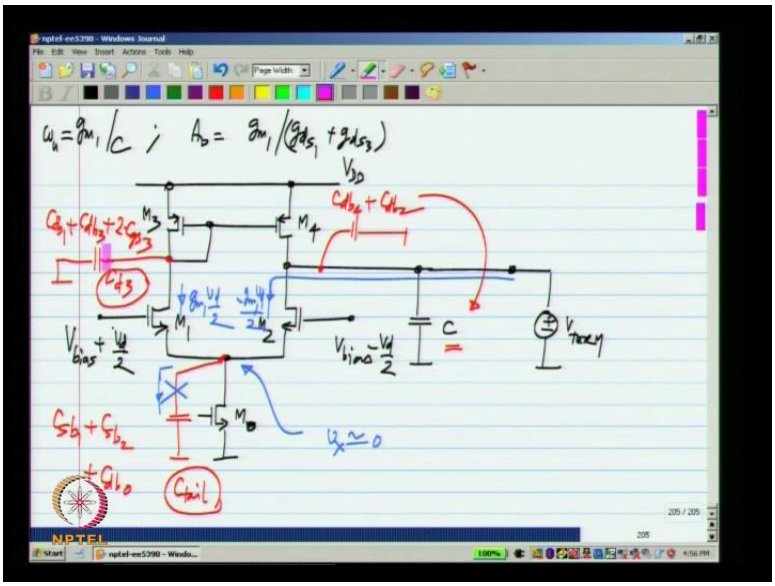

So, this is the simplest op amp, that i have i bias the inputs at some v bias and I could apply v d and minus v d by 2. But, of course my objective is to put this op amp in feedback and operate. It as a feedback circuit and this I said was an op amp with a unity gain frequency g m 1 by c and d c gain of g m 1 by g d s 1 plus g d s 3 or g m 1 times r d s 1 parallel r d s 3. Now I could use of buffer if I wanted to it is many times inconvenient to use that but, if i do want use the buffer i can use that.

So, these results seem to say that circuit with a single pole right, we have single capacitance in the circuit and that gives you a pole very close to the origin. But not exactly at the origin, the pole will be at g d s 1 plus g d s 3, divided by c in the left hand half plane. Now of course, we know that is not true because, we have not included the parasitic capacitances of any of the devices in the op amp.

So, we will do that and then see what happens because, we also investigated the stability of feedback system earlier and we know that any extra poles or 0's can cause phase lag or lid and modify the stability characteristics. Now, we have to look at the complete circuit including all the parasitic capacitances and judge the stability of the circuit. Now where we will have parasitic capacitances, in general we will have parasitic capacitances everywhere in the circuit.

Now, one guideline that I am going to use is generally, c g d is much smaller than c g s and many times I am going to neglect that, otherwise the c g s capacitances significant as

or c d b and c s b which are the bulk source and bulk drain capacitances. So, first of all i will have some capacitances here, now this will consist of c s b of M 1 plus c s b of M 2 by the way this current source i naught is also going to be made using a mos transistor let me call it M 0.

So, it will also have the c d b of M 0 and here from this point to the small signal ground, i will have a parasitic capacitances and what will that consist of first of all it will consist of, drain bulk capacitances of M 1 and M 3. Now because, the drain of M 3 is connected to it is gate it will also include c g s of M 3. Now, the gate of M 4 is connected to the same point.

So, it will also consist of c g s of M 4 which we assume is identical to that of M 3, so we will have 2 times c g s 3, i will neglect c g d's in this analysis. So, we will have another capacitance here and finally, to this node we also have parasitic capacitances which are added which are c d b 4 and c d b 2. Now this we will assume is observe into the capacitor c, so c capacitor consists of the actual c that you connect plus the parasitic capacitances that you have here.

Now, this entire thing can be represented by a capacitance let me just call it c d 3 and this entire capacitances can be clubbed into single capacitance 3 tail. So, we have 3 extra capacitances but, 1 of them is in parallel with an existing capacitance, so it can be observe into it right. So, it just modifies the values of c, so we have these 2 extra capacitances that we have to take care of as before, what we will do is to terminate the output with an ideal voltage source.

So, that way we can use you simplified, the result that tail node voltage is approximately 0 and go ahead. Now only the difference between earlier analysis and now is that earlier the circuit was frequency independent. Now the circuit will be frequency dependent i will terminate the output with a voltage v term which is equal to v d d minus v s g 3, so that no current flows in the quiescent condition.

Now, if i apply v d by 2 and minus v d by 2 to M 1 M 2 gates what will happen first of all i know that, v x is approximately 0. So, the incremental voltage at the tail is 0 the current through this parasitic capacitances is approximately 0. So, i will neglect that I will analyze this only with a purely differential inputs, that is plus v d by 2 and minus v d

by 2, under that condition the current flowing through c tail is negligible. I will just ignore that. So, I can ignore this one all i have to do now is to find the effect of c d 3.

Now, because this voltage is 0 I can calculate these two currents easily this is g m 1 v d by 2 and that is minus g m 1, v d by 2. Now this current goes into the voltage source because, the voltage source present the short circuit. So, all of these current simply has to go into the voltage source it cannot go elsewhere, now this current was getting mirrored through M 3 and M 4.

Now there is an additional capacitance, so we should say what happens to it and finally, the current that is coming out of M 4 will get added to the output, previously all of g m 1 v d by 2 came out of M 4 and it was added to this 1. Now some part of it go through this capacitance c d 3 and whose the remaining part will get added to M 4.

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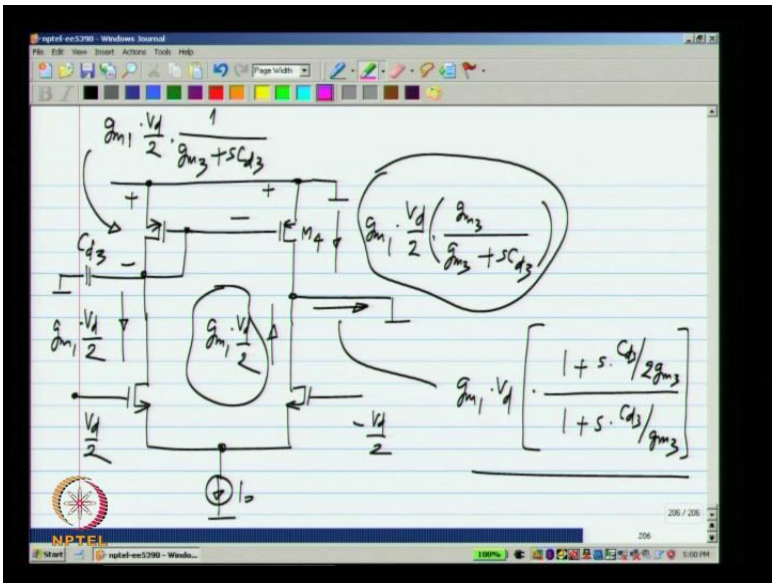

So, I will put down only the current mirror and I have a current g m 1 v d by 2, I will use the Laplace to M 1 quantities here. Because, I have to analyze the frequency dependence circuit, that is c d 3 and this mos transistor is equivalent to small signal resistance of 1 over g m 3. If you wish to you can put down the small signal pictures and analyze it completely. But, I am going to again do it simply this is terminated by short circuit an incremental short circuit because, i have v term over there.

So, the voltage that is develop here in that direction this v d d by the is also small signal ground. So, the voltage here will be the current input g m 1 v d by 2 divided by the total admittance, which is g m 3 plus s c d 3, now this voltage is applied as v g s to m 4. So, the incremental current in m 4 would be that times g m 3 or g m 4, which is the same as g m 3. So, the current there the current in this direction would be g m 3 times v g s, the voltages in the other polarity. So, the current flowing out of M 4 would be equal to g m 1 v d by 2 g m 3 by g m 3 plus s c d 3.

I have ignored the g d s of M 3 because, when compare to the conductance g m 3, that is the rather negligible conductance. So, I am going to ignore that ok. Now, first of all you see that this expression at d c when s equals 0. It is g m 1 times v d by 2, so that is what we had assumed earlier while doing the d c analysis. Now what happens at high frequencies more and more of the current from the transistor M 1 goes into the capacitor.

So, at very high frequencies no current is mirror, what else do we have in the circuit i have increments of v d by 2 and minus v d by 2. So, the current here in the upwards direction is g m one times v d by 2. So, the total current flowing out will be the sum of this current and that current and if i write it down, i will get g m 1 v d by 2 g m 3 plus s g d 3 divided by g m 3 plus s c d 3.

Which i will rewrite as g m 1 times v d 1 plus s c d 3 by 2 g m 3, 1 plus s c d 3 by g m 3. So, it turns out that the trans conductance of our basic amplifier, which is a differential pair with a current mirror load has a pole and a 0. The pole is at minus g m 3 by c d 3 in the left half plane and the 0 is at twice that frequency. Now, why do get this pole and 0 first of all there are two paths to the output the output consists of two half's of current 1 through M 1 and 1 through M 2, that is the drain currents of M 1 and M 2 get targeted up.

Now, the drain current of M 2 goes directly to the output, now it is not affected by high frequencies. The drain current M 1 goes to a current mirror but, the current mirror is imperfect at high frequencies. Because, of the parasitic capacitances c d 3 because, of this at very high frequencies all of this current simply, goes into the parasitic capacitances and nothing is mirror only the current in M 2 goes to the output and that is very obvious from the expression as well, you can see that at low frequencies.

The trans conductance is g M 1 and at very high frequencies the trans conductance will be g m 1 by 2, that is only the part of the current contributed by M 2 will go to the output. So, in the middle somewhere you will have 0 and the pole and this will modify the frequency response to some extent and you can see that. The pole is at the lower frequency than the 0. So, you will have net phase lag in the overall trans conductance or trans admittance to be precise.

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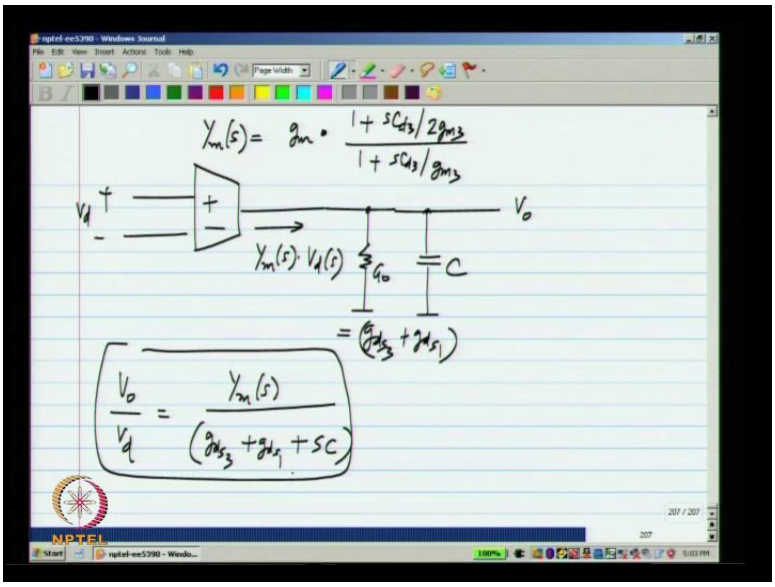

So, before when i v d here i would write the output current as g m 1 times v d, now that is no longer true this is a frequency dependent quantity. So, I can represent the trans admittance as g m times 1 plus s c d 3 by 2 g m 3 and 1 plus s c d 3 by g m 3 and the output is not g m times v d but, that is trans admittance times v d of s. We know that that goes into an impedance with consists of the integrating capacitor c and the output resistance g o, which is basically g d s 3 plus g d s 1.

You want the transfer function of the op amp, v naught by v d that is simply the trans admittance divided by g d s 3 plus g d s 1 plus s c and if you do not have this conductance you will simply have y m of s by s c. So, what you end up having is the dominant pole, due to the integrating capacitance and a non dominant pole and 0 because, of the current mirroring. Now, earlier I had said that if you have two paths with different frequency dependences, to the output you can expect to have a 0 and that is exactly.

What is happening here as well you have the path through the current mirror which is dependent on frequency and path from M 2, which is largely dependent of frequency, so you will end up having 0 as well we will continue from here in the next class.