Analog Integrated Circuit Design
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Lecture No - 29
Differential and Common Mode Half Circuits;
Differential Pair with Active Load

Hello and welcome to lecture 29 of Analog Integrated Circuit Design. In the previous lecture, we look at the differential pair as means of taking a difference between two signal, this is an operation that is essential in realizing an opamp. In this lecture what we will do, is to analyze the various aspects of differential pair and also look at the simplest opamp that possible using a differential pair.

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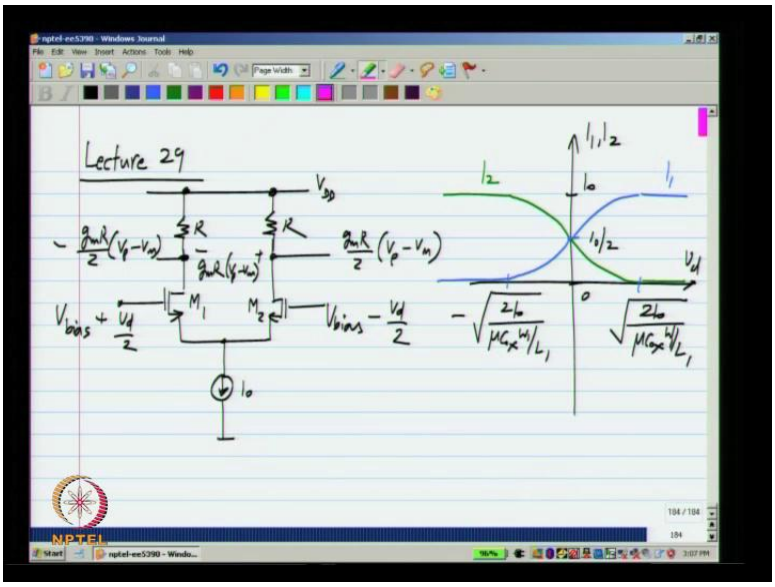

We want to take the difference between two signals V p and V m, and this is the structure we thought of it as V m being buffered by this transistor M 2, and apply to the source of M 1. Whereas, the V p is applied to the gate of M 1 and the current in M 1 of course, depends on the difference between the gate and source voltages. Now, the structure is symmetrical and you can insert thing of V p being buffered by M 1 and applied to the source of M 2. So, the currents and the drains of both M 1 and M 2 will have information about V p minus V m, so you can load either of them, I will show a case where both sides are loaded by resistance R.

In this case what happens is that on the right side, we will get g m R by 2 V p minus V m and on the left side we get g m R by 2 V m minus V p, and the difference voltage between these two is g m R V p minus V m. Now, this node is called the tail node of the differential pair M 1, M 2 and this current is called the tail current source and that is equal to I naught. We know that the bias current in the transistors will be I naught by 2 because of symmetry, let us say each side is bias that some voltage V bias and then, we can apply V p and V m as increments to the two sides.

Then when V p and V m are 0 we have I naught by 2 flowing each side, and when V p and V m are applied you will have these currents. Now, this is somewhat crude analysis we assume that, we have an idle current source in the tail, later we will add non idle features to that and see what happens. Now, this is the small signal behavior small signal currents in M 1 and M 2 will be related to the difference voltage and this is the exactly the behavior we want to in an opamp. An opamp of course, we want in integrating behavior, we would like this current to go into a capacitor we will see how to arrange that.

But, for now we know that, the currents through these are related to g m times V p minus V m by 2 and we also analyze the large signal behavior we assume that, V p and V m are equal and opposite voltages. And in such a case the currents in the two transistors would be something like that, this value is I naught by 2 and that is I naught this is 0 of course, and these voltages are ((Refer Time: 04:09)). Now, as we increases in the positive direction, what happens is that the V g s of M 1 will be larger than the V g s of M 2, so the current M 1 will be larger than the current in M 2.

And as V D increases this imbalance goes on increasing, until a point where all of the tail current I naught flows in M 1 and nothing flows into M 2. And the voltage tills that is happens is given by square root of 2 I naught by mu c x w y l, now when you have a negative value of V D the opposite happens, the V g s in M 2 will be more than the V g s in M 1, and it is currents goes on increasing until it reaches a value of I naught. Now, around the value of V D equal to 0 the variation in current with the input voltage will be a straight line, and the slop will be g m by 2.

In each transistor the incremental current will be g m by 2 times V D that is what we mean by the small signal current being g m by 2 times V p minus V m. So, the current

does increase in proportion to the input difference of course, as you expected over a small range and beyond that the circuit becomes no linear and in this part the circuit is saturated. Now, once you go beyond this point there is no response with V D by the way these are the currents I 1, I 2 verses V D and this is the current I 1 in transistor M 1, and this is the current I 2 in transistor the M 2.

So, this is something kept in mind, sometimes we need to know what is the linear range over which this differential pair operates. This is sometimes important for cases where we operate the differential pair not inside of opamp, but just by itself. And in an opamp also it is good to know when the current gets saturated, because it is when those current gets saturated that to enter slowing.

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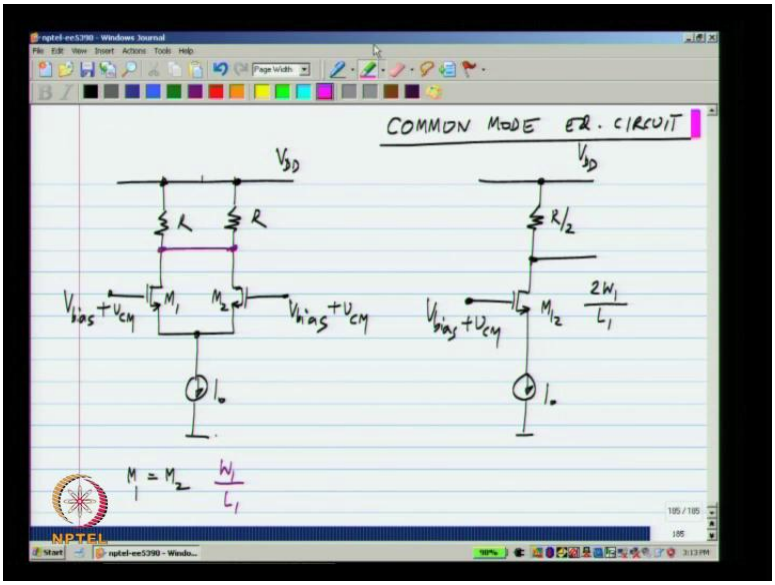

Now, we have a circuit like this, and the circuit itself is symmetrical it is of course, assumed that M 1 and M 2 are identical, so M 1 as size W 1 by L 1 and M 2 has also same size W 1 by L 1, so once this is assumed the circuit is symmetrical about that line. Now, before we going to make this into an opamp, let us look at some properties of this circuit and see how to analyze it. Now, we want to do these both for large and small signals, specifically for small signals that is when we apply the small signal increments to the two inputs, we want to see how things behave.

Now, let us see couple of cases first of all in this condition the circuit is completely symmetric, and the voltages are also symmetrical the same V bias is applied to each of

these sides and by symmetry is obvious that this voltage and that voltage will be same. In fact, you can assume them not to be the same and then, come up with the counted diction and through that they will indeed with the same. Now, let us say we apply equal increments to the two sides I call that V C M that means, it is a common mode increment, it is common to the two sides and I will apply an equal increment.

Again it is easy to see that, this voltage on that voltage will also be equal to each other, in general let us say we have a circuit, which is completely symmetrical just to show the symmetry I will show it as the same network mirror or down the two sides. Now, the circuit will have a number of nodes in that have as well, and let us things of these two as input and apply equal voltages to the two sides, now by symmetry it is clear. So, some of these could be tried to ground and there could be some components here as well, but by symmetry it is clear that let me number these nodes 1 2 3, 1 2 3.

The voltage here will be the same as the voltage there the voltage here will be the same as the voltage there, and the voltage here will be the same as the voltage there, in our circuit we have only one such node, so the voltage here and there will be the same. Now, in that case, we can safely connect the responding nodes together, because they were the same voltage. When you connect them like this no current will flow through the wires connecting them, and so the circuit is not disturbed in anyway, so nothing changes due to this connection.

So, what I could do is to do that, now what it does is to simplify the circuit the significantly for the sake of analysis. Now, as you can see the two resistors are in parallel, and the two Mosfet are in parallel, when we say two Mosfet are in parallel, it means that all the corresponding terminal are connected to each other. That is the two gates are connected to each other, the two drains are connected to each other and so are the sources and the bulks. So, let me redraw this circuit, let me assume that the size of M 1 and M 2 was sum W 1 by L 1.

Now, I can combine the parallel resistors into a single resistor R by 2, I can combine the parallel MOS transistor into a single MOS transistor M 1 2 with the width 2 W 1 and the same length L 1 and this current remains I naught. And this will be a V bias plus V C M, as you can see where we had pairs of components, we have a single component for the

resistor and the MOS transistor. And the component along the center line of the circuit, in this case the current source will remain as it is.

So, roughly speaking the number of components gets divided by half, whatever is in pairs will be halves and whatever is along with center lane will remain as it is. So, the number of components in the new circuit will be a little more than halves of the original circuit, so that means, a corresponding simplification in analysis, which we are going to exploit. And this is known as the common mode equivalent circuit, now this came just from the symmetry between two halves as a circuit, always side was we have symmetrical circuits we apply equal inputs to the two sides.

So, that means, that the voltages in each halves will be the same, they can be connected together, so if we have symmetric circuit like this, we can fold it up connect the corresponding nodes and come up with a simpler circuits with which we can analyze. And this is as I said called the common mode halves circuit, and also one thing to notice here is that the only property that I used here is the symmetry of the circuit, I did not say anything about linearity, I did not use that. So, this common mode halve circuit as valid four large signal increments in V C M, as well as small signal is obvious. Now, we would not do the analysis right now, we will do the analysis a lit later.

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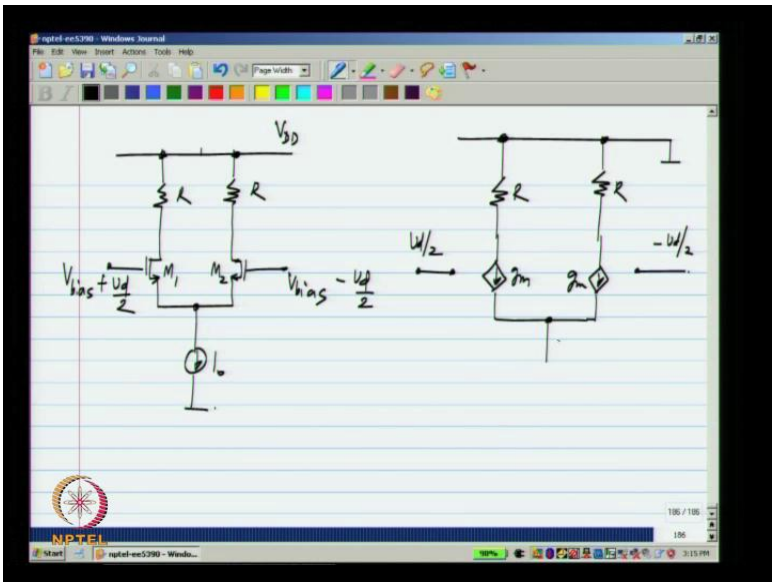

Now, let us consider a different kind of input, let us assume that that two inputs, the inputs to the two side of the symmetrical circuit are equal and opposite, and this is

known as anti-symmetric excitation. Let me draw the small signal equivalent circuit of this, this is what we will have the reason do, the small signal equivalent circuit was the small signal equivalent circuit is by definition linear, and I am going to use that.

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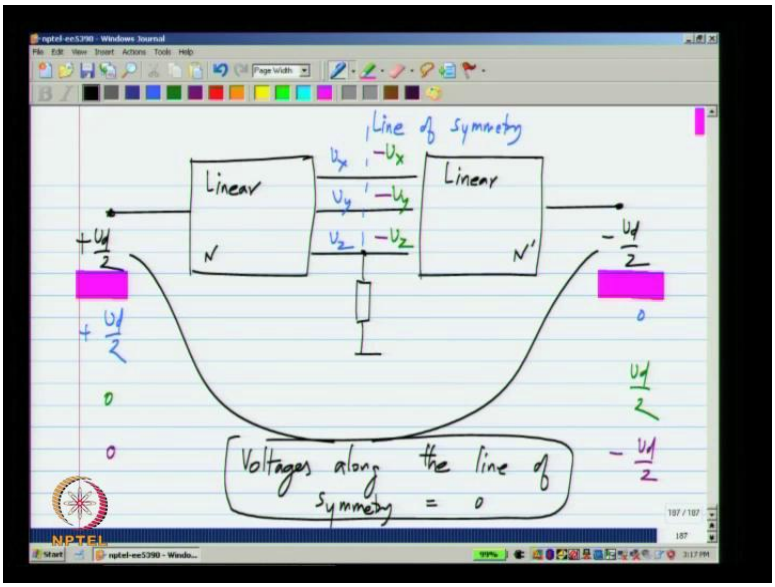

So, let us imagine that we have two linear circuits, which are exactly the same, that is it is a symmetrical circuit with some nodes connected between them, and there could be some common components as well. And let me assume one input on each side, there could be more the important thing is that these are linear, and let us say I have anti-symmetric excitation. What happens in this case, because it is linear I can apply super position, first of all I have only let us say, I have plus V d by 2 and 0 on this side, allow some voltages V x, V y. V z along the nodes of the line of symmetry.

Now, let us say I have 0 and V d by 2, now because of the symmetry in the circuit, I will also have V x, V y and V z along the line of symmetric, on the nodes which lie on the line of symmetry. Let us say I instead have 0 and minus V d by 2, what will happen because of linearity where I had V x earlier, I will have minus V x and minus V y here and minus V z and so on. So, when I have both plus V d by 2 and minus V d by 2, what am I going to get I will get a super position of these two obviously, the super position is 0, so that means that in this case, in case of anti-symmetric excitation, the voltages along the line of symmetry equal 0.

So, this comes from my combination of linearity and symmetry, symmetry guarantee is that, the response from each side is the same and linearity guarantee is that, if you make one of the stimulus opposite, one of the input voltages opposite of what it was. Then the response also will be the negative of what it was, and if you sum of the two you will obviously, get 0 along the line of symmetry.

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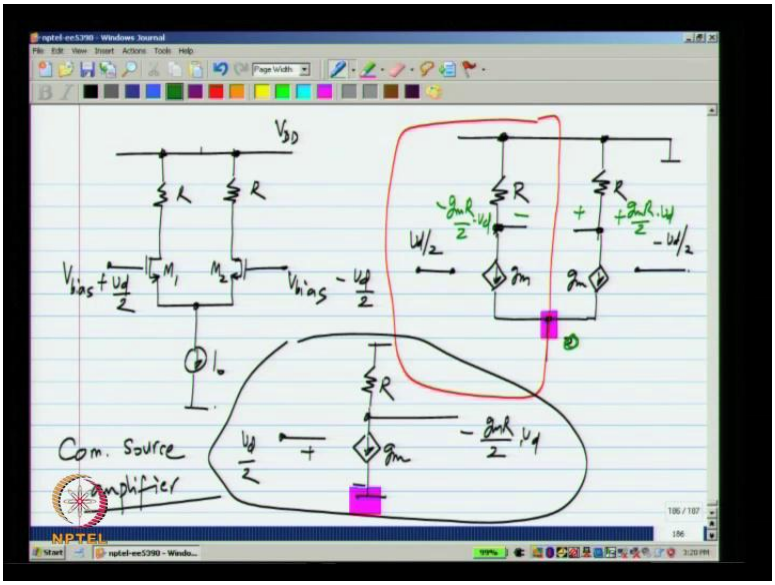

And the case of differential pair, there is this one node along the symmetry and that will be at 0, now earlier we determined this from a conventional analysis, but in any fully symmetrical circuit with anti-symmetric excitation, the nodes along the center line will have 0 volts. So, this can also be used to simplify the circuits, so these voltages will be 0 0 and 0, now again because of symmetry and linearity, if the voltage at a particular node here is some V w to voltage of the corresponding node there will be minus V w.

So, first of all I do not have to analyze the full circuit, I analyze it by setting these voltages to 0 and I analyze only one halves of the circuit, then I know that in the other halves of the circuit, whatever voltages I have here can be negated and the solution obtained. So, whatever voltage is here, let me call that V w that will be minus V w, so what do I do with the differential halve circuit, I will analyze only one halves of the circuit, this case I will analyze let us say only this halves. Now, how do I do that, this point corresponds to that point it is at 0, this is anyway a small signal ground, I have R and g m and g m times this voltage of course, and in input V d by 2.

And the solution here is trivial the output is minus g m R by 2 times V d, and this is nothing but, the common source amplifier. Now, what do I do with the differential circuit I know that here, I will have minus g m R by 2 times V d. And from earlier arguments at this point I will have plus g m R by 2 times V d, the exact opposite polarity and the difference between these will be the g m R times V d, so I can easily calculate that. And this node voltage will be at 0, it is not connected to ground, but in the differential circuit, because of symmetry of the circuit and anti-symmetry of the excitation that will be at 0.

And this is known as the differential halve circuit, just like the common mode halve circuit it reduces the number of components and consequently makes the analysis easier. So, that is why we use that, these are very useful when you have a fully symmetric circuit and anti-symmetry excitation or symmetric excitation. Now, right now the circuits that we make will not have this property, that the circuits will not be fully symmetrical, later we will come to a class of circuits which for various very good reasons will be fully symmetrical.

And the voltages supplied will be either the same on two sides, that is symmetry excitation or equal and opposite on the two sides, that is anti-symmetrical excitation. So, this analysis extremely useful for those circuits, but because the differential pair by itself is symmetric, it is a good idea to know those things. Now, earlier we analyze the differential pair using conversational model analysis it is quite easy, because it is a circuit itself quite small.

But, it can be made even simpler and this simplicity is particularly helpful, when we go to bigger and bigger circuits. Let us come back to the common mode equivalent circuit, what did we have, I have V bias V C M and this is M 1 2 the combine transistor, which has the width of 2 times W 1 and a length of L 1.

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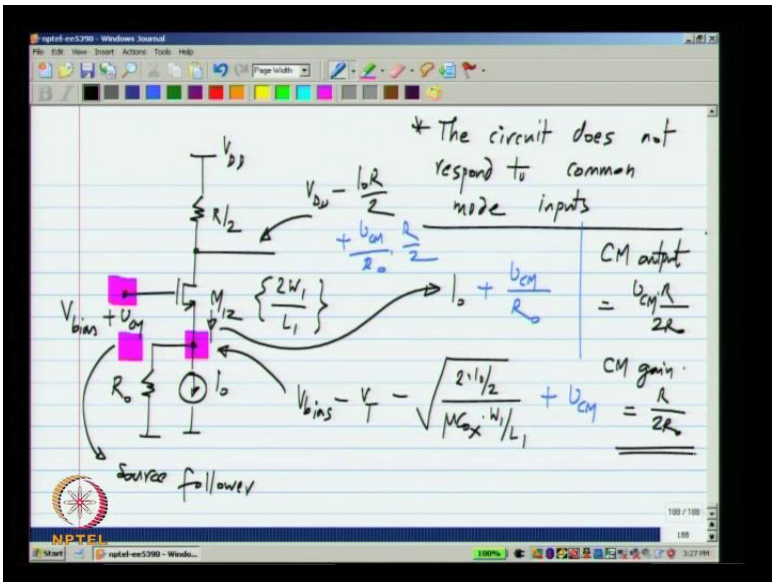

Now, is obvious in this that V C M has no effect on the output voltage, because this I naught, the current I naught has to flow into the source and also out of the drain, so the voltage at this point will be V D D minus I naught R by 2, independently of the voltage V C M. So, this means that the circuit does not respond to common mode inputs, that is common mode gain of differential pair is 0. Now, some time back we discuss the common mode rejection ratio of opamp, I said that the opamp should respond only to the difference voltage and not to individual voltages, not to the average value of the voltage.

And here it look like we have exactly what you wanted, it responds to the difference voltage where it does not respond to the common model voltage at all. Now, of course, this is not true, because we have assumed the idle component here, the tail current source that we have used is idle and that is why it looks like, it does not respond to the common mode input, well replace it by a real current source and see what happens. Now, this current source is idle, so the current through a load resistance is also exactly I naught, this is a combine load resistance by the way.

Now, in reality the current source will not be idle, it will have some output resistance R naught what will happen in this case as increment V C M is applied, this node increases. In fact, if you think of the circuit with this as input and that as the output it is a source follower, the quiescent voltage here when V C M is 0 is V bias minus V g s of M 1 2 which is a threshold voltage minus square root of 2 times I naught by 2. I can think of

this is each transistor, that is each transistor W 1 by L 1 carrying a current I naught by 2 or the combine transistor carrying a current of i naught, either way that is the quiescent voltage. And when we apply in an increment V C M, there will be some increment in the source voltage, the voltage across the current source. Now, because of the source follower I will assume that the increment is equal to the input, we have earlier analyze the source follower and showed that the increment is not exactly equal to the input it is attenuated.

And in case of the subtract being tied to the MOS negative potential, it is attenuated even more because of body effect, so please take it as an exercise, calculate exactly what happens with the common mode input in this particular circuit. But, I am not going to do that I will just assume that the increment in the source is also V C M and go with the analysis. So, if the increment is V C M, these R naught remember as the incremental resistance of the current source, so the total current flowing into the source as a transistor, this was I naught and it will change to I naught plus V C M by R naught.

So, that is the total current and similarly, the quiescent output voltage was V D D minus I naught R by 2, now we have this incremental current also flowing into the load, so we will have plus V C M by R naught times R by 2. So, the common mode input does have an effect on the output, it has a gain the common mode gain is equal to V C M by R naught R by 2, that is common mode output voltage. the gain will be that divided by V C M, so the common mode gain is R by 2 R naught.

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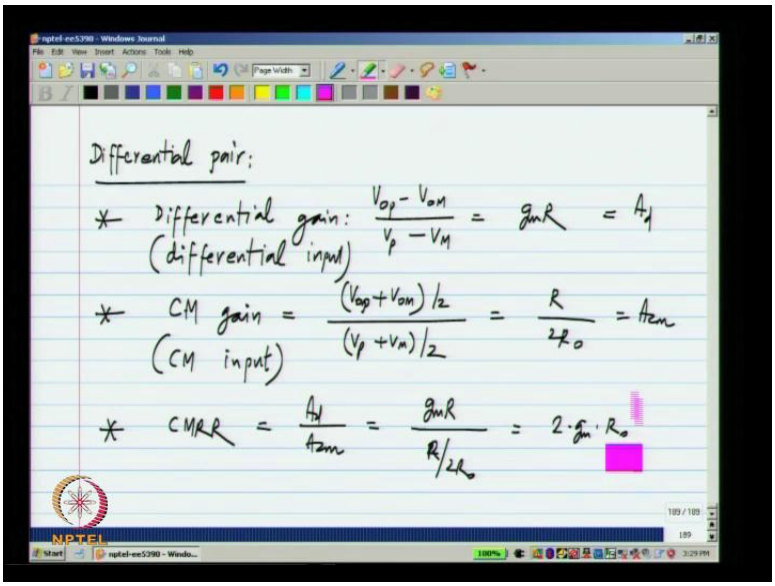

So, it quick summary of the differential pair is that, the differential gain this means that, the differential output the difference between these two divided by the difference between those two. When I apply a differential input only is given by g m R I look at the difference between the two output voltages, and divided by the difference between input voltages this is the gain. The common mode gain which refers to the output common mode voltage which is V o p plus V o m by 2.

Remember, when I apply the same input to the two sides, when I apply a common mode input, the two output fill also be the same as each other, so the average value is the same as the individual output voltages. And this is with common mode input, it is measured with the common mode input and the common mode rejection ratio, which is the ratio of differential gain divided by the common mode gain, let me call these A d and A c m equals g m R divided by R by 2 R naught, which is equal to two times g m times R naught.

You can see that it dominantly depends on the tail current source, the output resistance to the tail current source, so if you want to improve the common mode resistance ratio, you have to improve the tail current source, you have to increase its internal resistance. Now, this is D C analysis, now in many cases the A c common mode gain is also important, the A c common mode rejection ratio is important. In that case the formula will be exactly the same except that the resistance R naught is replaced by an A c impedance g naught.

So, you will have two times g m times absolute value of g naught, and you have to improve the impedance of the current source at all frequencies, if you want to improve the common mode rejection ratio at that frequency. Now, why are we thinking of common mode and differential inputs I have explained this before.

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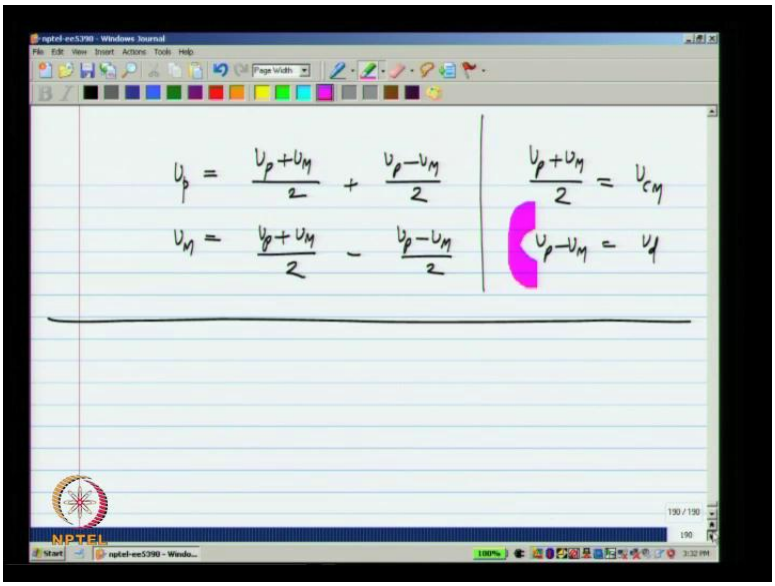

So, any signal let us say, if I we have a pair of signals instead of thinking of independent signal V p and V m, we can think of them as, their average value plus halves the difference and minus halves the difference V p plus V m by 2 is the average voltage or the common mode voltage, and V p minus V m is the differential voltage. We prefer to think of this way instead of thinking V p and V m directly, because in a lot of cases, we want something to happen to the differential signal, usually we want our circuit respond very well to the differential signal, and not respond at all to the common mode signal.

So, because of this we separate the signals into differential and common mode, there also alternative cases, where we want some parts of the circuit to respond only to the common mode and not respond to the differential. So, that is why mathematically the two representations are equivalent, you can represent a pair of voltages as V p and V m or their average and difference values. We prefer to think of them, in terms of the average that is common mode voltage and the differential voltage, because functionally they make more sense.

So, we have symmetrical circuit with a symmetrical load, now this is not yet an opamp, we have to make an opamp out of it, but the this is the circuit that we came up with along the way to synthesizing something that takes the difference between voltages. And this is the very widely use circuit, so that is why we analyze it, now we will try and make an opamp out of this circuit.

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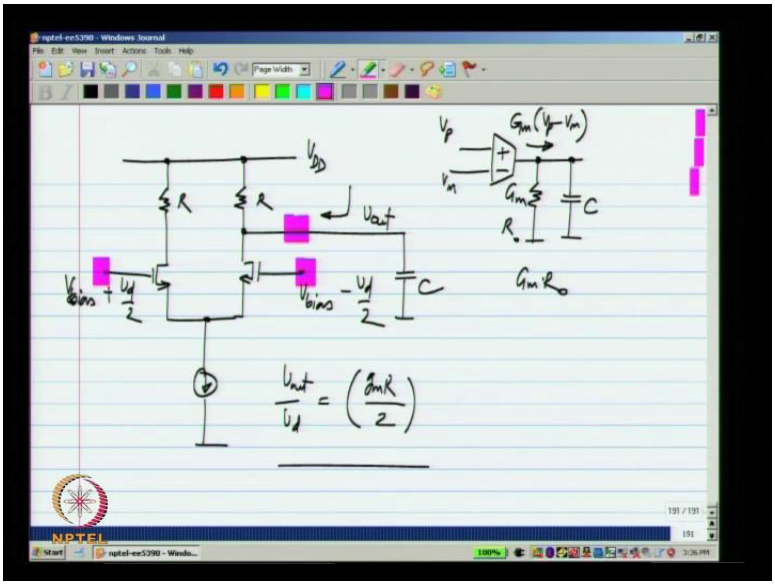

Now, let us say I have some bias voltage on the two sides, and equal and opposite V D by two on the two sides, now what is my opamp circuit, I have some trans conductor that converts the input difference into a current and passes that through a capacitor C. Now, I know that whatever trans conductons I make we will have some resistance R naught, and I would like to maximize this. Now, if you compare this to the circuit that we have, we do have a circuit that takes the difference, and the incremental current in the transistor is related to the difference in the voltage.

Now, the circuit that we have also has an output resistance, and also the way we run the circuit is symmetrical, we want only one output, so we will just take one of the outputs and ignore the other one, that is entirely possible. So, let us say, I take the output only from this side and I could pass this through a capacitor, now I also want the output resistance looking in there to be very large. Now, what is the output resistance going to be, let us assume that transistors have no output resistance at all, they have G d s equal to 0 or R d s equal to infinity.

Now, when you have 0 incremental voltage here, the transistors simply become an open circuit and the resistance looking here will be just this resistance R, it can also be thought of in another way the D C gain of the circuit is g m times R naught, the D C gain of that circuit from this different input to the output that is let me call these V out. V out by V d will be g m R divided by 2, now we know that this can only be only a modest number, because this is the gain of the common source amplifier. And this is only rather modest number that we get, when our supply voltages are limited, to increase this gain value we have to go on increasing the value of R.

But, if increase the value of R that D C voltage drop cross it, I naught R by 2 will go on increasing, so that is mean that we have to increase the supply voltage as well, we keep all the transistors in saturation region. Now, this is prohibit able expansive it is just not allowed in real circuits, their supply will be limited to some extent. So, this is not a way of increasing the D C gain, we cannot make better opamp's using that kind of technique, what we have to do is to substitute the resistance with something else, that will look like very high resistance, but will not demand as much a voltage drop.

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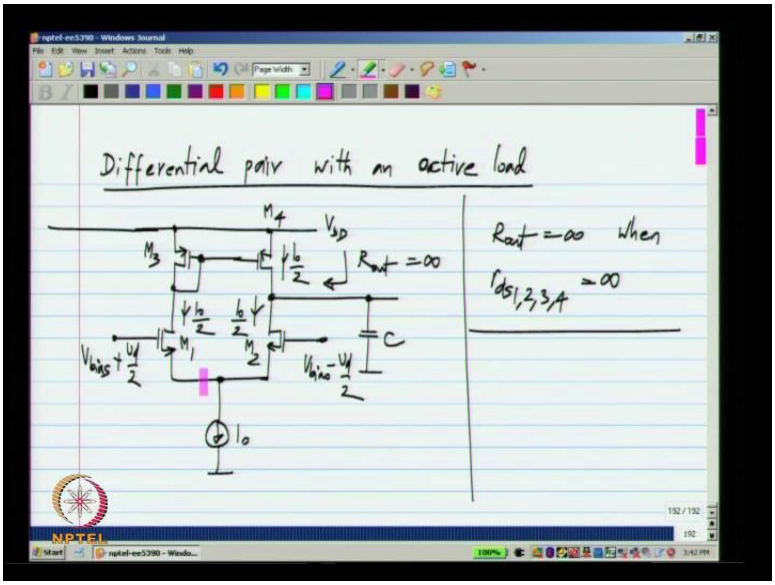

We know that on active load that is using a MOS transistor as a current source, as a very common way of obtaining of very high incremental resistance, while keeping the voltage drop cross it to a limited value. So, if you have transistor in saturation region, so let us say I have to connect a resistance to V D D this is the situation I have in my differential

pair. Now, this can be equivalently done by connecting a p MOS transistor to V D D and insuring that this is in saturation region.

If it is in saturation region, what does this look like its look like an equal resistance r d s, and we know that in saturation region this r d s is rather high, from the output characteristic of the MOS transistor which are very flat and saturation region. We know that the g d s is very low or r d s is very high, and this is a very common way of simulating very high incremental resistance. And the voltage drop across this, it is not related to the resistance value, but it is related to V g s minus V t of the transistor, it is the V g s minus V t of the transistor, so depending on what V g s you bias with you can have a fairly limited value.

So, let me start again with my differential ((Refer Time: 36:13)) pair R and R, now this side is not being used, the left side is not being used I could connected to anything I wanted, and I take my output from here and what I want do is to replace this by a p MOS transistor in saturation region. Now, clearly the p MOS transistor in saturation region must carry a current of I naught by 2 and a convenient way of biasing, could be from a current mirror, where this is I naught by 2.

Let us assume that these transistors R in saturation region and go with the analysis, now this is the way of doing it, but this is also looking particularly wasteful, because we have an extra bias branch of I naught by 2. And we also have a current of I naught in the tail of that differential pair of M 1, m two, so what we can do instead given that the current in transistor M 1 is not used at all. And we also know that in the quiescent condition the current in M 1 is the same as current in the m two, and it is equal to I naught by 2, so what I can do that, so in the quiescent condition, because of symmetry will examine this little more detail.

So, the current here will be I naught by 2, and the current there will be I naught by 2, so this will get mirrored in the current mirror, let me call this M 3 and M 4. And here also will have I naught by 2, we will assume all transistors are in saturation, then what happens is first of all, if you do assume that the transistor has 0 g d s, then the incremental resistance looking into the into the differential pair is infinity. Because, you see that all transistors will have infinite r d s and this is also infinity, and that will be the idle case, when we have a trans conductance with infinite output resistance.

And the opamp behaves like an idle integrator, in reality the transistors will have some g d s and we have to analyze the effect of that, that we are going to do soon. But, this is at topology that can be used, because it gives very high output resistance, as the value of g d s can possibly be, and it converts the input different voltage into a current and drive set out. Now, I said that the currents here will be similar to the currents earlier, that is something that we still have to examine, now it turns out that when r d s values are infinity that is true. The current in each of these transistors will be simply equal to g m times V d by 2, that I leave it as an exercise to you to verify by circuit analysis.

When r d s values are infinity, you please find out the currents in each of these transistors, now when the r d s are not infinity or g d s value are not 0, the analysis concerned will little more tricky, and we have to be careful. And particularly careful, because the answer looks similar to what you get when you assume g d s equal to infinity, but some of the things are different. So, we will spend some time analyzing the circuit both for the voltage gain, and the output resistance and so on.

And also one important thing to note here is that, the symmetry has been destroyed, earlier we said that when you have a symmetrical circuit with anti-symmetrical excitation, we can do the analyses very easily. That was because of linearity in super position the voltage along the center line was 0, now this circuit is not symmetrical, the p MOS side of it M 3 and M 4 are not connected symmetrically. So, we have to be lot more careful and we cannot apply the concept of differential halves circuit directly to this particular circuit.

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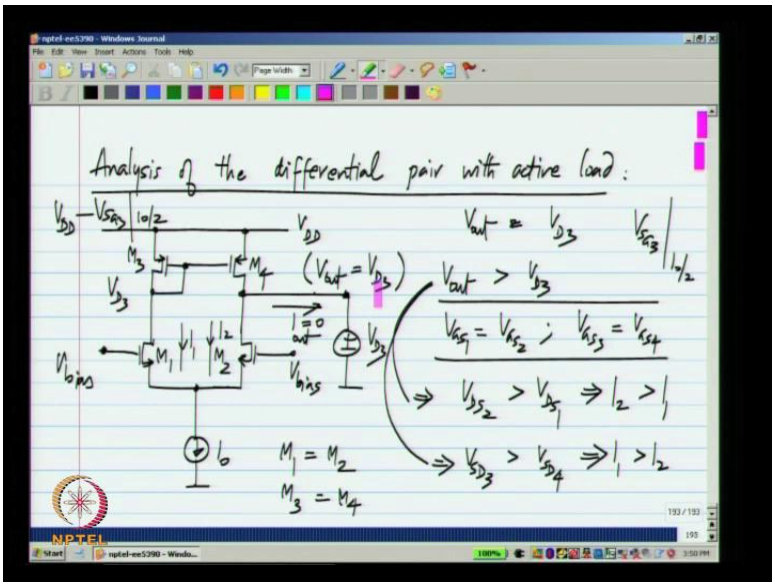

As I mention many times M 1 is identical to M 2 and M 3 is identical to M 4, instead of V p and V m, I will show it as a bias voltage plus differential or common mode increments. Now, the transistor will have some g d s values, in reality they will be there and we have to include that in analysis, and throwing all the equations together and analyzing it does not very useful, we have to get some intuition as well, so that is what we will do. Now, first let us start with the quiescent condition, that is we have only V bias applied to the two sides, and we have a tail current I naught.

And the transistors are exactly identical, in this case we do not assume any mismatch, we assume that the transistors are perfectly matched. And the question is what is the output voltage going to be, this is the output of my differential pair trans conductor, so what is this V out. So, again as usual please pause the lecture or this point and try to reason it out, and you can assume some value of g d s for the transistors and M 1, m two can be consider identical as are M 3 and M 4.

Now, if you through the reasoning correctly you will find that this V out under the quiescent condition will be the exactly the same as that. Let me call this V D 3, so V out will be equal to V D 3, now what do we know the easiest way to prove this is by assuming that, let us say V out is more than V D 3. Now, keep in mind that under the quiescent condition V G S 1 and V G S 2 are equal to each other and V G S 3 and V G S

4 are equal to each other. I have two identical transistors have the same V G S and if their currents are different, the only for that to happen is for the V D S is to be different.

That is if two transistors have the same V G S and one of them has a larger V D S it will also have larger current, and let us assume that V out is more than V D 3, and see what happen. So, V out is more than V D 3 undo the thing of M 1, m two this implies that V D S 2 is more than V D S 1, which in turn employ that, the current in transistor M 2 is more than the current in transistor M 1. Now, if you look at the same thing for M 3 and M 4, the same condition employs that V S D 3 is more than V S D 4, which employs that I 1 is more than I 2.

So, clearly this contradiction and the only consistent solution is to have V out equals V D 3, so when the circuit is perfectly symmetrical, this will be the case and that also means that all transistors will be in saturation, assuming that the V bias is small enough. It very clear that M 4 will be in saturation, because the gate voltage of M 3 is the same as the drain voltage of M 3, and the drain voltage of M 4 is the same. Now, V bias let us assume a small enough, so that M 1 and m two are also in saturation region.

So, this tells you something about quiescent condition the V out equal to V D 3, now what this means is that let us say I connect a voltage source here, which is equal to V D 3. What is V D 3, V D 3 is V D D minus V S D 3 at a current of I naught by 2, I will use this notation what it means is the V S D of transistor of M 3 at a current of I naught by 2, I do not want to keep on writing V t plus square root of I by mu c ox etcetera, etcetera every time, so I will use this notation.

If I connect a voltage source of that value to the output, nothing changes in the circuit and the current here will be 0, because the current balance is between M 2 and M 4 and M 1 and M 3 and nothing flows into the source. But, the output is not incremental in short circuited and will exploit this fact to do, further analysis of our differential pair. So, what we have done is to look at ways of analysis of fully symmetrical circuit, which symmetric and anti symmetric excitation that gives you common mode differential halve circuit concepts.

And we also came up with the circuit for obtaining a high gain while taking the difference between the input voltages. And that is the differential pair with the active current mirror load, but this circuit is not symmetrical and if you throw every aspect of

the circuit into the analysis, we will get no intuition at all, so we will proceed step by step. First we uproot that the operating point by itself will be identical, and this also means that I can connect an output voltage of some value, which I know that is equal to V D 3 and nothing will change in circuit; using this we will analyze the differential pair in more detail in the next lecture.

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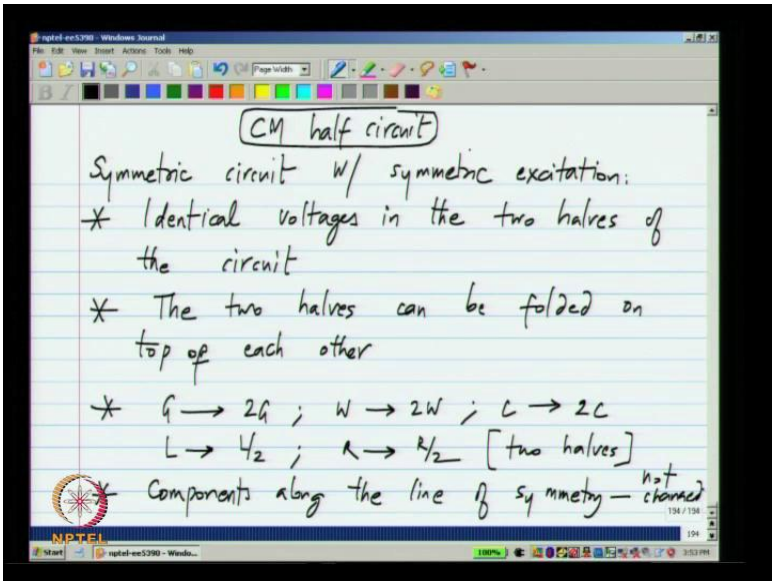

Now, just quick summary of what we read today, we will have identical voltages in the two halves of the circuit, so this means that basically the two halves can be folded on top of each other. So, this means that all conductance will be doubled, all Mosfet to it will be doubled, all capacitances will be doubled, the capacitances which are repeated on both side the Mosfet which are repeated on both sides and so on. And similarly, the inductance will become halves and resistances will become halves and so on, these are the components in the two halves. And the components along the line of symmetry, these are not changed, and this gives us what is known as the common mode halve circuits, which is considerably simpler than the original circuits, and also considerably easier to analyze.

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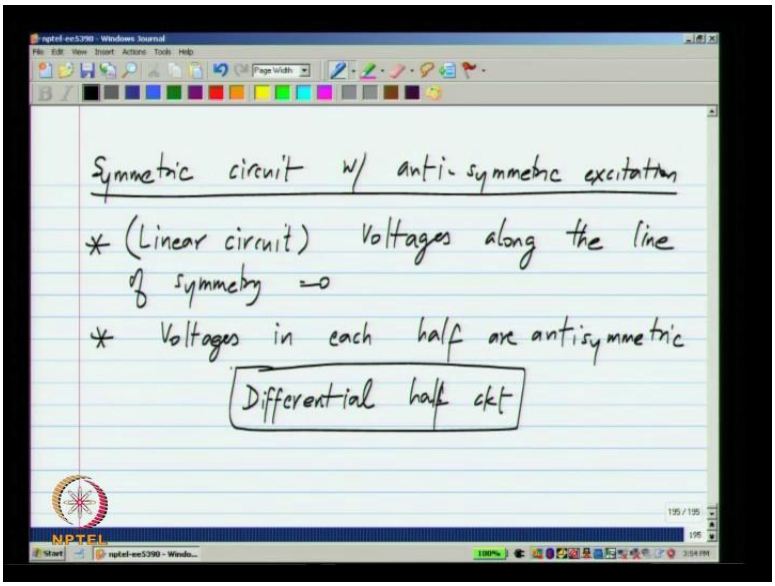

Now, let us say we have symmetric circuit with anti-symmetric excitation, so if the circuit is linear, which could be a linear circuit by itself or the small signal equivalent of a non-linear circuit. The voltages along the line of symmetry, and the voltages in each halve an anti-symmetric, this gives you the differential halve circuit. So, you analyze only halves the circuit by tying all the voltages along the line of symmetry to 0, very useful technique when you have fully symmetrical circuits, we will continue from this in the next lecture.