Analog Integrated Circuit Design
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Lecture - 27
Basic Amplifier Stages- Common Drain;
Frequency Response of Amplifiers

Hello and welcome to lecture 27 of Analog Integrated Circuit Design, we were looking at the consequences of body effect in basic amplifies stages, we looked at what happens in common source amplifier, which is nothing. And in a common gate amplifier, which is that g m b gets added to g m, today we look at what happens to common drain amplifier or the source follower.

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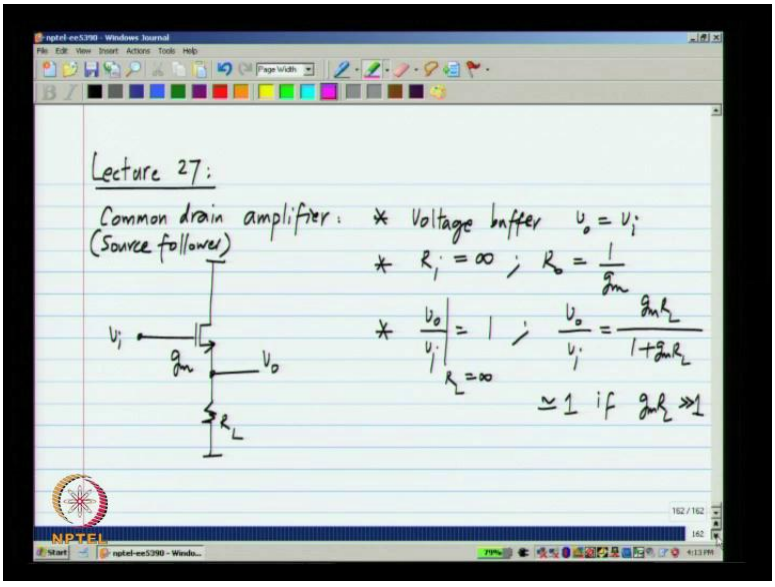

Now, the common drain amplifier is one, where small signal input is applied here, the drain is that small signal ground and output is taken from the source, and there will be some load resistance r l. The small transistor will have certain g m, now what is supposed to do it is a voltage buffer, whose output voltage equals the input voltage that is what it is ideally supposed to do. Now, what is the use of something like that it presents high input resistance, r i is infinity looking into the gate, but typically the bias network that you have will dominant the input resistance and R out equals one over g m.

So, this is what is the case, and the gain v naught by v i equals 1, if r l equals infinity now as you are aware v naught by v i will be g m r l by 1 plus g m r l, for some r l that is

not infinite. So, the gain, in fact is less than 1, it is not equal to 1, but it can be approximated to be 1, if g m r l is much, much more than 1, so the common drain amplifier are the source follower is operated in this condition usually. Now, what happens in presence of body effect, let me write the small signal picture, this is small signal source g m times v g s, and there is this small signal conductance g d s.

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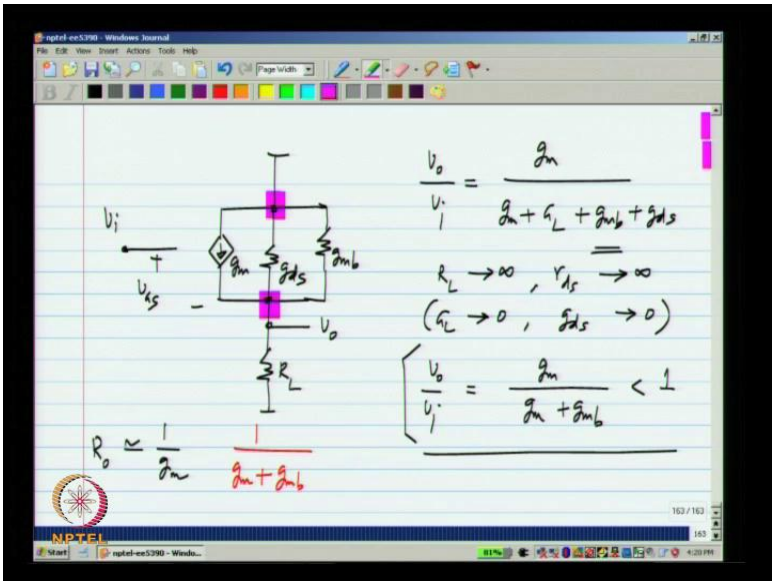

And also the small signal source g m b, which multiplies the voltage v b s and the bulk is at ground, the bulk is always at ground, because specially with n most transistors, they are connected to the lowest potential to the circuit, which is a fixed voltage. And the resistance r l is over there, by the way these expression here are excluding g d s, if we include g d s they get modified slightly, but g m is much more than g d s for any reasonable operating point.

So, we can ignore that, if we do include g d s what happens is the output resistance changes to 1 by g m plus g d s which is small modification and also you see that the g d s, which appears here is simply across r l. So, in this formulae as well v naught by v a, which could be rewritten as g m by g m plus g l, we also have g d s, because g d s simply is an additional load. This is a small modification not very significant, now let us come back to the effect of g m b, now what is the effect of g m b, the input v i is applied there.

We can write the equations and solve for this, again as usual i encourage you to do that and make sure that the answers are consistent with what I say here, but again I leaves a

shortcut. Now this g m b is proportional to that voltage the voltage between that point and ground, and you also see that the control source g m b is also connected between this point and ground.

So, the controlling nodes of the controlled source g m b, v b s is the same as the nodes between, which the controlled source is connected, and you very well know that, if you have voltage controlled current source connected between the same nodes as the controlling voltage it can be represented by an impedance. So, this g m b which is connected between the source node of the MOSFET and ground is controlled by the same voltage, I will call it v b s, like this is more convenient to think of current flowing upwards.

And this being v s b, that is basically this voltage with respect to ground, so this current source is not invert, this is g m b times v x, and this is equivalent to a conductance g m b. So, in this particular circuit I can replace this controlled source by conductance g m b this is only, because in this circuit the controlling nodes and the controlled current source nodes are the same.

So, this is now very easy to analyze, because we already done the analysis all we have to do is to add g m b in parallel with the load conductance, so v naught by v i trans out to be g m by g m plus g l, which is what we had originally, plus the extra conductance g m b plus g d s. So, the significant extra term is this g m b that appears in the denominator, now what is the effect of this I already mentioned that g m b can be significant fraction of g m.

It could be one third or one fourth or something like that whereas, g d s is really small fraction of g m, and that also can be adjusted by adjusting the length. So, that the g d s reduces whereas, the ratio of g m to g m b is something that is fixed, it is a sort of property of the process that is use to make the MOSFET, we saw that it is g m times the derivative of v t with respect to v s b. And that is something that is related to the doping in the transistor and so on, so it some fraction of g m.

So, even with r l tending to infinity and r d s tending to infinity with basically means g l tends to 0, and g d s tends to 0, the gain of this source follower will not approach 1, but it will be g m by g m plus g m b, which will be less than 1 by a significant number. Now, this is one of the reason why source followers are not extremely popular, you use them

and you have to specially because when you have an n m o s transistor, in at final process that is you have only common piece of straight for all n m o s transistors.

You do not have any freedom in connecting the sub straight, it has to be connected to the lower potential some fixed voltage. Now, the source follower by definition will not have the source at ground, it is at the output voltage, so it will suffer from body effect, which has the gain less than 1. So, it is not all the great buffer, when you make it with n m o s transistor, if you are able to tight the bulk to the source the situation is different.

And that can be done normally with PMOS transistor, as we will see and if you have trivial process which has isolated n m o s transistor also you can do it, now that brings with the its own disadvantages, but at least it can be done. The main consequence of the body effect in the source follower is that the gain will be less than 1, it has no influence on the input resistance the output resistance will be modified, but in a good way R o, which is approximately 1 by g m.

If I neglect the g d s will change to 1 by g m plus g m b, in fact the output resistance of a source follower or a common ray an amplifier is exactly same as the input resistance of a common gate amplifier. It is measure between the source and ground with the gate being at small signal ground, so just as the body effect imbrued the small signal input resistance of common gate amplifier, it imbrued the output resistance of a common drain amplifier.

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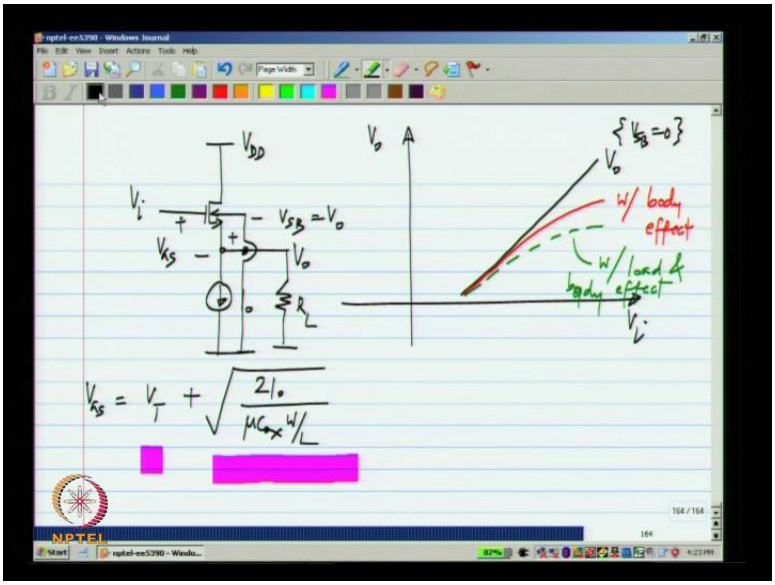

Now, there is another way to think about the gain of this source follower being less than 1, for that I will use the large signal picture, I will assume that there transistor is bias at the some fixed current I naught. I apply a large signal v i here, I will try to plot v naught versus v i, and notice that I have not put any load to the source follower, which means that its operating in the best possible condition with an open circuit load.

Now, what happens lets an increase the input from very small values some value, so the input itself would increase like that, now what will this voltage be it is v i minus v g s and v g s is nothing but, the threshold voltage plus square root of 1 I naught by mu c ox w by l. So, that is the fixed offset if the threshold voltage is fixed, so the output volt simply follow the input, and that is why it is called a source follower, this is the output, that is what input do.

Now, what happens in reality when we have the bulk connected to the source, this v s b is nothing but, the output voltage itself with respect to the ground, now as the output voltage tends to increase, the threshold voltage also increases. So, the difference between input and output voltage is starts becoming larger and larger, for what we will see is that with body effect, we will have something like that.

And this will be the case with v s b equal to 0, now this can be arranged by time the bulk to the source, so now, as you go to higher and higher voltages, you have a larger gap between the input, and output and the output does not follow the input anymore. Now, in the addition to this, let us say you also have a load resistance what happens as the output increases the current through the most transistor increases, so not only does v t increase, but this part also increases.

So, you will have an even worse situation, you will have something like that, so this will be with load and body effect, so the source follower is not all that creative buffer. The emitter follower the counter part with bi polar transistors works very well and it choose very widely, now in load at CMOS technologies this gap between the gate and source is too much should tolerate in addition to that with n m o s source followers you have this constrain of body effect.

So, it is not use all that often, now this comes into play initially, when we design the opamps we designed it using trans conductors and said that we can put a buffer at the output in order to reduce the loading and isolated the load from the trans conductor, but

to be see that most often in the CMOS opamps are made without the source follower buffers, and it is for this reason.

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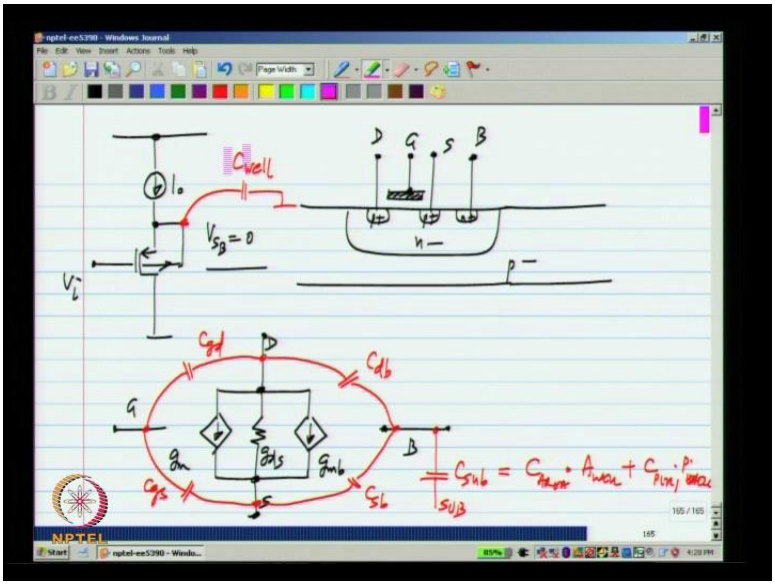

Let us say the PMOS source follower, we will assume that the PMOS is made inside an isolated annual, now seems this annual is not shared with other transistor, I could tie the bulk anywhere I want. So, let us a make a PMOS source follower apply v i here, the bias is, so that constant current I naught that tie it there, and this is a way of avoiding body effect because this guarantee is that v s b equals 0.

Now, it turns out that this is, but this brings with it problems of its own, when we look at high frequencies, so for we remote the 3 amplifiers at d c, we do not take into the account any capacitance of the device or partially capacitances or lets also look at that. Earlier, we have learned that the small signal model of a transistor is this, this is the 4 terminal small signal model with that drain, gate, source and bulk, and this part is the same for n and PMOS transistors.

This is a current source g m v g s, this is g m b times v b s, and this is g d s, and when we added the capacitance, we saw that there was a capacitance between this terminals. There was c g d and c g s due to overlap as well as channel search, and there was c d b and c s b due to reverse bias junctions, and also there is one more important thing that, because this annual is made on this common substrate. And also you see that the size of the

annual is larger than the size of the PMOS transistor, in PMOS transistor made inside an annual there is also a capacitance to substrate.

This is the bulk of the PMOS transistor, this is the common substrate of the integrated circuit, I will call it c sub and just like we model these junction diode capacitances with some area capacitance and perimeter capacitance. C sub will also be classified by some c area, which will be different value from c area of the drain or source partially capacitance, but it will have some unit area capacitance, times the area of the bulk plus c perimeter times the perimeter of the bulk.

Now, you see that because this annual is quite large this area is quite large, and this capacitance can be significant, when you tie the bulks together to some common potential, let us say v d d or ground PMOS bulks would be tight to the highest voltage,. and n m o s to the lowest voltage. If you choose to tie to a common voltage, then capacitance does not come into picture, because it appears between 2 fixed voltages v d d and ground, and it does not really do anything.

And in this particular case, when we have tight the PMOS bulk node PMOS substrate to its source, we will have this will capacitance between that point and ground, the substrate is common ground of the circuit. So, this is c value, so essentially we have an additional loading, which is c well and that can also be a problem, this is not to say that you cannot use PMOS source follower with its source tight to the substrate. You can, but you have to be aware that you have an extra capacitive load, now just for completeness, we will also analyze these three amplifiers with small signal parasitic capacitances.

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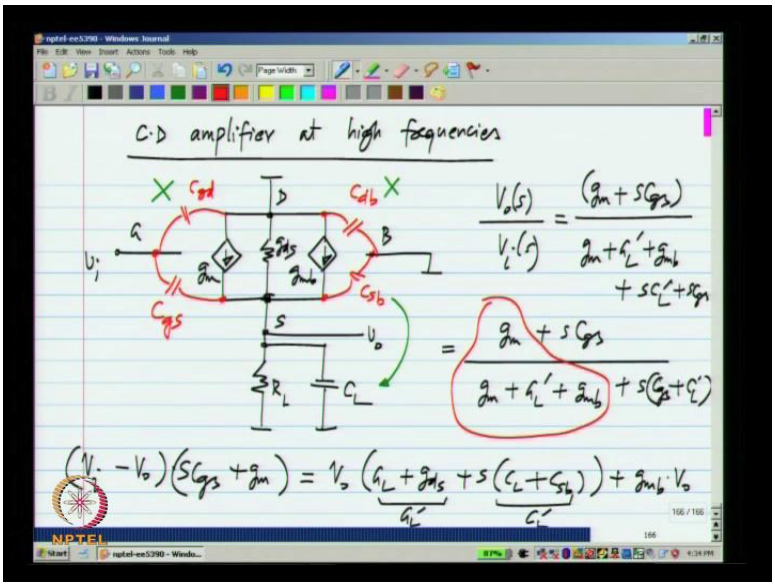

Since, we are talking about the common drain amplifier, we will continue with that what is the small signal model of the common drain amplifier, we have that transistor model. This is the drain, source, bulk and gate, I will start by assuming that the bulk is tight to ground, and this is the model for both PMOS and n m o s common drain amplifier or source follower. I will assume that there is some load capacitance, now that transistor capacitance will also be there, there is c g s, c s b, c d p and c g d.

I will assume that the input is driven by an ideal voltage source, this is not always the case, in fact because this is the buffer many times it is not driven by an ideal source at all, but I will just assume that. So, if we drives this with an ideal voltage source, the c g d simply appears across the input, and as no effect that can be ignored, this c d p appears between drain and bulk which are both a small signal ground, so that can also be ignored.

The c s b appears in parallel with c l, so it can be absorbed into c l, so your actual c l will be the load capacitance that you connect plus c s b, and you have this c g s which appears between gate and source. So, we really have only this two capacitances to worry about, now just for practicing circuit analysis please all the lecture at this point, and calculate this small signal v naught by v i, and when I say small signal v naught by v high frequencies, I mean that in the low class ((Refer Time: 20:25)).

What will that be very easy to calculate, we have only one node the source node at which we write Kirchhoff's current law and calculate, so that k c l equation there will be v i

minus v naught times c g s that is due to this, plus g m due to that one. That is the total current coming into this node, and I will sum everything into the current going out of that node, which is v naught times g l plus g d s plus s times c l plus c s b.

As, I mentioned earlier g g d s could be absorbed into g l and c s b into c l, so let me call this g l prime and c l prime for simplicity of notation a naught of s by v i of s will turned out to be. Now, because this g m b acts like a conductance, this expression should also contain g m b times v naught, so this was explain earlier I had omitted while writing this expression that is also there.

So, v naught of s by v i of s is g m plus s c g s divided by g m plus g l prime plus g m b plus s c g s plus c l prime, so again there is an s c g s the d c gain this part is exactly same as before. As usual anytime, you calculate a transfer function, you do a sanity check and make sure that it make sense, now this transfer function has a single zero and a single pole. Now, this we could have predicted right from the beginning, because we have only to capacitors of consequence that is c g s and c l, c s b is the same as c l, it appears in parallel and also we assume that the input is driven by an ideal voltage source.

So, we have a loop of a voltage source, and these capacitors the input voltage source c g s and c l, so this means that there is really only one independent set variable, so the order of the system is 1. Now, we could also guess there would be a 0, because there are 2 paths to the output with different frequency dependences from the input, one is through the gate source capacitance c g s, and the other one through the trans conductance g m, so that is why we get g m plus s c g s.

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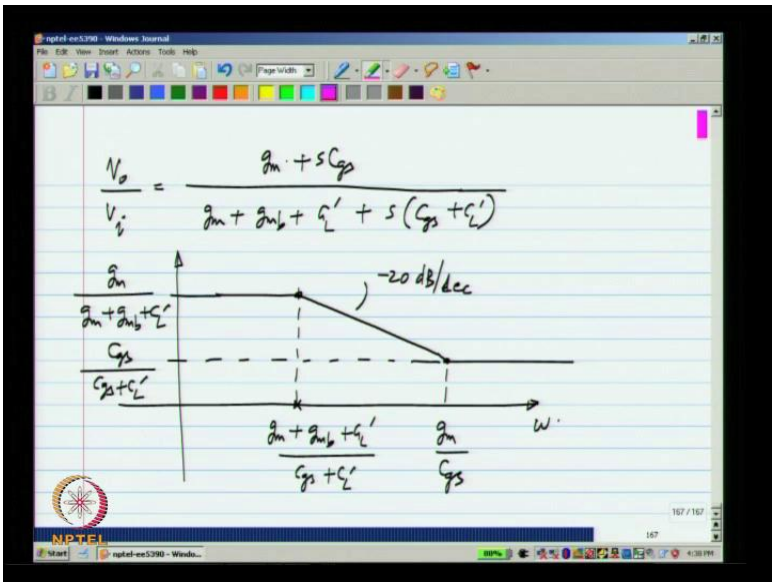

So, when you make a source follower you can expect, that they will be one pole and the zero when driven by an ideal voltage source, when you drive with a non ideal voltage source you will end up having more than one pole. If I draw the broad a magnetic product of this, what it will look like, at low frequencies the gain will be g m by g m plus g m b plus c l prime, and they will be a pole at a frequency given by this conductance divided by that capacitance, and after that the gain drop of that minus 20 d b per decade.

At high frequencies as you can see when s c g s is dominant over g m, and s times c g s plus c l prime is dominant over that, we will have again frequency independent ratio c g s by c g s plus c l prime, and the frequency of the 0 is g m by c g s. Now, what does this really mean at very low frequencies, it is act though the capacitance are not there, whatever d c analysis we did earlier will hold, and the gain will be g m by g m plus g m b plus g l prime.

Now, what happens at high frequencies the currents through the capacitors will dominant over the currents through the conductance's and trans conductance's, so what will we have we effectively will have only the capacitance c g s between the input and the output. And a capacitance c l prime from output to ground, so this is a capacitive divider, and the ratio v naught by v i is; obviously, c g s by c g s plus c l prime and that is what we see here.

So, again when you sees a mathematical result, it is always good to go back to the circuit and make sure that that make sense, so at low frequencies it is look like the source follower in d c condition. At high frequencies it is look like capacitive divider, and both have frequency independent ratio so; that means, that there has to be a pole and a 0, and that is what we see from the analysis of the transfer function as well.

So, the result make sense that is what is important, and you can see that if you have to drive a very heavy capacitive load, your band width will end up reducing, because c l appears in the denominator of the pole frequency. Now, alternatively if you want to drive a very heavy capacitive load with a very high band width, it means that the value of g m has to be very large, and which consequently means that the power dissipation has to be very large.

Now, earlier while discussing opamps I said that you can guess, whether there is 0 or not in the transfer function, it is not as easy as with poles with poles with most of the common circuits you will end up having isolated r's and c's, which you can pair. And look at what conductance appears across what capacitance, and by taking the ratio of conductance to capacitance you can estimate the poles, with 0's it is a little more difficult, but now we can look at how we can try to estimate that as well.

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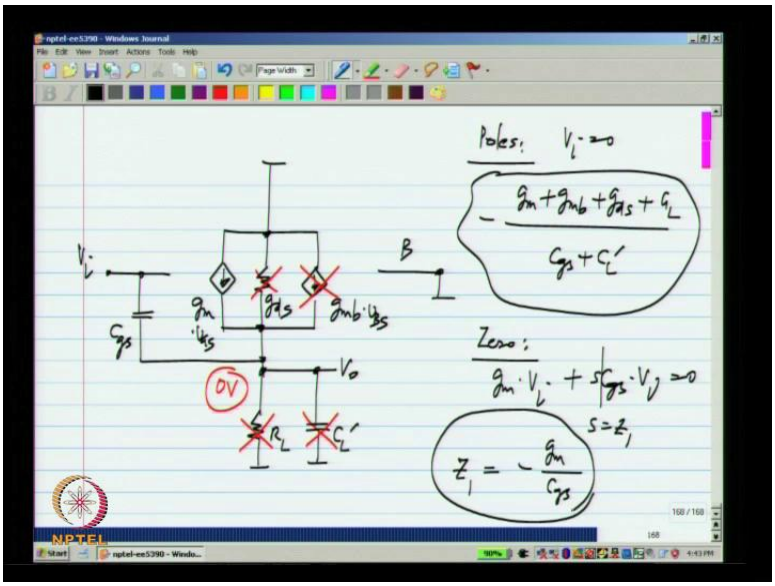

So, first let me put down the small signal circuit, again I will club everything in the c l prime, and I will not include the irrelevant capacitors c g d and c d b. First of all to

estimate the poles, we could do this before I did the analysis, and in fact that is a very good practice, before you do the full blown analysis look at the circuit. And look at what the result should be, and then do the analysis and reconcile the two this will build both your analysis, and intuitions kills.

The intuitive answers that you get, before you do the analysis will serve as sanity check, and the analytical skills will fixed any false in the intuition that you may have, because of lack of experience. As, you get more and more experience, you should be able to answer pretty much any question about any circuit intuitively. Now, for poles, which are the characteristics of the system, and not the input or output we said v i to be 0, and if I do that what do I have, I have a single capacitor c g s and c l, appears in parallel.

And what is the conductance that appears across, it see that because this is grounded, and that is grounded, and this is grounded, and this is g m b times v b s and this is g m times, the v g s both this controlled sources are across the controlling nodes, which is this point and ground. So, this contributes a conductance g m, this contributes a conductance g m b, additionally you also have g d s and g l.

So, the total conductance is g m plus g m b plus g d s plus g l and of course, the pole is in the left half plain, so that is where the pole is. Now, one thing to keep in mind while talking about circuits it is very common to talk about poles, as though they are a positive quantity now for any stable circuit the poles will be in the left half plain, but because in the board a plot.

We the bandwidth of a first order system turns out to be the pole, and that is the positive quantity, you very commonly hear thing like the pole is at some quantity which is positive. It really means that usually the pole is in the left of plain, but we are only referring to the magnitude of the pole. So, earlier when I said that pole is at g m plus g m b plus g d s plus g l divided by c g s plus c l prime, that is the logic that I was using, now what do I do about the 0, first of all, because we have two paths from the input to the output.

V i minus v naught times c g s and v m minus v naught times c m, we can guess that the pole is at g m by c g s, there is also another thing you can use. Now, what is the zero after all its the value of s, at which the output becomes 0, so let us assume that the output is 0. Now, what happens then we have 0 volts across r l c l prime, and g d s, and also v b s is

0, assuming that the source potential is at 0, so we have currents possibly only through this two components c g s and g m, and k c l still has to be satisfied with all this other currents being 0.

So, what does that mean g m times v i plus s c g s times v i should be 0, and this is true when the value of s equals the 0 value, so what does this mean, now the 0 g 1 is at minus g m by c g s. It is also in the left half plain, 0's by the way can be in the left or right half plain, they do not influence stability, there is no implication on stability if the 0 is on the left or the right half plain.

And this is exactly the answer we get from the transfer function as well, so when you see any circuit, you first try to solve for it imperatively try to guess set the answers. It is not always possible sometimes thing may not be isolated things may be coupled in a complicated way, so for that you do need the analysis, and when you do the analysis you reconcile them and see, where you have gone for.

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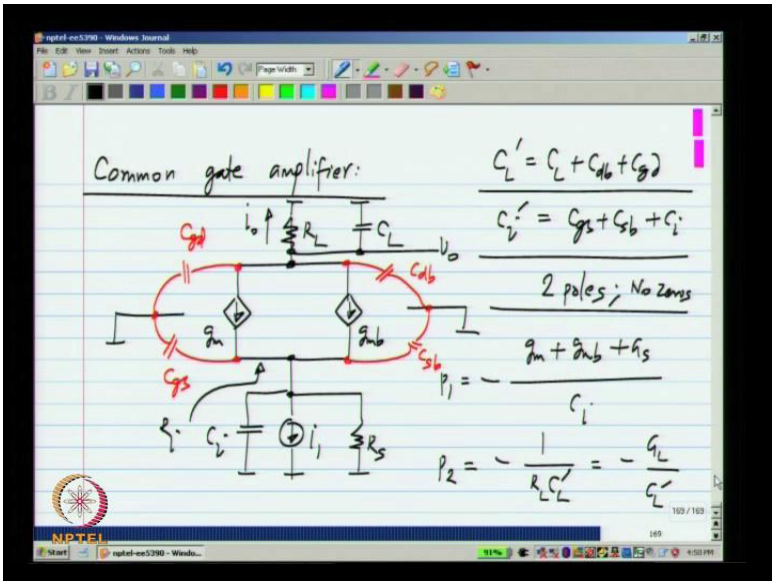

Now, let us move on to the common gate amplifier, in this case the gate is grounded, and we have g m g m b and g d s, and we have some load, which I will assume to be a resistance, I have an input current here. And, which has an in internal resistance r s i could also have load capacitance c l, and then I will add the device capacitances, which are c g d c g s c s b and c d b.

Now, very clearly c g d and c d b can be observed with c l, and c g s and c s b can be observed with the impedance in parallel with the current source. I will call this c i, it may have some capacitance due to the current source itself, but I will just assume that its due to c g s and c s b, and if I do have some capacitance c r c i the c i prime will be including that one.

Now, it answered that the expressions are quite complicated in presence of g d s, and also they do not lend to much inside, because g d s is rather small and usually the effect can be ignored. So, I will do the analysis assuming that there is no g d s or g d s equals 0, now in this particular condition again you can do the analysis, and please do it please put the Kirchhoff's current laws at the two nodes.

And then find the expression I naught by i, where I naught is the load current in r l, alternatively you can also find the output voltage across r l divided by I i, they will be related by some simple factor v naught is simply equal to I naught times r l. So, either case you will find some poles, and possibly 0's and you can reconcile them with the intuitive results, that I discuss here, now first of all how many poles and zeros will there be, how many poles will there be.

Now, in this circuit there are two capacitors c i prime and c l prime, there are many, but they can be observed into parallel combinations and finally, there are only 2 c i prime and c l prime. So, there will be at most two poles, and the ((refer time: 36:12)) do not form a capacitor loop or loop of voltage sources and capacitors, so there are really two independent state variables.

So, we will have two poles and what about zeros, now it is not very obvious, but we do not see path from the input to the output with different frequency dependences. From the input to the output, there are only two voltage control current sources, which are g m and g m b, and they simply appear in parallel, as discussed earlier I can replace them with a single control source of value g m plus g m b.

So, I expect two poles and no zeros, where will the poles be I look at the capacitance v i prime, which is between the input node and ground, and I look at the resistance that appears across it. What is that it is nothing but, the input resistance looking into the circuit in parallel with the conductance g s, so one of the poles will be simply the input conductance which is g m plus g m b plus g s divided by c i.

And of course, the pole will be in the left half plain, this is the pole due to the input node, usually when you have a circuit with many nodes, with each nodes you can associate a capacitance and typically a pole with that node. Now, where is the other capacitance that is c l prime from the output node to ground, and what is the conductance that appears across it, it is just g l prime, so the other parts are isolated due to this g m and g m b.

That is if I apply 0 input current, this voltage will be zero, and these two current sources will be inactive, I am left with only r l and c l. So, the other pole due to the output node is minus 1 over the r l c l or minus g l by c l prime, where c l prime is the total capacitance of the output. Now, in this circuit the input parts and the output parts are isolated, and we have two poles and the transfer function can be written as.

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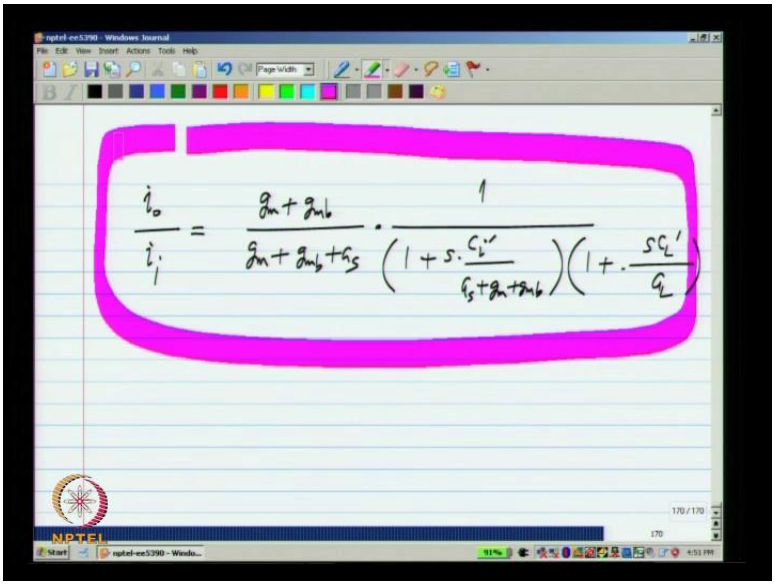

Let me write I naught by i i that will be simply the d c value, which is approximately 1, it is not exactly one it will be g m plus g m b divided by g m plus g m b plus g s times 1 plus 1 plus s c i by g s plus g m plus g m b, that is one of the poles times corresponding to the one of poles and s c l prime divided by g l. So, that is what we will have, so please do the full blown calculation and verify this, you can also do the calculation including g d s and find out the conditions under which, g d s is negligible.

One of the advantages of the common gate amplifiers is turns out that, basically the input and the output parts are isolated, that is we have some pole at the input and some pole at the output. And there is really no interaction between the two, because there is really no

component, between the drain, and the source no impedance connecting there drain and source directly, there are only controlled current sources, which becomes open circuits if the controlling terminals are zero.

They are truly isolated now there is g d s between them, so that causes some coupling, but unlike in other amplifiers in the common drain amplifier, we have c g s connecting directly from the input to output and in the common source amplifier, which we will see shortly. There will be c g d connecting the input to output, the input run output run as well isolated, where as the common gate amplifier they are isolated. So, one of the reasons you use the common gate amplifier is for isolating the input from the output, the details of that we will see later.

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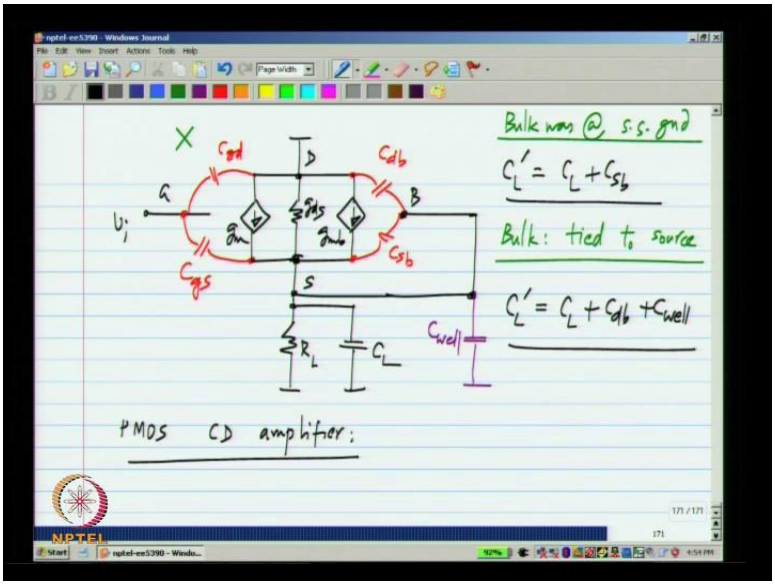

Let us consider a PMOS source follower or a common drain amplifier, the result will be exactly the same as the n m o s common drain amplifier that we derived earlier. If the bulk is tight with fixed potential, but like I said to avoid body effect and reduce the attrition of source follower, you could connect the bulk to the source directly. Now, this does not cause any fundamental change in the analysis, previously c l prime was equal to c l plus c s b, and c g s add no effect and c d b had no effect, this is when bulk was at small signal ground, now the bulk is tied to source.

What happens now, first of all c s b is assorted, so it has no effect and my c l prime will be c l plus c d b c d b can no longer be ignored, and also as I mentioned from the bulk to

ground they will be the well capacitance that has to be included. So, that is all the difference all the expressions that I evaluated earlier will be valid, if you change the definition of c l prime and the important difference is that you have this rather large well capacitance being added to c l prime.

And I already remarked that the bandwidth of the source follower is related to c l prime, it is inversely proportional to c l prime. So, when you have this large well capacitance, you will have a smaller bandwidth, that is one of the problems. I mentioned earlier that you could connect the PMOS bulk to the source, and use it as a source follower without at dimension, but the problem will be that you will suffer from lower bandwidth.

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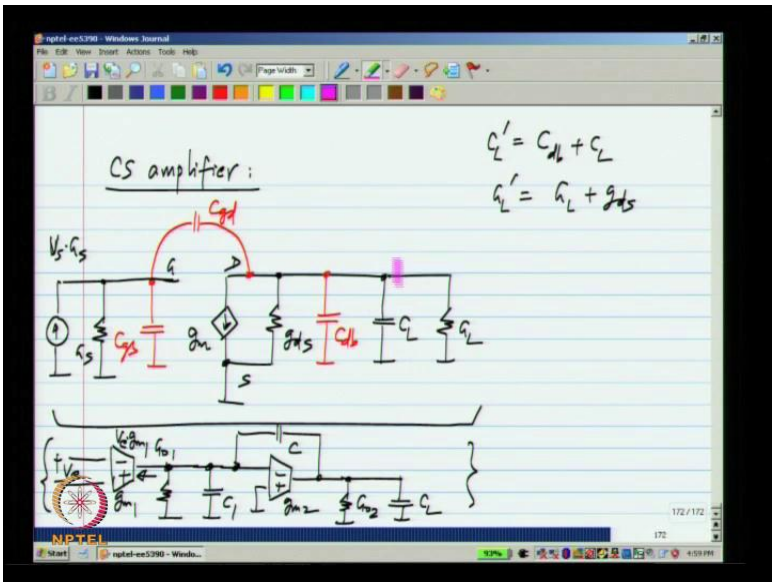

Finally, let us go to the common source amplifier, and the common source amplifier including the transistor parasitic, now because the sources at ground and bulk is also at some fixed potential. We do not have any effect due to g m b, and I will not even include that in the figure, so I have only g m and the input is applied here, I will assume that it is applied, from an input source with the source resistance r s.

And there is this g d s and to that I have some load capacitance c l, this is what I load the common source amplifier with, I also have a load conductance g l. Now, if I include the transistor parasitic, I will have c g d between gate and drain, this is the gate drain, and this is the source, I will have c g s over here, and I will have c d b over there. As usual, I

can observe c d b into c l and for my single load capacitance c l prime, and then I will effect this two capacitors, I can also absorb g d s into the load conductance.

Now finally, it turns out that this analysis is lot easier, if I convert this into an not an equivalent circuit with a current source, v s times g s and an impedance g s. Now, we can analyze this, but first you see that this looks very much like the analysis of the amplifier, we did that boost as mineral opamp that we did. What did we have in the boost as mineral opamp, we had a trans conductance g m one its output conductance g o one and some capacitance c 1 here.

And we had a trans conductance g m 2 with this polarity; that means, that if this voltages increases some current would be drawn into it, and that is exactly the polarity with which we have the g m of the common source amplifier. We had a integrating or compensating cap see over that, and we had g o two which can also stand in for the load conductance g l, and we had a load capacitance c l. This was the circuit that, we had now you see that it is exactly the same as this one, the trans conductance g m one is replaced by this source v s g s that is all.

So, we have to modify the source, in case of the opamp, if the error voltage we v e was there the current would be drawn, so that is would v e times g m 1, in this case v s times g s is being pushed into this node. So, that will simply inward the polarity, but otherwise its exactly the same this, g o 1 is like g s c 1 is like c g s c is like c g d g o two is like g d s and this c l like this c l prime this g o 2 is like g d s plus g l it is the total load conductance.

So, because we have already analyze this, I am not going to do it again, first I will just intuitively say that, how many poles do we have and zeros do, we have you may recall the result you. And if you do not you see that there are three capacitors in a loop, so there will only two independent capacitor voltages or two independent state variables. So, the order of the system is two, and also you have two paths from the input to output with different frequency dependences, ones through c g s and other through g m. That you expect will give you a 0, exactly what frequency it is we will see, in fact what we will do is simply borrow the analysis that we did. So, far for the common source amplifier, and substitute the terms and see how exactly, this behaves.

Thank you, I will see you in the next lecture.