Analog Integrated Circuit Design
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Lecture - 23
MOS Transistors - Mismatch, Speed

Hello and welcome to lecture 23 of analog integrated circuit design. In the previous lecture we discussed the mos model in great detail. We looked at the large and small signal models and at the end of the lecture we were looking at a description of mismatch of MOS transistors. We could describe the mismatch and MOS transistor by two parameters- mismatch and the current factor data and mismatch in the threshold voltage VT. Now, in this lecture, what we will do is look at how to use these parameters to calculate whatever we want in a circuit. We will take an example circuit of a current mirror and calculate the amount of mismatch. We will take the simple example of a current mirror, I am sure all of you are familiar with this.

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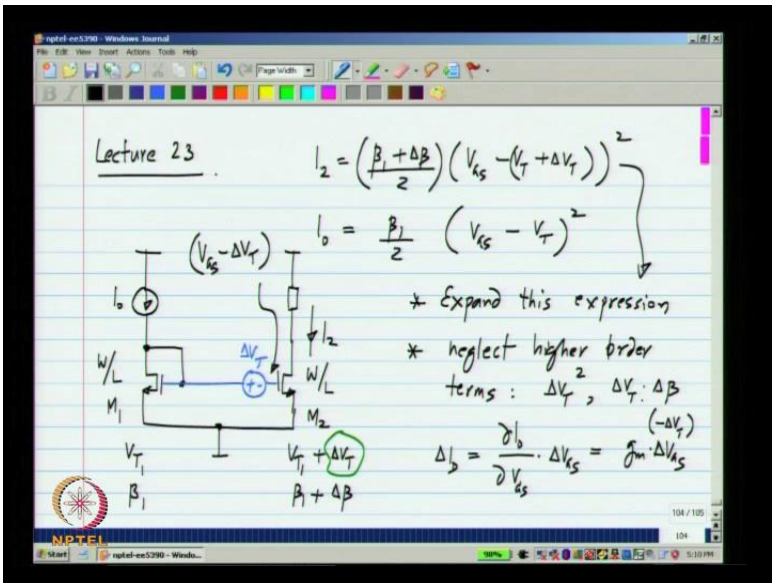

We have a diode connected transistor M 0 and M 1 here and we will assume operation saturation reason and negligible dependence on VDS, so that the current here is normally identical to I 0. Now a current mirror is a perfect example with feast to do mismatch calculation because a current mirror after all is suppose to replicate the current exactly. So, any error due to mismatch will contribute to error in the output and will be of some

concern. We have see how to control the amount of mismatch, so that the output is within a certain accuracy of the input current. Obviously, I have assumed that each of these has the same size W and L.

Now, how do we describe the mismatch in the MOS transistor, if this has VT one, the second transistor has VT one plus delta VT and if M 0 has a certain current factor beta 1, this has beta 1plus delta -beta. So, the current in the second transistor is given by let me call this change in the notation here, let me call this M 1 and M 2 and I will call this I 2. The I 2 is nominally equal to I 0. There are many ways of calculating this, we know what VGS is based on beta 1 and VT one and so on and the current I 0. So, I 0 is nothing, but delta 1 by 2 VGS minus VT square, now there are many ways to calculate this.

You can expand this expression and the key to any mismatch calculation is to neglect, second and higher terms and keep only first order terms of the mismatch quantities, so that means that we will if we have terms like delta VT square or delta VT times delta beta that is coming in, we will neglect all those things and will consider only terms containing either delta beta or delta VT. This is because the mismatch itself is assumed to be a relatively small compare to the nominal value and that is the normal condition anyhow.

So, this is a good approximation. Now, when you do this what happens is because we retain only the linear terms, we get something related to delta- beta and something related to delta VT and a linear combination of the two, if we recall how the small signal models and small signal analysis was derived it is by retaining first order expressions only in the incremental quantities. If we have a circuit with a number of voltages and increment all of them in the small signal approximation you neglect the squares of the increment or the cross products increments and so on and you retain only the first order terms and exactly the same thing will be done for mismatch as well.

So, I suggest that you go through the whole exercise of calculating the complete expression and neglecting the higher order terms and making sure that the exactly what you will get by the simplified analysis that I am going to show. There is nothing performed in this; that is something very simple, I am going to calculate only the first order terms. Let me copy over these expressions, now because I know already that I will

get two terms one related to delta -beta and one related to delta VT and some of those two.

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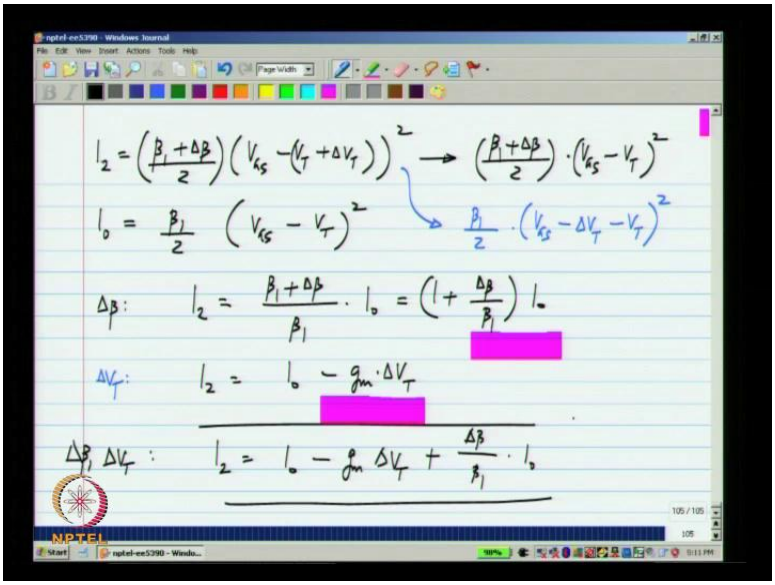

So, instead of going through the whole calculation, I will first assume that I have only delta -beta and no delta VT, In that case this expression would be beta 1 plus delta beta by 2 times VGS minus VT square, because any way to neglect the product of delta- beta and delta VT, this is a good enough approximation. So, the effect of delta- beta would be that, high to simply equal beta 1 plus delta- beta from here divided by beta 1 times I0 or 1 plus delta –beta by beta one times I 0. Now, given that beta one is the current factor, this is exactly what you expected; Right? So, if there is an error in the factor you will get one plus the error in the factor divided by nominal factor times the current.

Now, second layer I will assume that there is only delta VT, in that case this terms to beta 1by 2 VGS minus VT plus delta VT whole square. Again I can go through the exercise of expanding this and neglecting higher order terms in delta VT, what I will do is I will rewrite this as VGS minus delta VT minus VT square, this is the very common trick that is used and you can see that an increment in VT by delta VT is equal to reducing VGS by delta VT. In all the expressions of the mosfet, we only get VGS minus VT together, will never get VGS and VT separately.

It is a fundamental thing; this is because the effective voltage across the gate outside between the gate and the channel is VGS minus VT, VT is the sum of all those internal

drops between different materials and so on. So, the amount of the charge in the channel is related to VGS minus VT and everything else comes from that. So, you only get VGS minus VT together. So, in general any change in VT can be described to change in VGS without changing the result. This is an equivalent modeling trick that we can use.

Now, what this means? What I am saying is, instead of a thinking of this as a second transistor as a transistor who threshold voltages change, I will assume that there is a change in the gate source voltages of the transistor by an amount delta VT. Whatever VGS appears here is reduced by delta VT, when it comes there and delta VT is the small quantity; Right? So, the voltage here is VGS minus delta VT also you see that this increment minus delta VT over a nominal value VGS.

Now, if this was VGS and there is no beta error the transistor here would have given the same current I 0. Now, I have an increment delta VT, what is the increment in the drain current? Now, delta VT is increment VGS; Right? So, we know that the increment in drain current is nothing but dou ID by dou VGS, times increment in the gate voltage which is nothing, but GM times delta VGS and delta VGS is minus delta VT. In this particular case because equivalently model change in threshold voltage, I will change in gate source voltage.

So, what I am going to gate because of delta VT, I 2 will be I 0, the nominal value minus GM times delta VT. So, the error due to error in current factor is thus much the error due to error in threshold voltage is that much? So, the total error is when you have both delta-beta and delta- bête will be I 0 minus GM delta VT plus delta beta by beta1 times I 0. So, as I said earlier please go through the complete expression neglect the higher terms and makes sure that this is exactly what you get. It is a good exercise in analysis also, just to increase your confidence. This kind of calculation makes sense if, delta VT is positive. What does it mean? The threshold voltage is increased and the current will reduce and we have minus GM delta VT. So, that part makes sense. Similarly, if the current facts or increased delta- beta will be positive and the current will be positive. So, the sign in front of that is also positive.

So, that mention as well as usual when we are dealing with mismatch. We are not interested calculating the exact current that is not possible because each of this delta VT delta- beta are random quantities, just like delta R and delta C they have Gaussian

distribution around some nominal value and what we describe is the standard division of that distribution, because it is a Gaussian, once you specify the standard deviation, you describe the whole thing for the output current as well as for high we have to just specify a standard deviation I 2, I 0 minus GM delta VT plus delta- beta by beta 1 times I 0.

So, I 2 minus I 0 is given by M minus GM delta VT plus delta- beta by beta 1 times I 0 and normally what I am interested in finding out this is delta I, is delta I relation to the nominal value of I naught. So, I will divide the whole thing by I naught. So, delta I by I naught turns out to be minus GM by I naught delta VT plus delta- beta by beta one. Now, we know that GM can describe many expressions and one of the expressions was 2 times I 0 the drain current divided by VGS minus VT, this is the most convenient form to be used here. So, GM by I 0 simply becomes minus 2 divided by VGS minus VT.

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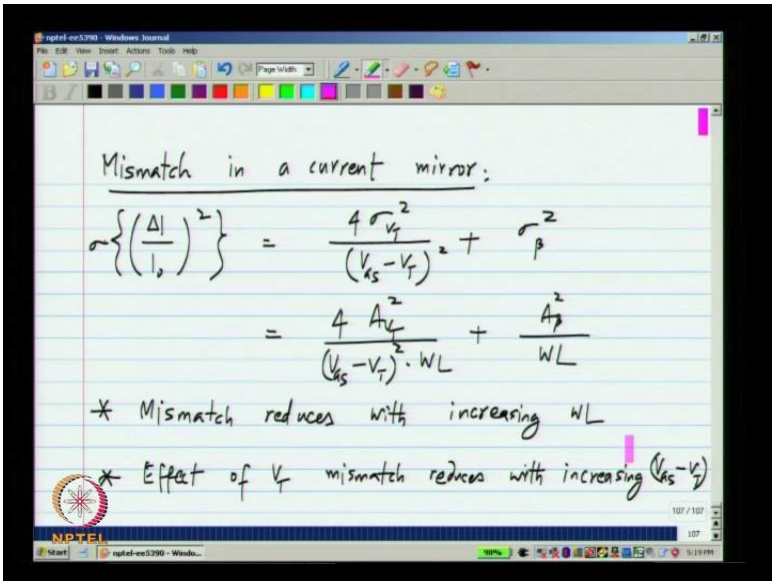

And have delta VT over there plus delta- beta by beta 1. We want to find the standard deviation or the variance of this one and we know that when we have uncorrelated random variable delta VT and delta- beta. This is very common consumption that these different things are uncorrelated, also the variation of different kinds of components unrelated form each other. We assume that variations and VT and variations beta are uncorrelated. So, the variations of this is given by four times the variance in VT divided by VGS minus VT square plus sigma beta square because sigma beta is nothing but the standard devotion of that delta- beta to the nominal value of beta.

So, finally the mismatch in a current mirror is given by this expression. The variations of mismatch is four times the variants in VT divided by VGS minus VT square plus variants of beta, which really is the variance of the difference in beta to the nominal beta and this in turn is given by 4a VT square by VGS minus VT square times WL plus a beta square by WL.

So, first of all what all the things we can conclude from this is clearly the current mismatch reduces with increasing WL. So, as you increase the size of mosfet the amount of mismatch reduces. This is exactly what we saw in resistor capacitors also. So, this is something that is consistent with what we had before. Also you see that there are two parts here, one is due to VT mismatch and one is due to the current factor mismatch. The current factor mismatch of course, depends only on a sigma beta square or a beta1 due to VT mismatch also has VGS minus VT whole square in the denominator.

So, these are interesting thing, that if you want to reduce that effect of VT mismatch, you would operate the transistor at a large VGS minus VT. Now, this second max intuitive sense because as I said the charge in the transistor and everything that follows the current are so on or a function of VGS minus VT. So, it is the change in this that we are worried about. So, you can see that what we get this something like delta VT divided by VGS minus VT the amount of fractional change in VGS minus VT. Now, just like everything else if we have a given change, but a very large nominal value, let us say you make a 1 millimeter error when you are measuring 10 centimeter. You get some fraction. You make 1 millimeter when you measure 1 kilo meter; obviously, the relative is much smaller.

So, if you have large VGS minus VT, then the same delta VT appears the small fractions of that and the effect of VT mismatch will be smaller. So, that is one thing to be kept in mind, second you see, that last time I said when you operate the transitions told reason that is when you operator transitions smaller and smaller VGS minus VT, there are some benefit like increasing the trans conductor for a given bios current, but here you see that the effect of VT is very much worse because delta VT divided by VGS minus VT will increase, if VGS minus VT becomes smaller. So, there are trade of everywhere we will try to put all of them together and usually a process of design is judicial choice of parameters. So, let no single factor will kill your circuit the effect of VT.

Mismatch reduces with increasing VGS minus VT. In fact, things are quite interesting as well. So, let us take a case where the current factor mismatch is negligible, I will say that a beta is 0 just hypothetically and you have only a VT in a given process, now I want to make a current with the given value of current, let say 200 micro amphioxus. What I should do to reduce the amount of mismatch? If you just blindly use, look at this expression you could say that I would use a larger transistor and it could be larger in W or L, because if you look at this expression both W and L appears in the denominator, but we are little more care full then that. The conditions I impose was that the current was given

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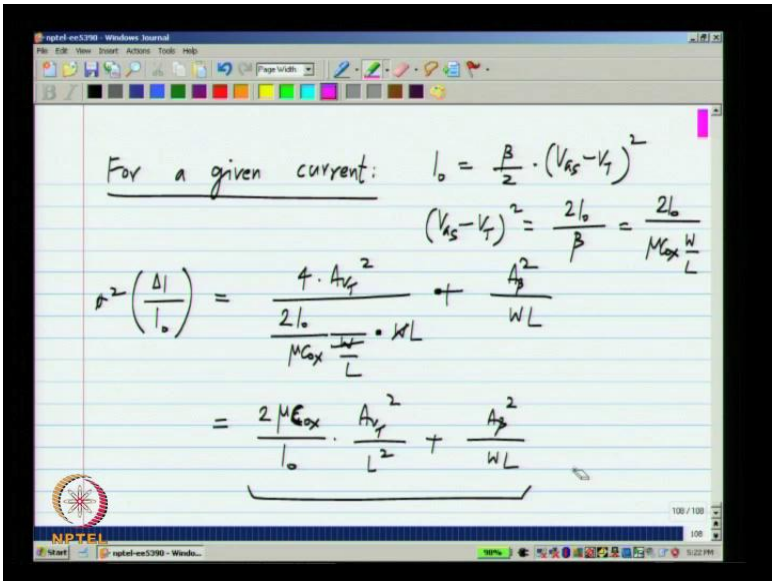

We're as the expression that we have assumed a given VGS minus VT for a given current. What we have I 0 is beta by 2 VGS minus VT square in other words VGS minus VT square is 2 I 0 by beta. Now, substituting that we will have standard deviation of delta I by I 0 to be 4 a VT square divided by this term and what is beta after all 2 I 0 by m Cox W by L that is what we have times WL that comes from a VT square by WL plus a VT square .

We can see that, W simply cancel all, so will have some constant two mu Cox by I 0 a VT square by l square plus a beta square by WL. So, this thing tells you that for a given current, if you want to reduce the effect of VT, this much you have to increase the length of the transistor. There is no other way now, this make sense again because for a given

current if you want to increase the value of VGS minus VT, you have to increase the length.

You may also have increase the W, but that is not relevant. What is relevant for the mismatch calculation is the increasing length, so again we will see effect of the length on the performance of the mos transistor and see that all of these things will give you some trade, if you make something better, something else will get worse. So, this is about the mismatch in a current mirror and it gives you a good idea of what happens with regards to mismatch in a MOS transistor circuit. There are two sources of mismatch VT mismatch and current factor mismatch and then lot of them circuits VT mismatch usually models dominion, but not universally.

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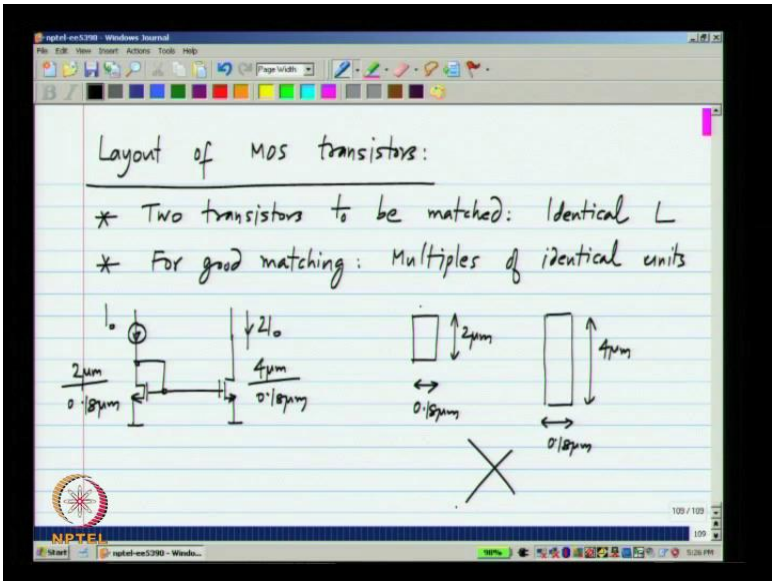

So, of course you can have the current factor also to be a quite dominant, but in any circuits VT mismatch also to be more dominant now as with resistors and capacitors two identical mosfet, two mosfets with same W and same L will match to each other, but the physical lay of those things cannot be arbitrary, you have to lay them out in a careful way, so that the parameter are identical to each other because always some symmetry in the directions and so on. They have to be oriented in the same way etc.

We will now briefly discuss the layout of mos transistors. First of all I have mentioned earlier the proportionality to W is more or less exact, but the initial proportion is L is each 0. So, whenever you have one term. Two transistors to be match your design with

identical values of L. This is sort of negotiable and unless there case, some cases where you cannot do this at all. You always do with identical L, you will never make a current mirror with the two transistors having different length as with any other component for good matching. You should use multiples of identical units.

So, for instant let us say I want a current mirror and let us say this is 2 microns by 0.18 microns and this is 4 microns by 0.18 microns. The idea here is that if I push I 0 here, I get a current 2 times I 0. Now, one possible lay out of this, I will show as usual this is 2 micron and this is the same L point at micron and the other one is like that 4 micron by 0.18 microns, but if you do this the current and in this transistor will not be twice the current in the transistor small error because this is wider transistor that add effects and so on will be somewhat different then that one.

So, this is not the way to lay out two transistors, where one of them has four microns and other one has the weight of 2 microns, the correct thing to do is take three transistors of width 2 microns and length 0.18 micron, the same everywhere and let me call this drain of transistor and that is the drain and the source and you connect this two transistor in parallel.

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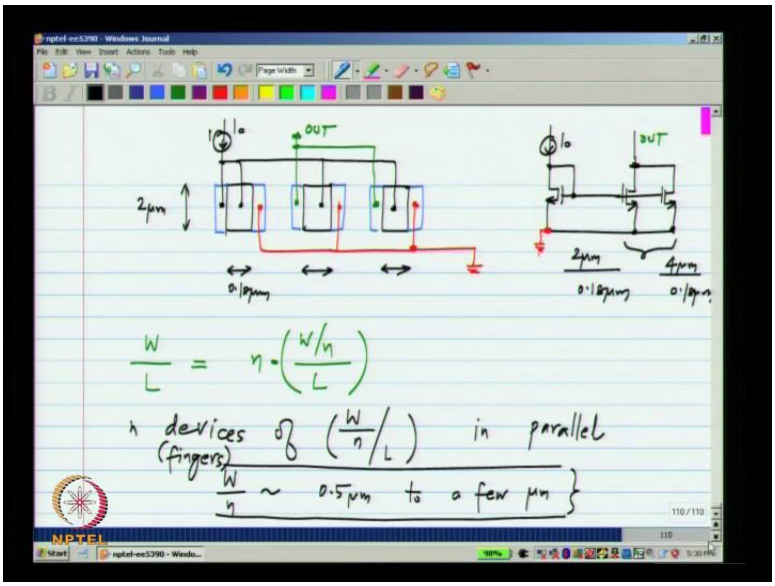

So, effectively the schematic might be represented like that now all three transistors are a 2 micron by 0.18 micron, but these two are type together. So, you can effectively thing as a single transistor of 4 micron 0.18 micron, but the physical layout has to be

something like that. So, perhaps this is the drain, this is where you connect I 0, this is where I have I 0 and that also connected to the gate and its connected to all of the gates.

Source of all are then connected together to ground if this is ground and the drains are connected together. So, this is the point which you get the output current. So, you have to lay out identical units and connect some of them in parallel. Now, this is done very frequently MOS transistors. Let us say you have a width of 100 microns and a length of 0.18 microns and this is you could have millimeter and the length of 0.18 micron, you never ever layout something.

So, eccentric that is you make it to 1 millimeter long like this only, 0.18micron long, if you make it 1 millimeter wide micron long it will be. So, less full of area that you will never ever do something like that. What you do is in general when you have WL, W has some dimension and L has another dimension and have already explain that it is not the ratio, but the dimension of each one that matters it is cutup into ten pieces W by n divided by L in parallel and devices of W by n divided by L in parallel.

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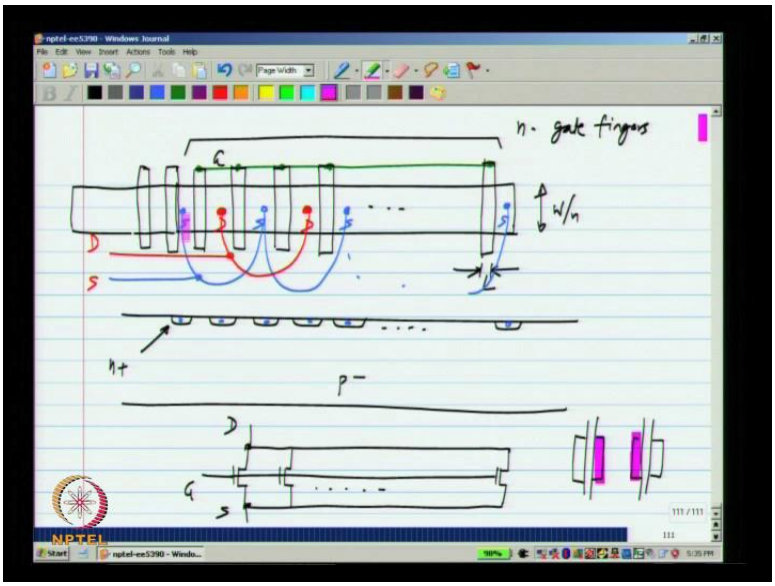

This can give you reasonable ratio and usually this W by n can be of course, any value, but typically let us say 0.5microns to few microns, these are not secret numbers these are all usual guidelines, but sometimes this could be while related as well, but this will unsure that you do not have eccentric expect ratio and this different devices are usually

called fingers because essentially when you have n devices it means that you have n gates of W by n width.

What I mean is the following top of such a layout. You look like that the gate fingers are all layout next to each other and the cross sectional view of a corresponding n mos might look like that and these are all the n plus reason. I will mark them like that they correspond to this things. So, you will have n gate fingers, all of them has the same length L and a width equal to W by n right and all these gates are connected in parallel by somewhere outside. They also have drains and sources in parallel and you can do that by making alternate once source and the other alternate once drain. So, perhaps this is the source and this is the drain and so on and if you connect like that right this is also source let us say and then you connect the drain also correspondingly.

You will see that this is the same as having all the gates of n fingers connected together and n drains connected together and n sources are connected together, this is the gate. So, the way it has been laid out that between two gates there is the diffusion reason and that serves to the drain of this transistor as well as that transistor, now sharing this refusing region is very advantages because of an alternate way of doing this could be that you have a transistor like this and for each of this fingers you make a separate drain and source region let me draw elsewhere. So, let us say this is one transistor and this is another transistor which is drawn separately now the problem with something like this is that you have drain diffusion here and drain diffusion there.

And it recall the small signal module of the mosfet, each if diffusion junction contributes to capacitance, now by sharing the diffusion between adjust and gates. What you have done is effectively reduced the amount of this parasitic capacitance by half. In fact, you can go and calculate this calculated area of this drain diffusion and the source diffusion. When the number of finger diffusion is very large for this kind of lay out verses each of transistor is separately lay out and things are connected in parallel you will find that the patristic capacitance is reduce approximately by the factor of two.

So, this is now mos transistor of layout if you cut off the mos transistor into a I units of some reasonable small rate usually amount of micron and then you connect in parallel. If you want the current mirror, what you do is you just expand this array as you have as they want and connect drains and sources appropriately this kind of lay out is use very

often and the moment you start using the lay out tool you do lay out to the mos transistor. Please start using this method. Please do not use separate layout of mosfets or settling none different lengths for devices that are supposed to be match are devices that are lay out in difference of the orientation and so on.

They should all be lay out in array of fingers like this if you want a current mirror let say I will just continue this array with more fingers and remember the terminal of the two transistors in a current mirror. There is some terminal right loads of two transistors are common, so this terminal between the transistor corresponding to M1 and transistor M2 corresponding to can be the terminal and then you connect the rest and also well laying out the resistor and capacitor and mention that for good matching you put dummy devices either in this case. You put dummy fingers again I will slow you quickly with an example of a current mirror.

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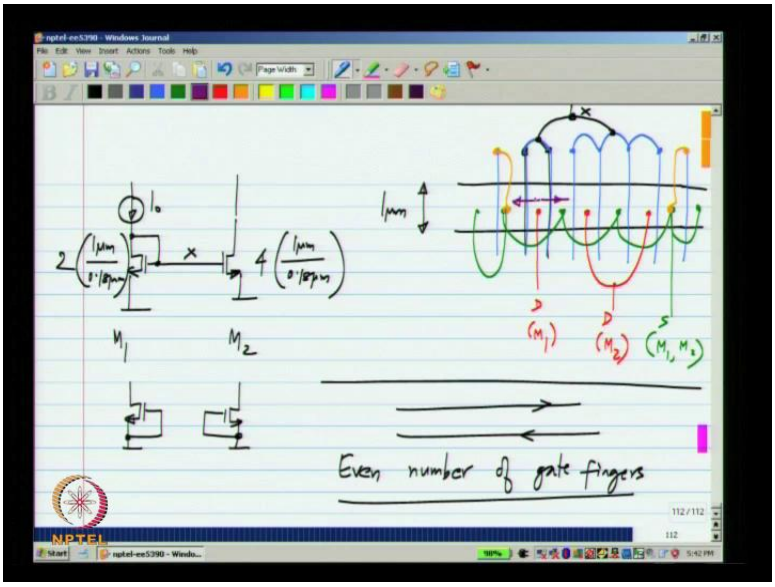

Let me assume that, I have a current mirror and this consist of 2 fingers of 1 micron by 0.8 micron and this consist of 4 finger of 1 micron by 0.18 micron an order to draw quickly I will show autistics. This is the 1 micron with and I have diffusion all over. If you study some lay out you will see that a gate policy relevant draw over the diffusion forms a mosfet. So, first of all for M1 I need two fingers, let us say, this two forms M1, this vertical lines denote the gates perhaps you got a different color.

So, these are gates and for the right side transistor M2, I need a four fingers and I will connect all of those gates together and because the current mirror is also connected to that, one that form this terminal. Now, for the drain of M1, this is what I have is the drain of M1 and the source of M1 and M2 which are common. I will be connected like that, this is the source of M1 and M2 and the drain of M2 will be connected in parallel. These two reasons connected in parallel will be the drain of M2 and finally, you see that there are totally 6 gate fingers, the one on the outside have only one neighbor, where as the other instead have two neighbors, so we also include dummy fingers on either side. I will show one dummy finger, but in some cases you may have to use more than one two or three.

So, those are like having two more transistors in the circuit and remember the source of terminals is common to these transitions that as well. So, the source of this happens to be grounded in these circuits and source of that is also grounded, but these transistors are not useful transistor. I have no role for them in my circuit. So, they should really carry zero current, so it means that, what I can do is to connect to the gate to the source. If I do this VGS will be zero and current will be zero. So, for these dummy transistors I will connect the gate to the source and real integrated circuit you have many layers of metal and you have to arrange the metal. So, that you come with this particular layout.

So, this for instance is an example of reasonable layout for a current mirror, where you take care of matching very well that is you have each transistor lay out as multiple provided units. One of them has 2 units, the other one has 4 units and you also take care out dummy transfer at both ends, so that all of the gate fingers that form the current mirror CN identical and there is one more thing that you can do, you can see that M2 the right of FM1 in this case. We have M2 here, M1 there, but they may or may not be the base layer. Sometimes, you may have the common centre for M2 and M1, so what you do is make the middle 2 fingers M1 and this one and those two combine will be M2.

So, M1 and M2 have the same geometrical center that the matching between them will be best even there are some linear variants in the parameters of the transistor and across the chip you will get cancel out and your identical line behavior. Now this is the lot of detail, but to get a IC2 works, which I you have to mind all this details because one of the difference between designing descript component circuit and integrated circuit is that you do not have freedom to play around the into the device. You are given the package

device, you sell as careful as possible and then your job is done, where as an integrated circuit there is freedom to even a modify the geometry of individual devices and it has to be done very carefully, so that you get the best result that is possible.

Now, one last point lay out it turns out that while these transistors are being made you have open from diffuse form the top and there is T some a symmetry, there is MS symmetry to this, which current in the that directions and transistor which carry in that directions to avoid this a simple technique is to always use and even number of gate fingers, what I mean is for instance and this particular current mirror that I took. Example of earlier, the current goes from drain to source right, so in this transistor the current goes that way and in other transistor that goes that way and we have no idea what is the symmetry and so on. What do I have even number of fingers always get, what plus even together. So, whatever a symmetry there is one, two add up the two that will go away and the unit becomes odd plus even.

So, which always recommends that, use even numbers of fingers, again sometimes you may have to violate this because this is not really possible, but as far as possible always use even number of fingers. So, we have delta with MOS small signal model and also calculated affect of mismatch in the mos transistor found out and discuss lay out techniques to minimize mismatch in a mos transistor circuit.

We took current mirror is example, but later we will come across many circuits where we need mos transistor to be identical and exactly the same principle supply. So, far we have looked at characteristics of MOS transistor, like a mismatch and other small signal characteristics. Now, what I will do is to discuss speed of mos transistor in a very general way. The actual speed of operation the unity frequency and so on depending on the specific for the circuit, but this is way to characterize the technology. Now, you hear in particularly in connection with the digital circuits that is becoming faster and faster with more and more advance technologies. Let us see, if there is the measure of speed for analog circuits? Now, this is the very generic measure based on the performance of the s single transistor.

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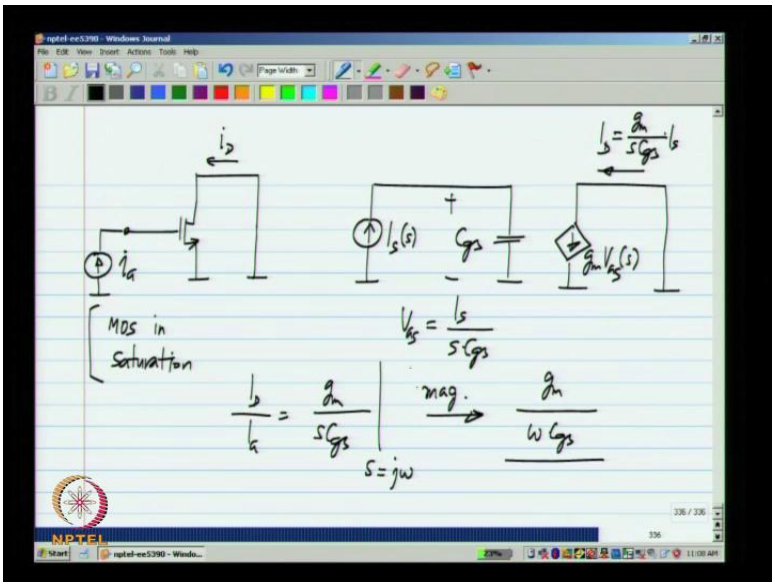

What we do is, this is a MOS transistor and this is equivalent circuit. I will ignore the body effect and other things, I will also ignore CGD, I will assume that MOS transistor operating in a saturation region, where we normally have MOS transistor. So, it has a CGS and assumes CG to be zero and it may also have some CDB. Now, what is done normally is to evaluate the short circuit current gain of such a device that is in the small signal picture, you apply a IG, that is the gate current and measure the value of ID, that is you apply small signal short circuit and measure and ID. Now, these strains like to apply current to the gate.

Here we are talking about high frequency currents and that can flow into the gate and also this kind of test was previously use for high bicolor transistors, which are very popular. There it was very common to characterize the bicolor transistor, the current gain and now the same thing is borrowed to characterize the speed of MOS transistor as well. Now, this is the incremental picture in reality, it is biased and the short circuit and this current sources are small signal incremental sources. If I write small source equal of this, the circuit is really simple. I have ISI which shows as a function of frequency and I have a CGS CM. I could have some parasitic capacitors from drain to the source subscribed, but because it is terminated by sort circuit, it is ignored.

So, I will have gm times VGS as the current, where VGS is this voltage as very obvious that VGS equals by SCGS. So, the drain current will be simply gm by SCGS times IS.

So, the current gain Id by Ig will be gm by sCgs of the mos transistor and at a frequency is equals gm omega. If we evaluate the magnitude, we get gm by omega Cgs. Now, you see that this mos transistor also behaves like an integrator, if you consider the input to be your current and the output to be a current.

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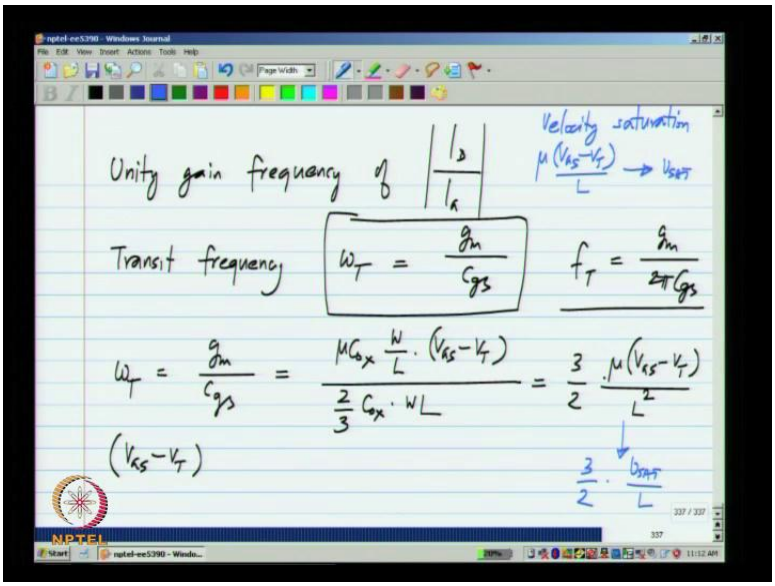

Now, the unity gain frequency of this integration mode Id by Ig is defined to be the transit frequency f T and that is of course, the omega T, this is the transit frequency and variance per second omega T, if you want Ft, you simply divide the result by two pi as I said earlier, this terms and the definition borrowed bicolor transistors now omega T by gm by Cgs. You can calculate for some transistor by a start as given VGS minus VT. So, if you have a transistor some VGS minus VT the value of gm is given by mu Cox W by L, VGS minus VT and Cgs itself is given by Cox WL. So, what we have here is two-third Cox WL in saturation region. What we have here is 3 by 2 mu VGS minus VT divided by one square.

So, both Cox and W cancel out. So, you see that the transit frequency depend only upon the mobility the operating point VGS minus VT and the length of the transistor now you also hear that as go to more advance technology minimum lengths goes on reducing. So, this transits frequency goes on increasing for a given bias voltage. Now, if you take a process technology the transit frequency will be specified for some value of VGS minus VT, which is typically equal to the supply or a large fraction of the power supply.

Now, what is the frequency mean? It does not by itself means much because this transit frequency for a modern technology could have been the many 10's or 100's of giga hertz because it is bias and very high VGS minus VT and in reality the bias transistor with a small VGS minus VT, such as100 and 200 mille volts which means too much, but it is a measure of the speed capability of transistor that is for the some VGS minus VT. If you go for short and channel technology the maximum possible speed will be increased, so do not pay too much attention to the absolute value of the frequency it is only improving with different process node that is what matters now.

What can we say from this now, first of all before I go further, let me say that, this is assuming square law and if you assume velocities saturation, the speed of the carriers in the device is mu times VGS minus VT by L, that is the mobility times the electric field in the device and this will be replaced by V SAT. So, in case of velocity saturation device, this will change to 3 by 2 V SAT by L. So, the one over L square dependence go away and you will have more dependence, but in another case, if you go to the shorter and shorter channel MOS transistors, the speed will increase, the reason I discussed to all. This is to give you favor of read between speed and accuracy and the power consumption in a very general way.

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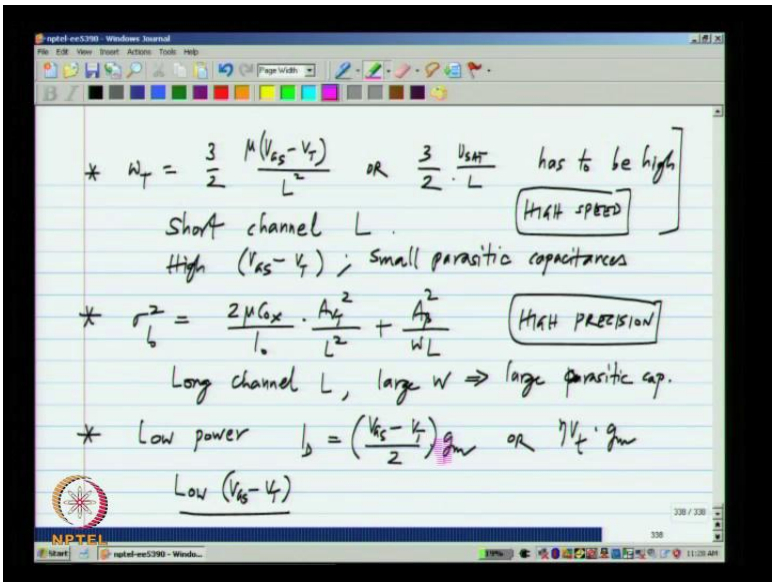

Now, all the three are important. You would like a circuit to consume the little power, you like them to be very accurate that is very mismatching, little error and you would

also like them to work at very high speed. What does that mean for a circuit by very high speed is that we have a measure of speeds. This has to be high, which means you use as short channel transistor as possible, this is for high speed and you would also like to operate the transistors with a high VGS minus VT.

Now, for high accuracy we have earlier derived the expression for mismatch, for instant on a current mirror. I will use that as a representative expression, so the error in a current mirror is given by something like this. So, you have high procession you would like to have variance error high precision or accuracy. We would like to use long channel like L channel it must be long and also a larger transistor large W as well.

Now, in general for high speed we need to have small parasitic capacitances and finally, for a low power we need to have small bios current. We know that the drain current is related to the gm that you want to realize and you can use the expression VGS minus VT by 2 times gm. I will assume that gm is something that fixes you to realize a certain value of gm or in weak version region; it could be eta BT time's gm. So, for lower power operation you would like to minimize Id and that means you operate with the low value of VGS minus VT. So, clearly you see a conflict between these three requirements for high speed. You need high VGS minus VT for low power you need the opposite. In fact, is the way to get high speed? These two pumps current into the small capacitor, similarly for high speed device you need a short channel length and general minimize patristic capacitance, but here or high accuracy you need to a long channel L.

And in general last device which also implies large patristic capacitances, have generally low value of mismatch. You operate with the high value of VGS minus VT and that is the in a conflict with this power requirement, which says that for a given gn you need to operate with the low VGS minus VT. So, this should give you flavor of trade between precision speed and low power. As an analog designer your job will be to manage these trades as well as possible.

Thank you. See you in the next lecture.