Analog Integrated Circuits Design
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Lecture No - 15
Two and Three Stage Miller Compensated Op amps;
Feed forward Compensated Op amp

Hello and welcome to the 15'th lecture of analog integration circuit design, in the previous lecture we discussed the two stage op amp in great detail. So, where the poles and 0's were and right to adjust the components, so that we get sufficient phase margin when the op amp is placed in feedback. Now, do not worry about, exactly what feedback loop the op amp is placed in we assume that, it is placed in a unity feedback configuration and then go with the calculations. And reality what you have to do is to find the value of k that is the feedback factor that you are trying to use in the actual circuit, and then do your loop gain calculations placed on that place.

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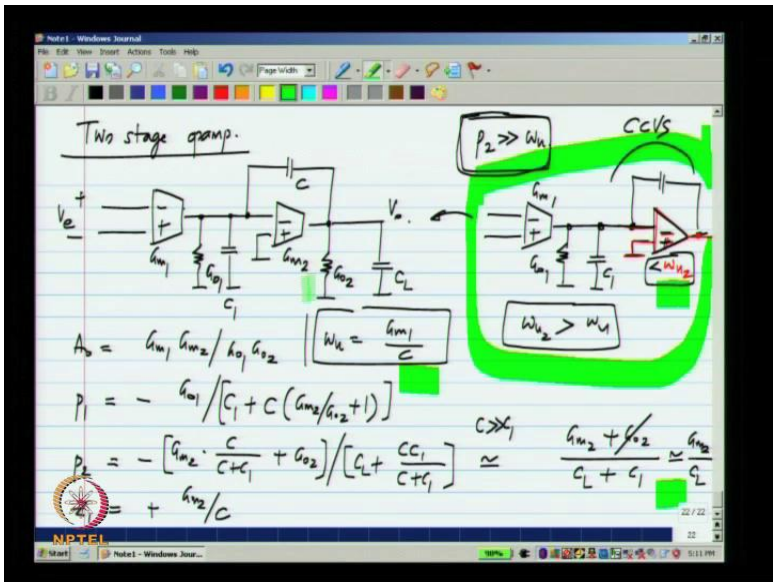

We just the quick recap this is a two stage op amp, the first stage G m 1 as an output resistance arrow 1 are an output conductance G o 1. And there is a capacitance C 1 here which can be due to various sources, and the second stage as a trans conductance G m 2 an output conductance G o 2 and a total capacitance of C L, which can be due to trans conductance itself.

And any load that is applied to the op amp and there is a capacitance C which is around the second stage, and this is the integrating capacitor that is the current from G m 1 is supposed to pass there is and give the integrating function with a unity gain frequency of G m 1 divided by C. And we also evaluated the expression for poles and 0's and all that stuff of this one, the DC gain is the product of the 2 DC gains the low frequency pole is at minus G o 1 that is this conductance divided by total capacitance, which is C 1 and miller multiplied C.

And the second pole P 2 is at total conductance is G o 2, but more predominately the effect of G m 2 in feedback. And here we have total capacitance which is C L plus C and C 1 in series, and the 0 is in the right half plane at G m 2 divided by C we also saw that the second pole can be further approximated by this is one C is much more than C 1, G m 2 plus G o 2 divided by C L plus C 1. Now, G m 2 is expected to be much more than G o 2, so we can neglect this as well.

And usually C will also many times happens to be much more than G o 1, so this can even be further many times approximated by G m 2 by C L. Now, what is a stability criterion of role, the unity gain frequency of this is of course, G m 1 divided by C a stability criterion says that the 0 and the pole has to be sufficiently beyond the unity loop gain frequency, which is the same as the unity gain frequency of the op amp for a unity gain amplifier.

Now, the phase lag contributed by the 0 is simply a function of the ratio of G m 2 by G m 1, and that has to be maintain sufficiently high. So, that the phase lag is small, the phase lag due to the pole will be something and we would like P 2 to be much more than omega u. Now, what is this mean remember this op amp was derived from a structure like this, we wanted the output current of G m 1 to go through a capacitance C, and we found that the best way was to implement a current control voltage source.

And this current control voltage sources is implemented using a some op amp show near in red, and let us say it has a certain frequency omega u 2. We also know that, if you taken op amp with a unity gain frequency omega u and you make a feedback circuit with it, then the feedback functionality will be until a frequency of the unity loop gain frequency. Below the unity loop gain frequency, the feedback loop function as a suppose

to above the unity loop gain frequency, the loop gain becomes very small and clearly the feedback loop does not function as desired.

Now, what is it mean the unity loop gain frequency of the second feedback loop, turns out to be omega u 2 itself. So, omega u 2 has to be sufficiently larger than the frequencies of interest, now what is a frequency of interest we can consider omega u itself to be the frequency of interest by this what I mean is, we are trying to make an op amp with a frequency with a unity gain frequency of omega u that is this entire circuit should behave like an integrator, up to a frequency of omega u.

Now, the integrator itself is made by placing a capacitor around the second op amp, so that we format current controlled voltage source. Now, this will behave like a current control voltage source only below a certain frequency omega u 2, which is the unity gain frequency of the second op amp. Now, clearly the unity gain frequency of the second op amp has to be more than, the unity gain frequency that we want to realize, this is not the case then clearly the entire circuit does not behave like an integrator at all.

So, to the integrator as to behave like an integrator that is have a 20 d B per decade role of at least up to the unity gain frequency of the integrator. So, this is what we would guess just by looking at this shot of system block diagram, now what is omega u 2 it is the unity gain frequency of the second op amp, and it is G m 2 by C L. Clearly then G m 2 by C L has to be much more than, the unity gain frequency we are trying to realize which is G m 1 by C.

So, that is this frequency here must be much more than G m 1 by C and that is exactly what this condition is saying also this P 2 has to be much more than omega u. The second pole P 2 appears because, the op amp with which we made the current control voltage source, itself has a finite unity gain frequency. If the unity gain frequency of this the second op amp was in finite, then we would not have this second pole and we would just have a single pole op amp is this clear. So, this gives you another intuitive way of figuring out why this conditions come about, it is extremely important when you get algebraic results to attach some intuitions to it.

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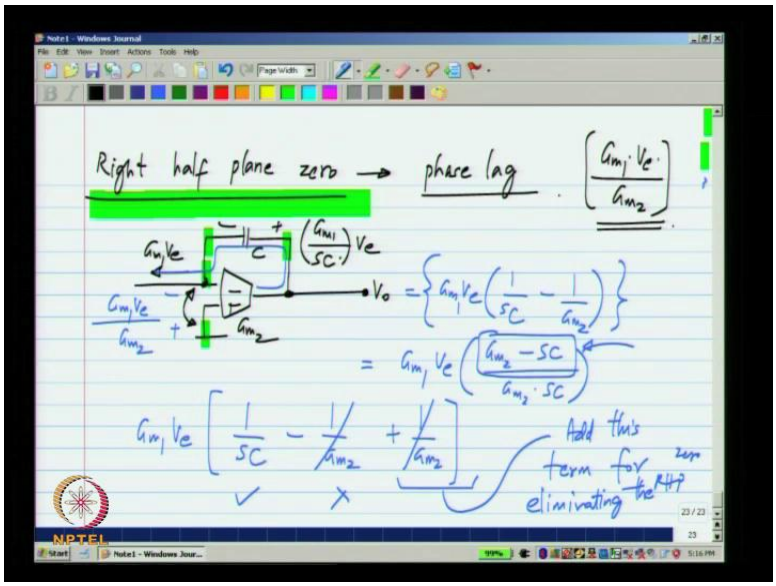

Now, the right half plane 0 this causes phase lag, now this is on annoying problem as well because, of this the phase margin is triturated. Now, we did not have the right half plane 0, we would have the phase lag only due to the poles and could have in a better situation that is you have less phase lag. Because, you do not have the right half plane 0. So, what we would like also is to investigate if there is a way of getting write of the right half plane 0 or may be eliminating the effect or reducing the effect of the right half plane 0.

In order to do this let us fast figure out why the right half plane 0 comes ago, for this I will focused only on the second stage of our op amp. We have a current G m 1 V e it is supplied by the first trans conductor, and that is pass through this current control voltage source, which behaves as an integrator. Now, what I will do is I will neglect all the other components because, I want to focus only on the right half plane 0, and not worry about other details.

Now, what happens if we do this, this G m 1 V e will pass through the capacitor, and it causes a voltage drop G m 1 by S C times V e. And this is the exactly the voltage that we want, but this is not the voltage that appears as V o because, that is equal to the voltage across the capacitor plus the voltage between this point and ground. And this will have a voltage I have assumed that there is no load or anything like that, so this G m 1 V e this current passes through the capacitor, and has to come out of the trans conductor.

If it has to come out of the trans conductor, across this there must be a voltage which is equal to the current through the trans conductor divided by the trans conductance value which is G m 2. So, the total voltage v naught equals G m 1 V e 1 over S C minus G m 2 sorry minus 1 over G m 2, now this is what results in the right half plane 0, this is exactly the term we saw in the numerator earlier also, and that is what gives you the right half plane 0 and we want to get read of this one.

Now, by looking at the expression for V o we can guess what we must do to get read of this the expression for V o is the input current to the second stage, which G m 1 v e times 1 over S C which is the desired term minus 1 over G m 2 which is the undesired term. If we add only the first term here, we would have integrator of unity gain frequency G m 1 by S C right. So, what can we do to get read of this we have to add plus 1 over G m 2 in somewhere the other. So, we have to add this term for eliminating the right half plane 0 if we do that then this simply cancel with that and we will be left with only the integrator. Now, how do we add that, so; that means, that is to the output voltage that we originally have we need to had a voltage equal to G m 1 V e divided by G m 2 that is the input current divided by G m 2.

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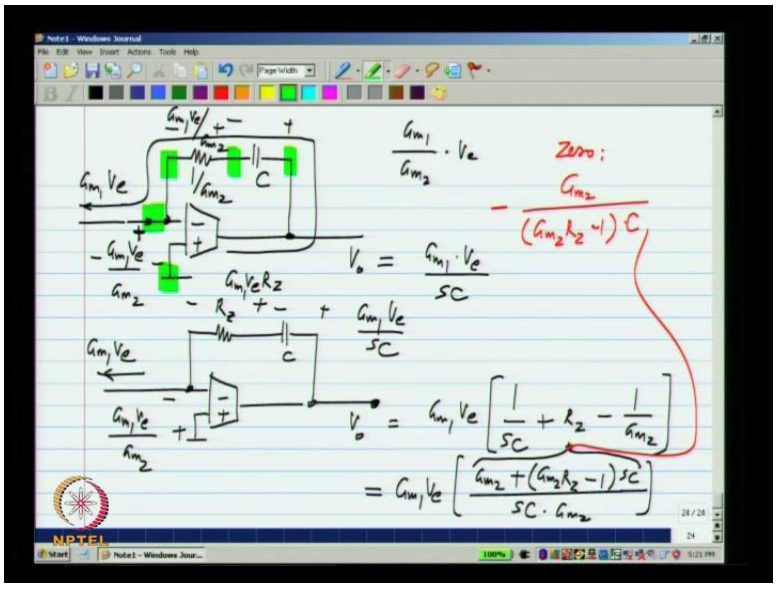

As a very simple way of doing this that the voltage that develops their this is G m 1 V e, and this branch the capacitor also carries a current G m 1 V e. So, I want the voltage to be the voltage across the capacitor plus this plus an extra term which is G m 1 by G m 2

times V e, it is very easy to see that if I insert a resistor here which is equal to 1 over G m 2 what will happen across this resistor I will have G m 1 V e by G m 2.

So, now, if I sum these three voltages the voltage across here plus the voltage between these 2 plus the voltage there I will get V naught, and V naught happens to be just equal to G m 1 times V e by S C this is fine. So, by placing a resistance in series with the capacitor, we can eliminate the right half plane 0 and the value of the resistance has to be 1 over G m 2. Now, if their value of the resistance changes from 1 over G m 2 what will happen is, you will get the some not an exact cancellation of the 0, but something else that we can also see.

So, let us assume that again the same circuit and I will call this R z voltage at the input of the trans conductor is G m 1 V e by G m 2, the voltage across this is G m 1 V e R z and the voltage across that is G m 1 V e by S C. So, the total output voltage is G m 1 V e times 1 over S C plus R z minus 1 over G m 2, so we will get G m 1 V e that and, so I will write this as G m 2 R z minus 1 times S C.

So, the numerator there is a 0, and the 0 is that G m 2 divided by G m 2 R z minus 1 times C in the negative of that one. So, this expression makes an because, first of all in R z is 0 that is the old case, we have a right half plane 0 it is G m 2 by C when R z is exactly equal to 1 over G m 2 the 0 moves to infinity, and when R z is more than 1 over G m 2 will have a left half plane 0. So. in fact, you can move the 0 to the left half plane 0, and the advantage of a left half plane 0 is that it offers a phase lead instead of a phase lag which enhances stability.

But, we cannot play this game very much we will see soon why, but at least we see that we can move the 0 to infinity or otherwise manipulate the position of the 0. Now, this particular structure is very simple I will eliminated C 1 C C L on the other side etcetera, etcetera. But, the principle works in exactly the same way, we will see that soon the principle of 0 cancellation what is in exactly the same way and is also widely used.

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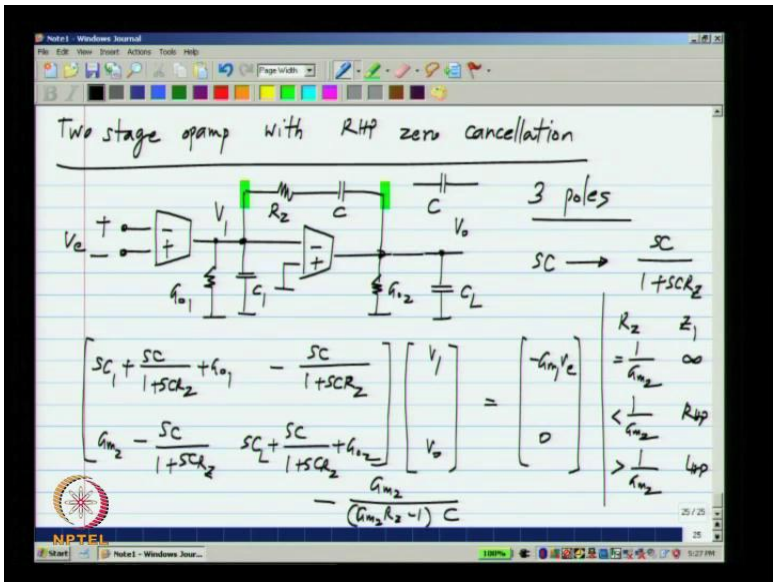

So, here then is the topology of the two stage op amp with right half plane 0 cancellation, now the transfer function of this can be evaluated in exactly the same way as before, while writing the node equations. And before we do that, we should again see what is the number of poles and 0's we have, what you think is it exactly the same as before. One difference from earlier case is that earlier also we have three capacitors, but the three capacitors were in a loop.

So, the sum of voltages of two capacitor was equal to the voltage on the other capacitor, so we could only said two of them independently and the third one was automatically fixed. Now, because, we have this R z in series with C, we can said all three of them independently, so this really has 3 poles, this again as something that keeps happening in design that, you should be aware of whenever you try to fix some problem, some other problem may come up it may or may not be severe, but it is something to be investigated.

Here what we did try to do, we try to eliminate the right half plane 0 because, it was causing phase lag we got some technique. And then when we finally, put it in the op amp we see that, we may not have a right half plane 0, but we will have an extra pole which also causes phase lag. So, you have to evaluated more thoroughly to see that the phase lag caused by the extra pole is not the ruining the advantage you got by eliminating the 0.

Now, I will not solve this completely, but I will outline the method, so again we can write the node equations and I will write it in terms to the same two node voltages as

earlier V 1 and V o equals the source current vector. Now, all we have to do is earlier between these two terminals we add just C, which gives you an admittance S C, so in the admittance matrix, now wherever we have S C we have to replace it by the admittance of this whole thing, which is what which is 1 over the series combination of R z and the capacitor.

Other words they says S C 1 plus S C R z this is an easy way to do it, we could define this two way node and right node equations, but that unnecessarily makes things complicated. So, the equations turn out to be that is the total admittance loading the first node, total admittance loading the second node like that, then here we will have and finally, there will have the source vector remains the same, here we have the minus G m 1 V e and 0.

And by taking the determinants we can find the solution, you will find that the 0 will be at what we determined earlier that is minus G m 2 by G m 2 as e minus 1 times C. So, if R z equals 1 over G m 2, the 0 is at infinity if it is less than 1 over G m 2 it is in the right half plane and if it is more than 1 over G m 2 it will be in the left half plane. Now, we will also have third pole, and again by using a similar approximation has before that is earlier we have to solve the quadratic equations we took two terms at a time, and turn it into two linear equations.

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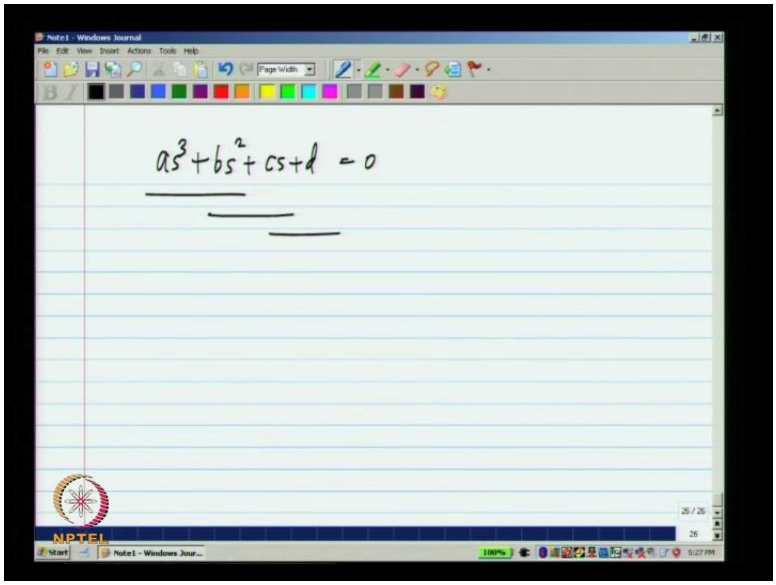

Exactly the same thing can be done for the third ordered equation that we have, if you have a s cube plus b s square plus c s plus d equal 0, we can take these two at a time equate that to 0 these two at a time equate that to 0 and these two at a time equate that to 0. We will get three linear equations, and solution to this will be valid approximation to the actual solution, only the if the 3 poles are very far from each other, the magnitude of the 3 poles have to be very different from each other.

And if you do that, you will find that the value of the first two poles are almost the same as before and you will also get a third pole. Now, I will not do the algebra here you can take it as an exercise and do it, please make sure that you will you solve this completely by using the kramers ruler, whatever your favorites method of solving the matrix equation is, and then do the approximate solution of the third order equation, and find out the poles. I will just tell you on intuitive way of finding out the poles, let me copy over this diagram.

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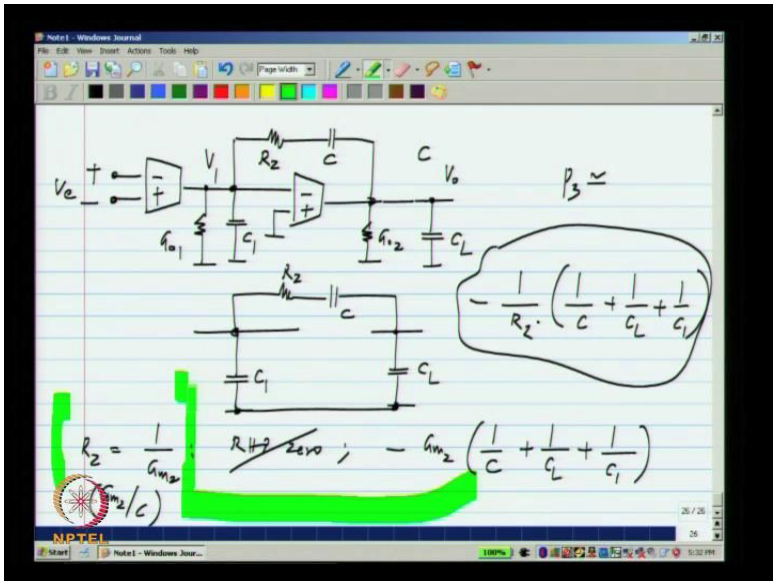

Now, the first pole will be associated with G o 1 and the total capacitance that we see, it will be almost the same as before that maybe some term is due to R z, but there will not be dominant. So, again one will again be due to G o 2 and the capacitance associated with that, and the third one will be due to R z and the capacitance is associated with that one. So, what we have there will just a turns out R z C C L and C 1, in a way you have an R z circuit involving this R z and this three capacitance of series.

Because, after all this is just ground and this two are together, so the pole associated with this turns out to be minus 1 by R z, and the series combination of the three capacitors which is just 1 over C plus 1 over C L plus 1 over C 1 that is approximate value of P 3. Now, if you do the third order equation and the approximations that I mentioned you will get exactly this solution, please verify that please those do not take this for granted. And also try to understand how I got this value here.

Now, what did we have what is the effect of putting R z there, we can eliminate the right half plane 0 and, but we will end up with a pole. The right half plane that we let say we choose R z to be exactly 1 over G m 2, then the right half plane 0 it goes away what will have a new pole what is that, it is given by that one the pole is at minus G m 2. Because, we choose R z to be 1 over G m 2, 1 over C plus 1 over C L plus 1 over C 1, and where was the right half plane 0 that we eliminated it was a G m 2 by C.

Now, comparing these two you see that the pole that you introduced is at higher frequency compared to the 0 that you eliminated. So, we are still safe the 0 that you eliminated removed some phase lag, the pole that we introduced introduce a some phase lag. But, because, the pole you introduced as a higher frequency it introduce us less phase lag, now that is why it is not a very wise thing to make a R z very large because, you may think that oh by making R z very large, I can move the pole into the left half plane.

And then even produce phase lead, but what happens is you will also have this additional pole, which will cause extra phase lag. And you will have a complete washout, and the extreme case is when let us say R z is infinity, then you will not have this capacitor here at all you will have these poles very close to each other. Earlier we saw that when this branch was not there, when C was not there, there was some pole frequency here and something else there. And when you introduce C they moved further apart, which is good for stability.

And if you make R z equal to infinity that is very large, then you will go to the original case where the poles are relatively close to each other, which is very bad for stability. So, it is not a wise thing to make R z very large, it is to make it try and cancel the R H P 0, now later you will also see that you cannot make component values exactly, you will not be able to make two unlike components have a relationship like this R z equal to 1 over

G m 2. So, even if you nominally make it like this it will vary in one or the other direction.

But, it is still a good thing because, it reduces the total phase lag that you would have got. So, it is a good technique, but do not try to overdo it that the message, so that summarizes the two stage op amp, it as a DC gain equal to the DC gain of the two stages, and when you have resistive loads you can optimize the DC gain of the first stage. And let the second stage have a modest gain, this you could not with a single stage op amp, the single stage as to provide all the gain with the two stages you also get this additional complication of extra poles and 0's. But, it is possible to design the values, so that you have a stable op amp.

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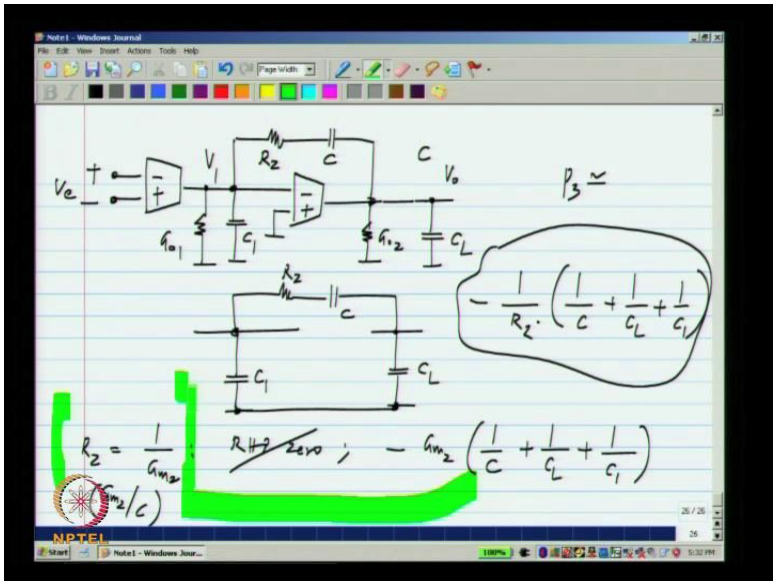

Now, let us revisit how we got the two stage op amp, first of all let me start with the simplest op amp that I had, which is thus that one. Let me just name them were let it be like this, now the two stage op amp what did I do, I try to make it better by using a current control voltage source instant. I wanted this to be an ideal op amp, but clearly that is not possible, this is the current control voltage source.

And I used by single stage op amp in place of that op amp, and I ended up with a topology which was the two stage op amp. Which of course, is that by substituting the single stage of op amp in place of this is one, which realize the current controlled voltage source I got the two stage op amp. And I also showed that the two stage op amp is better

than the single stage op amp because, it offers higher DC gain and, so on. I can play this game further right I know that, if this were an ideal op amp I would get ideal integration from there to there.

But, of course, I do not have an ideal op amp, but instead of using a single stage op amp which is inferior I could try and use, the two stage op amp over there. So, that may give me better results right, because after all two stage op amp is better than the single stage op amp, using a two stage op amp here has give me better results than using a single stage op amp. So, that is what I will do here I will read write with this op amp being a two stage op amp.

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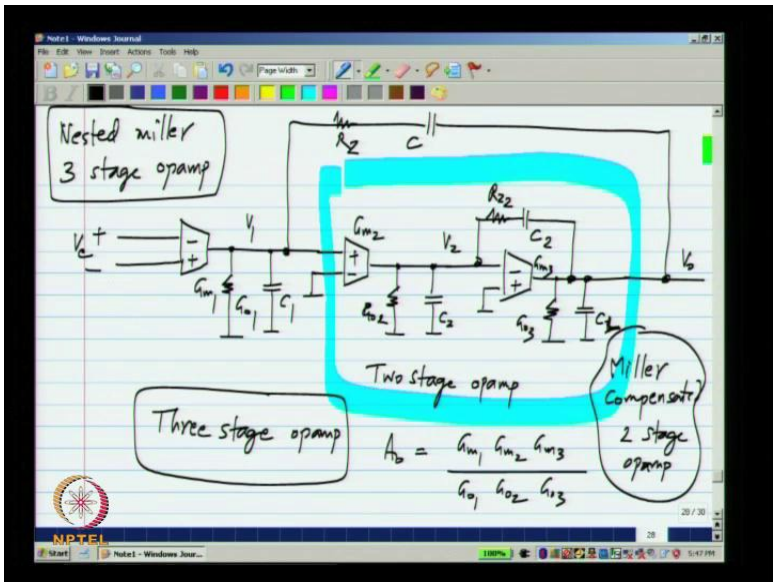

So, first let me draw the two stage op amp I will call this G o 2 and C 2, and G o 3 and C 3 and I will have and make all this C 2. Now, this forms my two stage op amp, and I have plus here and minus here because, that is the sense I want to implement the current control voltage source. This is my current control voltage source that is this part of the circuit, and I drive it with what I had earlier I will call this G m 1, it could have on output conductance G o 1 and there will also be a capacitance C 1 over sorry this is not grounded, this is the input to the op amp V e.

So, all I did was I know that a trans conductance driving a current controlled voltage source gives me a good op amp, and how do I make the current control voltage source I made it with the best op amp I have now which is the two stage op amp. Now, this entire

thing will give me the three stage op amp and fine we can go further, in practice it is not done although you can have even 4 or 5 stages right. And get better and better results, what is better about it first of all the reason we went to multiple stages in the op amp is to get higher DC gain.

The DC gain that you get from the first single stage op amp was not good enough, what is the DC gain of this stage. If I open circuit all capacitors I open all of this things I will simply have G m 1, G o 1, G m 2, G o 2 let me label these things G m 2, G o 2 and this is G m 3 and G o 3 all of them in castrate. So, the DC gain will be the product of the DC gains of the three stages, so this clearly is better than what we could get with a two stage op amp because, there we had only product to two stages.

So, let us see each stage has potentially as a maximum gain of the 50 than with a single stage op amp, you can get a gain of fifty the two stage op amp 25 100 and with the three stage op amp 12500. So, that is what is the advantages about the three stage op amp, now of course, you can write the node equations for this, there are three independent state variables in this case. I will call it V o V V 2 and V 1 and you can write it down and analyze it. And such an analysis is necessary for the complete design, but the expression will be, so complicated that we will not have any inside from them. So, I will only intuitively derive some conditions, first of all the unity gain frequency of the op amp that I would trying to realize is G m 1 by C.

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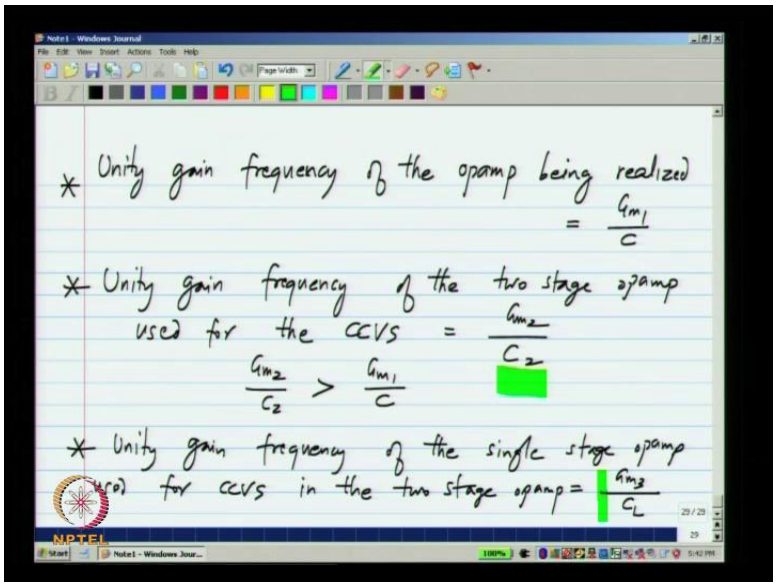

Now, the unity gain frequency of the two stage op amp use for the current control voltage source is G m 2 by C 2 sorry reduce the upper case G m s here, this is G m 1 by C and G m 2 by C 2. Now, clearly the current control voltage source has to function as a current control voltage source, over a frequency range beyond G m 1 by C only then we will get this integrating action that is a transfer function of G m 1 by S C from the input to the output.

So, this clearly means that G m 2 by C 2 has to be greater than G m 1 by C and this two stage op amp itself is made using a current control voltage source. So, I think I call this C L earlier let me go back to the terminology C L consist of any capacitance here plus external load that is applied. So, the unity gain frequency of the single stage op amp used for the current control voltage source in the two stage op amp equals G m 3 by C L and this clearly has to be more than that one. So, that the two stage op amp itself works properly, in fact, for the two stage op amp we did a rigorous analysis found the second pole, and this is the approximate value that we got this is the value that we got here I am only going through the intuitive stuff. In fact, if you evaluate the expressions you will see the exact condition.

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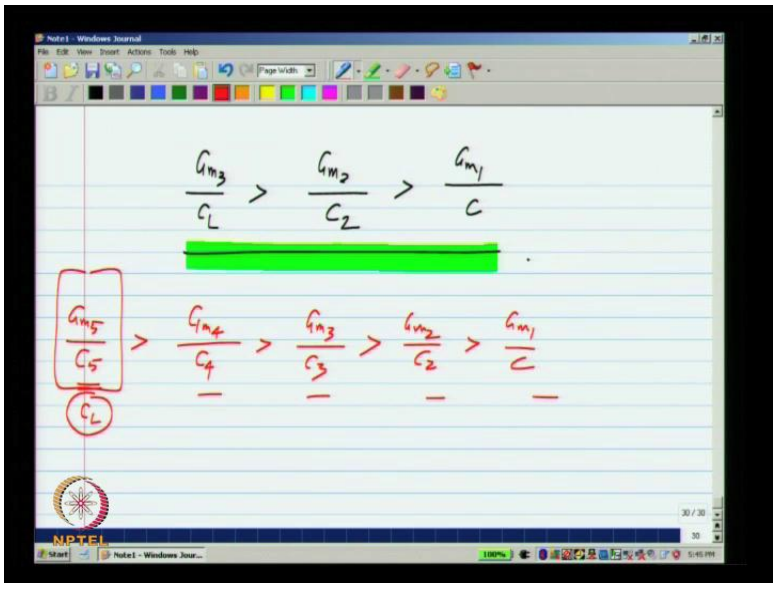

But, what this finally, says is the innermost op amp should have a unity gain frequency that is more than the unity gain frequency of the inner op amp, it is has to be more than the unity gain frequency that you are trying to realize. So, this also points to some

constraints like a see this is only an approximate description because, now the transfer function of this can be quite complicated, you will have the third ordered denominator and also you will have 2 0's because, of these parallel pass through the capacitors and, so on.

It is not very easy to figure out where those 0's are intuitively you can do it analytically, and then do it by the easily. But, intuitively this condition has to be satisfied, the unity gain frequency of the innermost op amp has to be more than that of the one outside it and which has to be more than that of the one outside it. And if you more stages let us say you go to five stage op amp then you also need to have, the innermost which is I will call G m 5 by C 5 which has to be more than let me write it separately G m 5 by C 5 has to be more than G m 4 by C 4 which has to be more than G m 3 by C 3 G m 2 C 2 and G m 1 by C and C 5 is nothing, but the total load C L.

Now, this condition also points you to some general constraint that is as you make op amp with more and more stages, we can only realize lower and lower unity gain frequencies. Because, typically there is an upper limit to G m by C ratios that you can realize because, what happens is even if you do not have an external load, the trans conductance itself will have some capacitances. And the ratios of G m 2 it, so inherent capacitance, there is a limit in any given technology.

As you go to smaller and smaller CMOS processes, this limit goes on increasing, but there is always a limit. Now, given that the highest one let us say you placed close to the limit that is possible, that is the ratio of the G m 2 the inner and capacitance is the highest that is implemented. Then you have to maintain all this things to be successively smaller, so; that means, that the highest unity gain frequency you can make a two stage op amp with is higher than, highest unity gain frequency you can obtain for a five stage op amp.

So, that is also the reason why you do not go crazy with the number of stages, although the higher number of stages will give you more DC gain, you only use the required number. So, three is a practical maybe four and five are done, but not, so often used and higher than that at least I have not seen, so that how you design multiple stage op amp. And because, by the way this kind of two stage op amp which has the C 2, and we earlier described C 2 as being miller multiplied and loading the first stages is known as a miller compensated op amp.

The two stage op amp that we discussed is a miller compensated two stage op amp, now you see that first of all the inside the op amp inside as a miller compensation, the outside one also has a miller like compensation. So, this entire thing is called the nested miller 3 stage op amp there are many variants of this to enhance stability and, so on, will not discuss any of those things. And just like we inserted a resistance in serious with these two eliminate the 0, we can also try inserting the resistances series with that and this as well in a various combinations.

All of the results of this has to be obtained from more complicated analysis and simulation, I will not discuss those things except to say that, that can be done. And there are lots of variants of this because, now you have more poles and 0's there will also more ways of trying to get rid of them. You can see the papers in the general for a state circuits or transactions on circuits from system for details of those things, one thing I want to summarize here is that, you can make multiple stage op amp, when we need higher and higher DC gains.

Let us say you want a DC gain of close to 10000 or a million here it is not possible to do with even two stages, we may have to go 3 or 4 or 5 stages it is possible. But, stability becomes a bigger concern because, of more poles and you are a maximum realizable unity gain frequency reduces. We started with a single stage op amp, and we try to make it better by passing the output current of the trans conductor, through a current control voltage source instead of directly through a capacitor. And that gave us a family of op amp that was better than the single stage op amp, now there is an alternative idea which also we can use that is this we traces back to the original discussion on negative feedback circuits, that gives a entirely different kind of op amp which also are of in interest of many cases.

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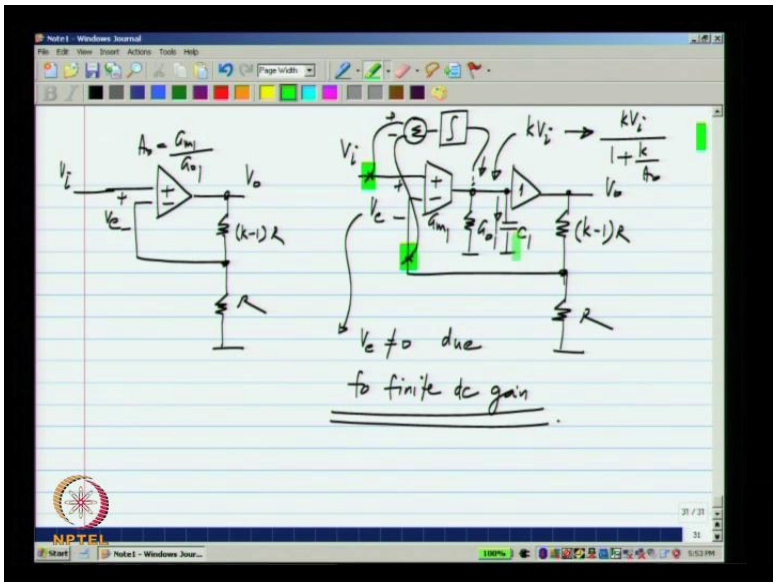

First of all let me consider the non-inverting amplifier that we designed long back, this is the input to the op amp that is the output and that is the input to the amplifier. Now, let me place a single stage op amp here, and this could have an output resistance G o 1, G m 1 that is it now I leaves a buffer to isolate this things just for simplicity. But, there still be DC gain limitation because, of G o 1 itself this is V o and because, of this finite DC gain even if you have a constant voltage V is not 0.

So, what happens is to support a certain output voltage, you need to have a certain voltage across G o 1. Which means that there has to be some current flowing through it and to have some current flowing through it, you need to have some voltage across this one that is the problem. So, in study state that is assume a constant input, there will be a difference between those two points when you implement this.

So, this is the same as this particular amplifier with DC gain of G m 1 by G o 1, let us go back to the basic idea of the negative feedback, what did we say had to happen. Basically in order to control some value to a desired value, we compared the desired and actual values, and then drive the output there is no that, that was the basic idea. Now, we know that this voltage which should have been K V i will settle to a value, which is less than that which is K V i by 1 plus K by A naught.

Now, the actual voltage is smaller than this one, and we can increase that by pushing more current into G o 1. If we some more manage to push more current into G o 1 we

will make this current voltage larger, and consequently the error smaller, now what is the desired outcome in a negative feedback system, the feedback quantity here must be exactly equal to that quantity there. In fact, with an ideal op amp that was happening right, if you add an integrator without a finite DC gain this is what was happening.

The severe capacitor of here C 1 that is what was going to happen, what we can do is this is the actual value we can compare to the desired value, and based on that control the current that is flowing there using an integrator. So, what we will do is, we will take that, will take that compute the error between two, now if V i is more than this value; that means, that there has to be more current flowing into G o in from top to bottom.

So, what we will do is, we will have an integrator and sum how make that push a current into G o that is the idea. So, another words just to summarize again, this feedback loops settled with a study state away between these two points, when we use this kind of an op amp. So, what we will do is we measure the error between these two points after it is settled that is it, and then we integrate that error further and inject a current into this output conductance.

So, once the current through the output conductance increases, this voltage is goes up this also goes up and the error will become smaller, it can be even become 0 if is the integrator is ideal right, it is very clear if this goes and integrating when the input is non 0 only way the study status when these two inputs are equal to each other or the input of the integrator is 0.

Now, this gives a different class of the op amps known as feed forward op amps which we will discuss in the next class. Now, one other thing that we can guess right away is that, we are assuming that the original circuit reaches that study state, and based on that study state error we are doing the integration. But, the integration itself is a continues operation what is really means is that, the second integration that we have here is much slower than the first one. It almost looks as though the first one reaches study state and based on the study state value we inject some current here.

In reality what will happen is the original one is though going through it is integration, and this is going through in it is integration all simultaneously it is just that, this integration has to happen slowly enough. So, that it appears as though the first one the

original loop as the reach study state, and you are measuring the study state error based on that injecting current into G naught will see the details of that in the next class.