Analog Integrated Circuit Design
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Lecture No - 12
Single Stage Op amp Realization

Hello and welcome again, so far we have looked extensively at negative feedback systems and out of design them how to design negative feedback amplifiers without significant ringing in the self response. So, now switch gears a little bit and actually tried to implement the integrator first at the control source level, and then finally at the transistor level.

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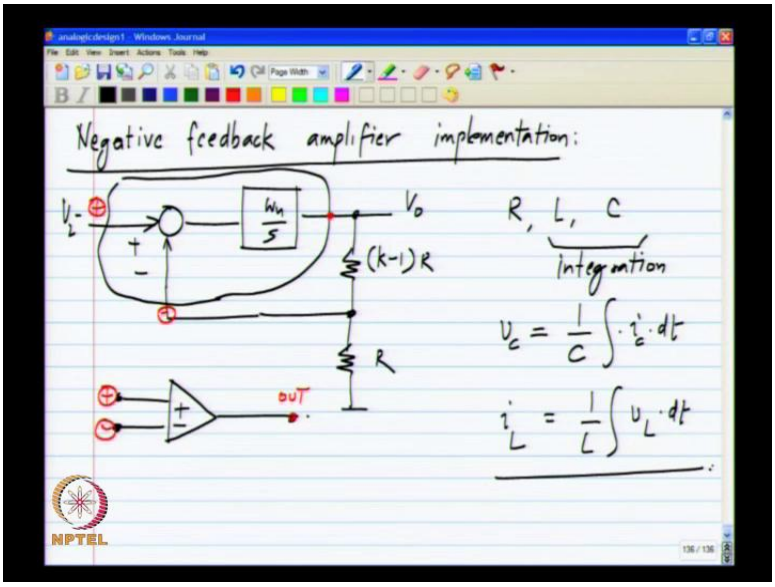

So, as you know this is an amplifier of gain k and we have investigated its behavior extensively be able to implement this. We need to have way to take the difference between the input and the feedback quantities and a way to integrated, and this combination of taking the difference and integrating, it is known as Op amp or the operational amplifier. So, this corresponds to these terminals we can think of this as a plus terminal minus and this is the output. Now, how do you actually go about implementing this one first of all we need to be able to make an integrator and we know of only two elements of the basic elements R, L and C, two elements which can implement integration.

So, the capacitor integrates the current into a voltage the voltage across the capacitor will be integral of the current flowing through the capacitor. Similarly, the current in an inductor is proportional to the integral of the voltage across the inductor. So, in principle we can use either of these to implement the function of integrating with respect to time, but in practice inductors are ordered to come by and more restricted in the range of values.

So, it is easier to make good quality capacitors than good-quality inductors and inductors also tend to be bulky and as you know this course is entitled analog integrated circuit design and on an integrated circuit everything is very small. So, you cannot use inductor as an integrator very effectively we have to use a capacitor. So, that is what we will do and our implementation of the integrator will consist of a capacitor.

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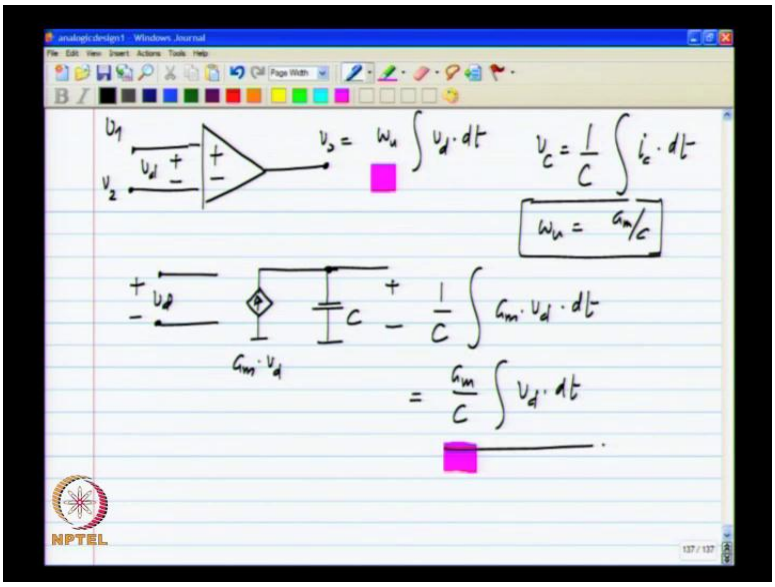

Now, a capacitor integrates the current flowing through it, whereas we want to integrate it may call this v 1 and v 2 and the difference is v d these are the inputs of the Op amp as we have defined and we want to integrate v d to get v o. We would like v o to be some omega u integral of v d with respect to time. So, first we need to convert the difference v d into a current and make that current flow through the capacitor narrate to do that is by using a voltage control current source. The voltage control current source will have a proportional constant G m and the current will be G m times v d.

So, this means that if difference v d is applied to the inputs of the voltage control current source, the voltage control current source raise a currents G m times v d and that is made to flow into a capacitor C. The voltage across this is 1 by C integral G m v d d t, which is G m by C taking the constant outside integral of v d d t. So, comparing these we see that the unity gain frequency of the integrator or the Op amp by itself is omega u which is G m by C. So, that is all there to it we now have a block that takes the difference v d and integrates it to give you v o.

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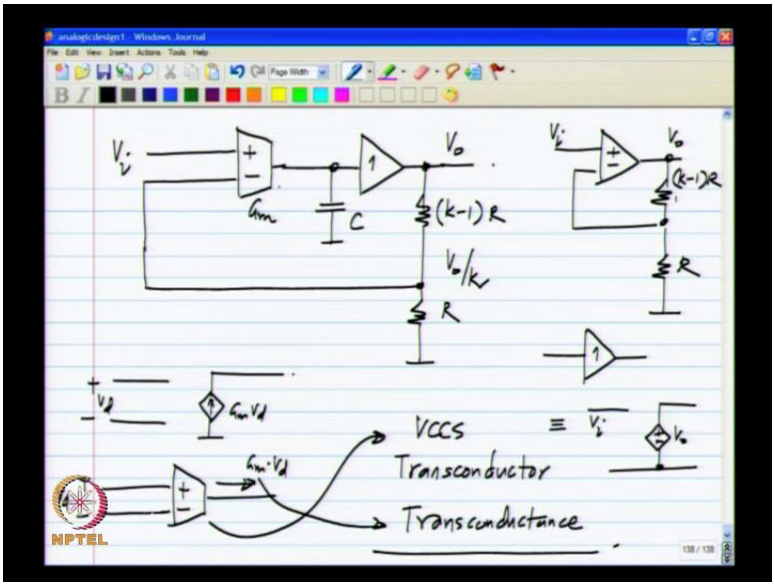

So, let us say if we can build our amplifier using this and we know that our amplifier as to look like this one, there are many kinds of amplifier you can build, but will still take our prototype amplifier that we started with the amplifier of gain k. So, here we have to have our resistive divider and this is v d and I will use the simple notation of simply writing G m, but it is understood that the current here will be G m times v d. So, think about this for a moment think about this circuit and see if it will work.

Now, if you look at this our idea was to convert v d to current and then make the current go through the capacitor, but now we have connected the resistive network. So, a part of the current will go through that. So, the voltage v naught is simply not the integral of v d and also has some other complicated terms and if this R happens to be very small, hardly any current goes through the capacitor and most of it will go through the registers. So,

this circuit by itself will not do we cannot use this because what we connect to the output disturbs the action of integration.

So, we need to insert a buffer here which I will denote like this means that the voltage here is exactly the same as a voltage there. This can drive a load can supply any current that is needed by the load this is equivalent to we have v i here it is a voltage control voltage shores of gain one. So, once the we do this our job is complete because now any current from the control source close into the capacitor and the buffer isolate the capacitor from what is happening outside.

Now, you can see that if you have a constant v i, v o divided by k which is being compared is different from v i. Then, a current will flow either into the capacitor or out of the capacitor and the capacitor voltage will go on changing the capacitor voltage will stop changing. It will remain static only if v i, v o by k happens to be exactly equal to v i or v o happens to be k v i, so this is the amplifier which we have learned earlier. So, this is the simplest implementation of the Op amp you need a voltage control current source under capacitor.

So, I will make one more changes to this diagram which is more of a notation change. So, an IC design it is common to denote a voltage control current source of this sort with this particular symbol which looks like the symbol of the Op amp with its no stop down. So, you have that difference v d and this means that if it is applied in this polarity indicated here plus minus a current G m times v d is forced out of the voltage control current source this is a voltage control current source also known as a transconductor and this G m is the transconductance. So, with that change the picture of my Op amp implementation will look like this and I will write G m here to indicate the trans conductor that is all there to it.

So, we have the Op amp, now what can be the possible problem with this because we know how to make voltage control current sources, we know that every most transistor or even by polar transistor is a voltage control current source. We can use it here in some form; the other will see exactly how to implement it, but before that let us see possible non ideologies. We can have when we come to the implementation what you think you think please about it for a moment what possible non ideologies. You can have now the obvious thing is that, you cannot make an ideal current source and ideal current source as

an infinite output resistance and any current source you make whether it is controlled or fixed will have a finite output resistance.

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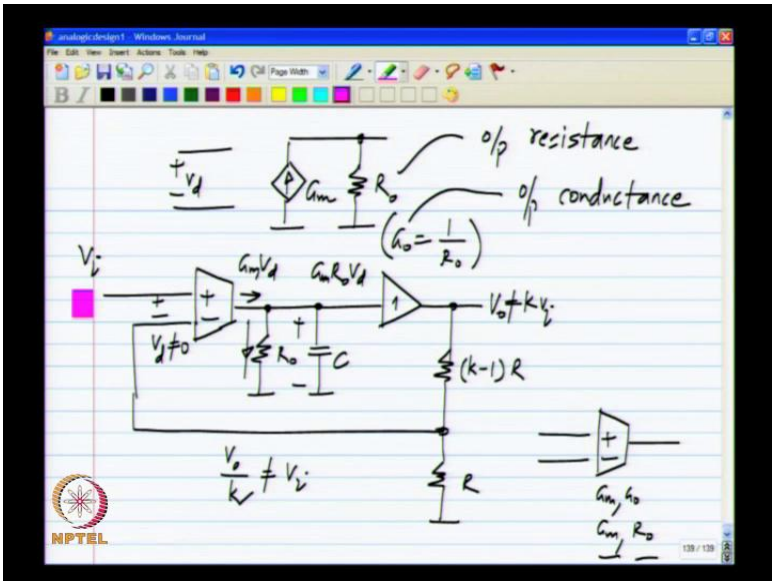

Which means that I cannot make this by itself it will always be accompanied by some R o or sometimes I will indicate by G o which is the reciprocal of R o the output conductance. So, what does this mean for our Op amp by the way this while using the new symbol embishun outside is sometimes just to make the schematic simpler. We may write G m and G o which means that this has a transconductance of G m and the output conductance of G o or alternatively we could even by G m and R o which means that it has a transconductance of G m and an output resistance of R o.

So, let us do that our amplifier and see exactly what happens this case I will showed explicitly outside, first let us reason out what happens and then analyze and see exactly what happens. So, again let us assume that v i is a constant and let us see what is the value of v o that we get earlier, if v i was a constant eventually v o would go to value which is k time v i.

So, that is how we got the amplifier, now let us see if v naught is k times v i this will be v naught by k which will be equal to v i. The different voltage of the transconductance is 0 which means that the current flowing out is 0 and because the current is 0 the current through the resistor will be 0 and a voltage across this is also 0, but we have a contradiction here if this is the 0 votes the unity gain buffer will make the output also 0.

So, there is a problem i mean this is the output cannot be at k times v i. So, what should happen is that v naught will be at some voltage which is not k times v I and v naught by k will not be equal to v i.

So, there will be some difference voltage here which is not 0 and that difference voltage should be such that G m time is v d and flowing through the resistor produces a voltage which is equal to v naught that is G m times R o times v d equals v naught. Note the time ignoring the current flowing through the capacitor because I am considering the steady state with a DC input in DC is steady state. There is no current flowing through the capacitor, so the difference should be such that the output G m R o v d equals v naught.

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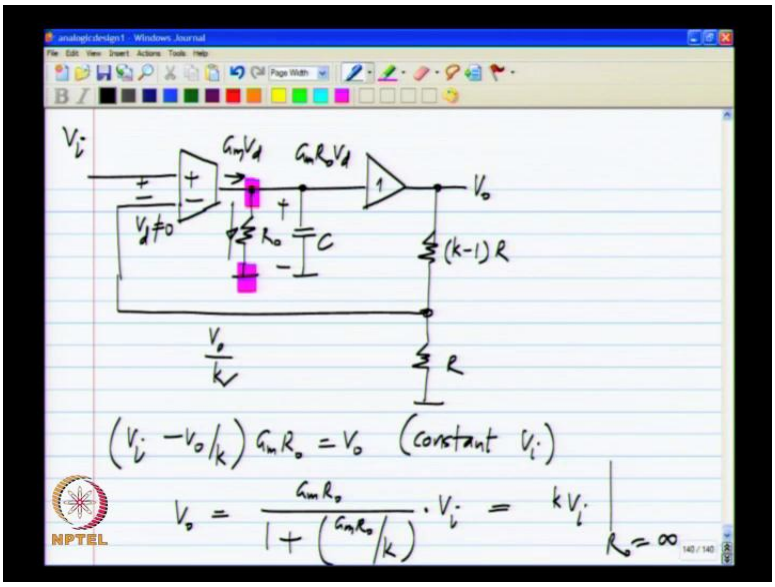

So, we can do the analysis exactly and see what happens, let us say v naught of some value and this is the v naught by k and v d equals v i minus v naught by k. That, times G m R o is the voltage developed across the register and that is the same voltage that is given out is v out. So, this is equal to v naught. So, this says that v naught is G m R o divided by 1 plus G m R o by k v naught is G m R o divided by 1 plus G m R o by k, sorry times v i and this is for constant v i that is v i is DC. We can see that in the limiting case, where R o goes to infinity this is k times v i when R o is infinity.

So, it passes the sanity check whatever case we had originally with ideal to voltage control current source this satisfies that one that corresponds to R o equals infinity. So, when our R o is not equal to infinity R o is less than infinity, this number will be smaller

than k. So, that is very obvious if we write it in an alternative form which is k 1 plus k by G m R o times v i.

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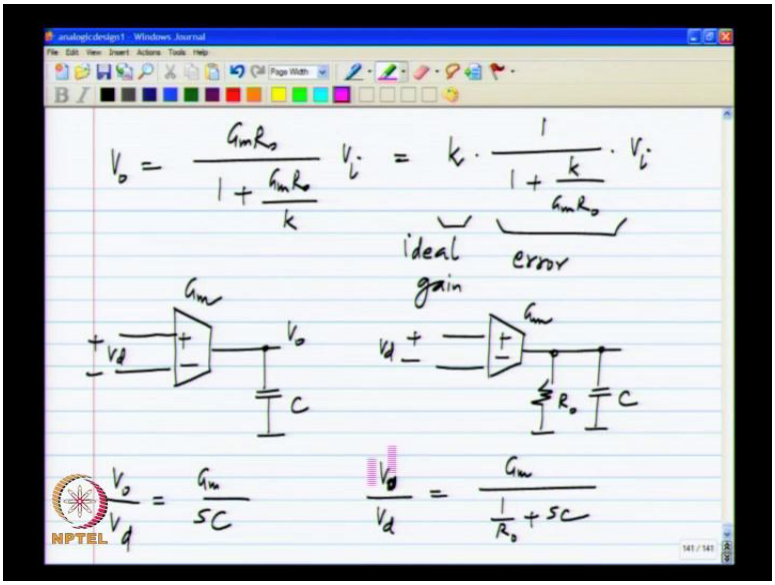

So, we have the ideal gain here and we have an error here due to the fact that R o is not in finite. So, we can analyze this little more and interpreted what interpret what it means, so first we let us look at what is the transfer function of the Op amp in this case. So, ideally be wanted the Op amp to be like this that is without any output resistance in the transconductor and the transfer function of the Op amp was G m by SC and G m by C is the unity gain frequency omega u, but in reality we have v d we have G m and we also have R o. So, in this case v naught by v d will be gm divided by the total admittance that output which is 1 by R o plus SC. So, we have an extra term and the pole which was at the origin as more to different frequency in this case, the pole is that the reason and in this case the pole is at a different frequency.

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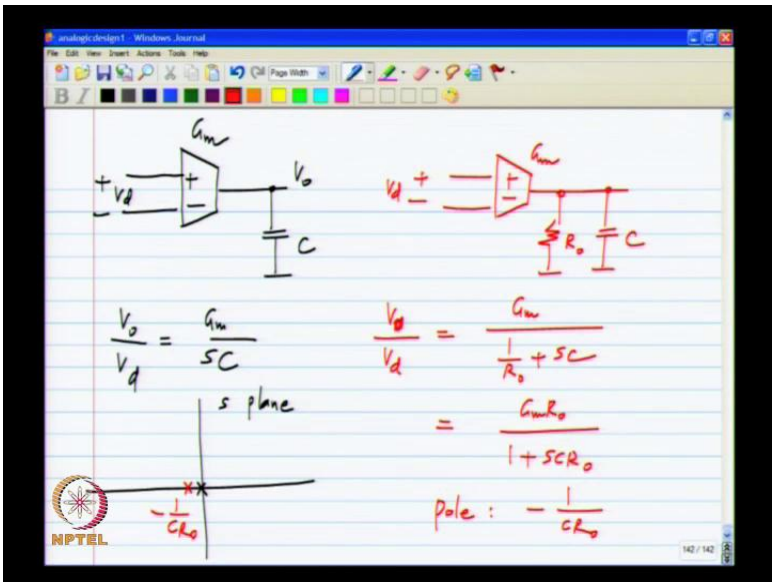

So, let me make this of a different colour just for distinction, so if you look at explain originally the pole was here. Now, this can be written as for instance G m R o 1 plus SC R o and the pole is at minus 1 by C R naught. So, the pole moves into the left of plain and exactly much it moves depends on the value of R naught the higher the value of R naught the lesser the movement into the left of plain. So, that is what it looks like and we can also look at the magnitude and phase of the two Op amps that is the ideal case when there is no R naught or R naught is infinity and the actual case when there will be a finite R naught.

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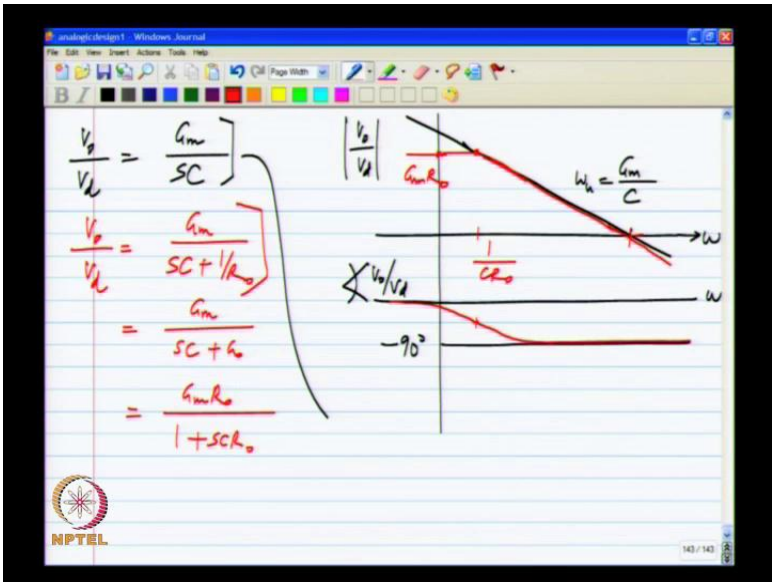

First I will draw it for the ideal case in magnitude will be like that and this is G m by C which is the omega u of the Op amp this is the magnitude plot of the gain of the Op amp in the phase plot. Of course, simply is that minus 90 degree or minus 5 by 2, now what happens in practice we will get this could also be written as G m by SC plus G naught or an a number of other ways or G m R naught by 1 plus SC R naught.

So, first of all at very low frequencies this is does not go to infinity. So, it goes to G m r naught and at frequency 1 by C R naught is has a pole and after the pole it drops down at 12 d v per decade. Notice that I would draw the black line and the red line to be coincident after 1 by C R naught. This is because if we look at the gain of this particular function when omega equals j by C R naught what you get at omega equals j by C R naught the magnitude of this is G m by 1 by C R naught time c which is equal to G m r naught.

So, at this particular frequency even the integrator has same gain. So, in body plot sense the red line meets the black line and then follows the black line because after that the slope is 20 d v per decade for both of these curves. So, this also means that even this one intersects the unity at a frequency approximately G m by c. So, we will conform that to the calculation later, but that is what happens.

So, the magnitude response of the non ideal Op amp follows I mean is a constant G m r naught up to a frequency 1 by C R naught after that it follows the same frequency response as that of the ideal Op amp. So, similarly, the phase plot it does not start from minus ninety which starts from 0, but at 1 by C R naught, it goes to minus 45 degrees and soon after that it goes to minus 90 degrees. So, the different occurs only in the low frequency range in at a frequency 1 by C R naught and surrounding it at very high frequencies that two transfer functions are identical.

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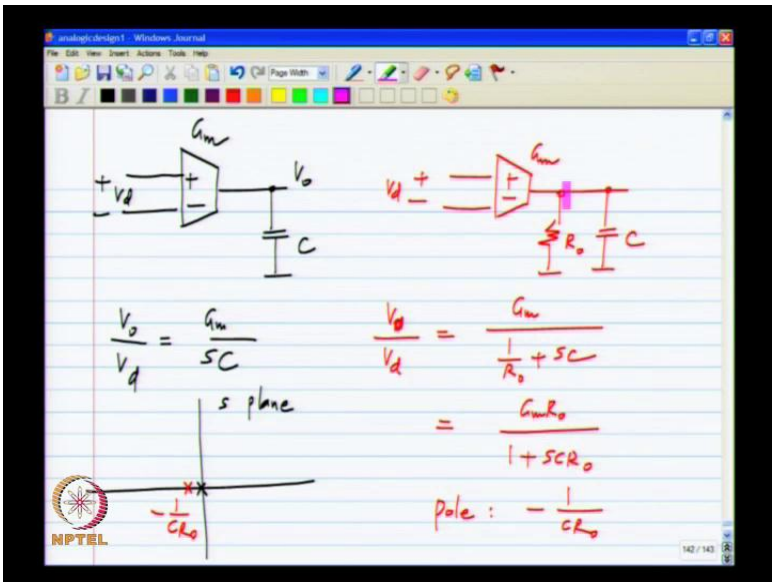

So, in circuit times what does mean is that if you think about it at low-frequencies the all of the current from G m goes into R naught whereas, in the ideal case the current from G m always goes into the capacitor. So, that is the substantial difference for at high frequencies what happens is the impedance of the capacitor is much less than the impedance of this output resistance r naught. So, most all of the current or most of the current from G m goes into the capacitor which is the same as in the ideal case.

So, this means that high frequencies these two r moreover less at the same at low frequencies they are not the same because the current from G m goes to r naught here. Whereas, C R even at low frequencies it has to go to C and from the analyses also it is clear low frequency is there is a difference in characteristics at i frequencies. There is no difference and just for completeness will calculate when the magnitude response here goes to unity to be unity.

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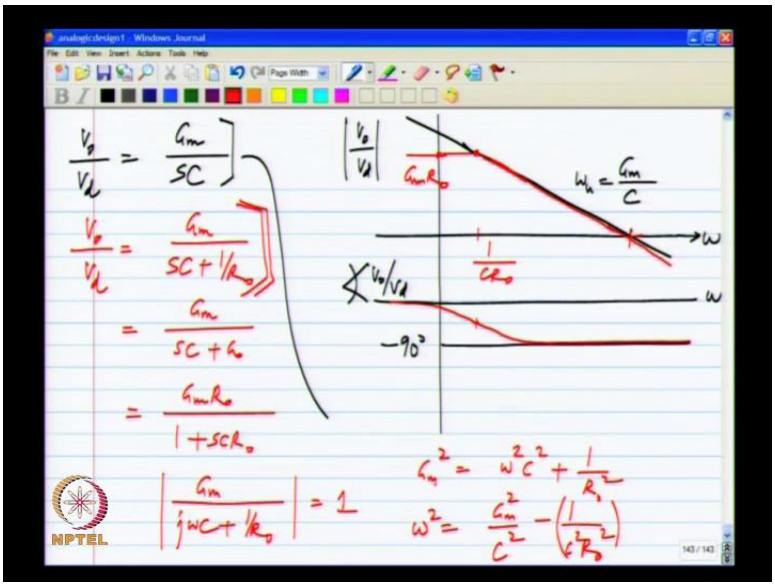

So, this means that G m square is omega square C square plus one by R naught square. So, omega square is given by G m square by C square minus 1 by C square R naught square. So, as long as this is very small as long as one over C R is much smaller than G m by C the unity gain frequency is still approximately G m by C. This is invariably the case for any reasonable Op amp because of this condition is violated the Op amp will be almost useless.

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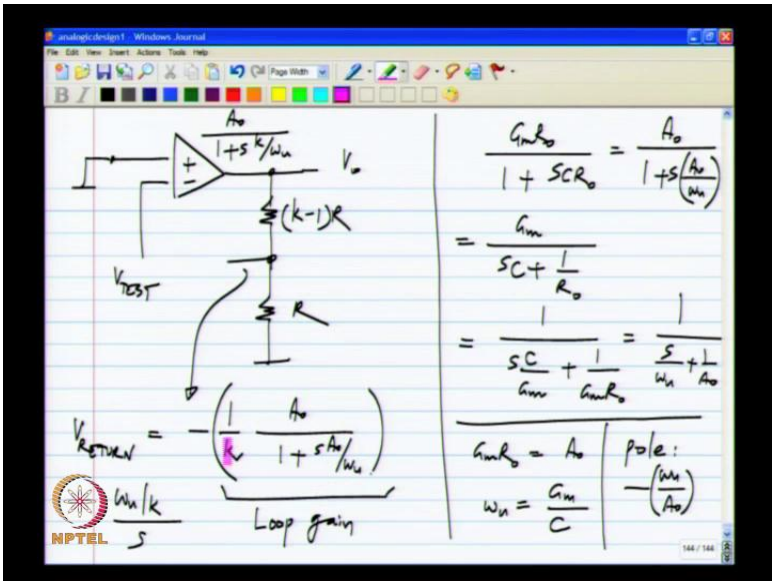

Now, let us take a look at this whole thing in turn to the loop gain of the system. So, we have an Op amp was transfer function is not of the form omega u by S. So, let us write it in general terms the actual transfer function is G m r naught by one plus SC R naught this is one way divided or we can write it as G m by SC plus 1 by R naught are equivalently also has one over SC by G m plus 1 by G m r naught. So, I will denote G m R naught by a quantity A naught and this A naught is the DC gain of the Op amp, as you can see if I apply DC increment v d the output DC will be equal to G m times R naught times v d.

So, the DC gain is G m R naught and we know that the unity gain frequency omega u we had defined it as G m by C I will keep it as it is. So, this form if I choose I can write this as 1 by S by omega u plus 1 by A naught and this kind of makes the non ideality very clear, if A naught tends to infinity you will get omega u by S as that transfer function. But it can also be written in number of other ways if i write it in the first form I will get A naught by 1 plus S omega u by A naught, sorry A naught by omega u.

So, note that I have not made a notation for p 1. So, we have three related parameters here the DC gain G m R naught the pole 1 by C R naught and the unity gain frequency of the original Op amp G m by C, I will always use the DC gain frequency of omega u and the DC gain A naught as the primary parameter and the third one can be derived format. So, pole is at omega u divided by A naught the poll of this system is at minus omega u by A naught.

So, ideally A naught as infinity in practice, it is a large number which means that the pole of the Op amp will be at much smaller frequency compared to the unity gain frequency the pole should have been at the origin, but it is at a small frequency which is naught at the origin. So, instead of this we will have A naught by one plus S k by omega u v i and v naught. Now, we have evaluated the systems of this type and we quantified the amount of negative feedback by loop gain and we said that whenever the loop gain is very large.

The system will behave ideally and whenever the log any small the system will not behave ideally and our original system when the Op amp was an ideal integrator add an infinite DC loop gain infinite DC gain. As the consequence, it also had an infinite DC loop gain, now let us evaluate the loop gain by setting the input to zero applying v test

voltage here by breaking the loop and saying what comes back. So, it is clear what is comes back, if I apply v test I get minus whole thing is time v test here and then that divided by k appears at the output of the resistive divider.

So, the return voltage v return will be minus 1 by k denote e naught by 1 plus S k by omega u and the loop gain is nothing but what is enclosed in this parenthesis excluding the minus sign. This is the loop gain and again just the quick recap the loop gain without this non ideality without the finite output resistance was omega u by k divided by S. You can easily see that if A naught goes to infinity this reduces to that, sorry this is not S k by omega u. It is A naught by omega u if A naught goes to infinity you will simply get 1 by k times omega u by S.

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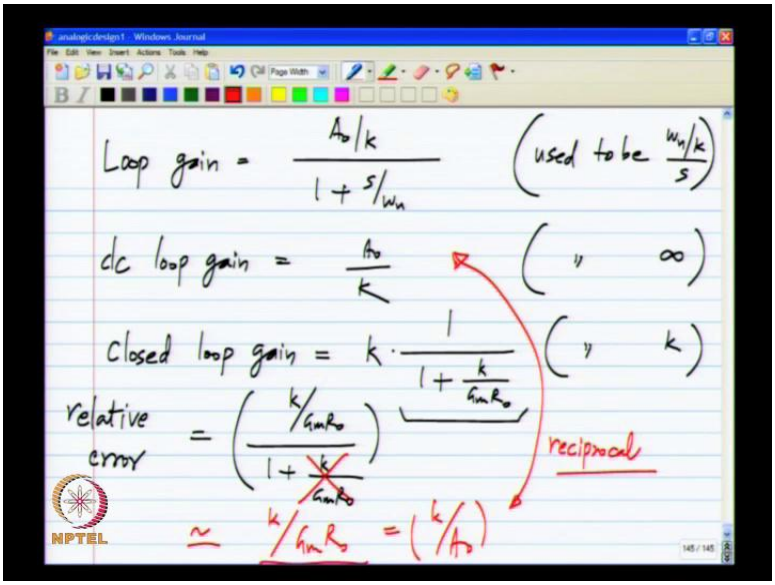

So, the key point A naught is that and it use to be that one, if I look at the DC loop gain it is A naught by k and this use to be in finite. So, and if you look at the close loop gain it is equal to k 1 plus k by G m R naught. So, let us it strictly go back and see that what we had, so if you see this is the expression rearranged to get that point there is an error. So, this is what we have and this used to be k, so if you look at the relative error in the gain relative error means the ideal gain minus the actual gain the difference in the gain this will be simply that and if I further simplify it, I will get that. So, that is my error in the gain that is the difference between the ideal and actual gain and that I normalize to the gain that I want k. So, that is the relative error that is how much the relative error is and

we would naturally want the relativistic to be small like a percent or point 1 percent are sometimes even less than that.

So, this means that this number k by G m R o has to be very small and this is also kind of expected because ideally G m R o was infinity. Now, we would liked to be as our just possible, so what we can do is simply neglect this k by G m R o in favour of one and approximate the relative error to be k by G m r naught. So, that is the relativistic and as you see this is k by A naught k by the DC gain of the Op amp and this is nothing but the reciprocal of DC loop gain and again this is not a coincidence please think about how this happened originally the DC loop gain was infinity. So, the relative error was 0, now the DC loop gain is A naught by k the relative error is k by A naught.

This is not a coincidence this is how it should be because loop gain quantifies the amount of negative feedback this is to have infinitely strong negative feedback at DC, now it is only finitely strong. So, we have a finite relating where and this also not surprising we have seen these earlier while evaluating the close loop frequency response of a negative feedback amplifier. We saw that the these the loop gain was omega u by k divided by S are in general some omega u loop divided by S.

So, the loop gain magnitude is very large for frequencies below omega u loop and the loop gain magnitude is small for frequencies beyond that. We have seen that the close loop gain is close to 1 for frequencies below omega u loop, where the loop gain magnitude is large. It does not follow the negative feedback amplifier gain for frequencies beyond omega u loop. So, the loop gain being large means that there is less error is, but in this case the loop gain is not infinitely large.

So, there is the relative error and the related is exactly the reciprocal of the loop gain. So, this is one of the problems with the implementation of negative feedback amplifier that you will always have a current source with the finite output resistance which means that you will get a finite frequency gain. So, what was an ideal amplifier at DC, before is no longer ideal even at d C, so that is the bottom line.

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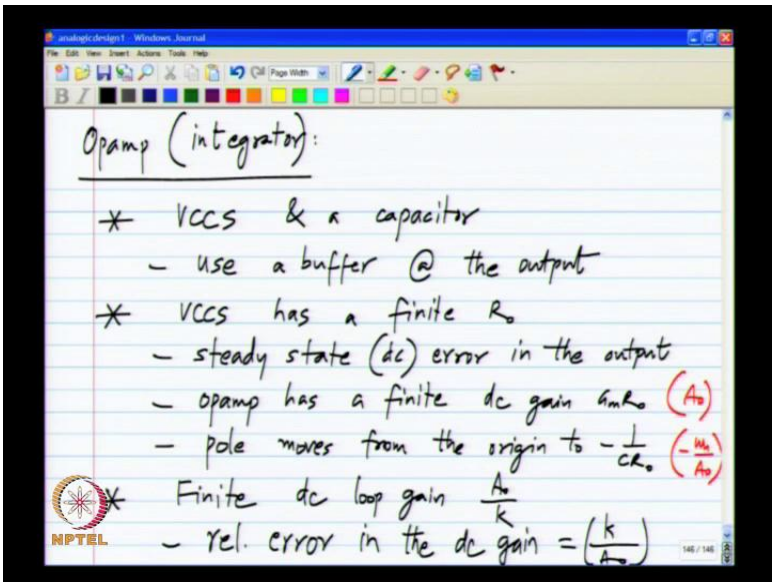

So, to summarize implement and Op amp which is an integrator, we need to have some integrating function and which we do using a voltage control current source under capacitor and we also used a buffer at the output. So, has not to disturb the current flowing through the capacitor due to the load now the problem is that VCCS has a finite output resistance. So, this means that there is a steady state error that is even for a DC input for an input that is constant the output will not settle to k times the input, it will settle to something like some something slightly smaller than k times the input.

So, this is known as a study state error or a DC error equivalently, we can think of this as the Op amp has a finite DC gain G m R o and because of this the pole moves from the origin to minus 1 by C R naught. So, in more general terms the Op amp will always have a finite DC gain, A naught which is not infinity and the pole moves to minus omega u divided by A naught where omega u is the intended unity gain frequency of the Op amp.

Finally, the result of this is that you have a finite DC loop gain which is A naught by k which gives a relative error you can think of it, a relative error in the DC output or relative error in the close loop DC gain of k by A naught that is the reciprocal of the loop gain. So, this is one of the implementation problems that we have to deal with right, because we cannot make ideal current sources we have leave with finite DC gain and this causes an error even in the DC gain of the amplifier.

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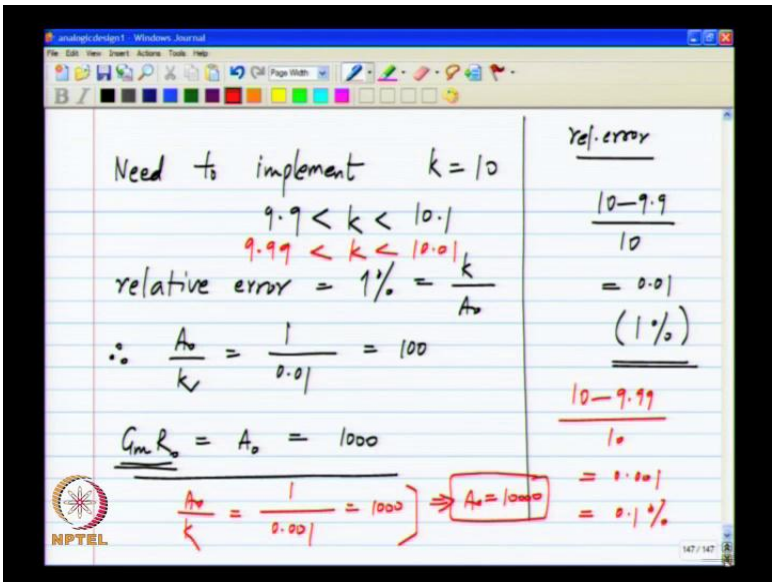

So, just you get a feel for numbers let us say I want to implement an amplifier of gain 10, we know that I am going to get an error and I would like the relative error to be less than something and I will say that my k as to be between 10.1 and 9.9. So, now we know that the finite DC gain of the Op amp will make the gain smaller. So, it is going to be about 9.9, so what is the relative error here 10 minus 0.9 divided by 10 which is equal to 0.01 or 1 percent the relative error 1 percent.

So, we need is sufficiently high DC loop gain this we know is k by A naught the reciprocal of the DC loop gain. Therefore, the DC loop gain as to be 100 and therefore, the DC gain of the Op amp G m times R naught which is A naught should be a 1000. So, this now put some more constraints on the Op amp before we are only concerned with implementing a certain unity gain frequency which lets us choose a certain capacitor C and is a time transconductance G m. Now, we also have to make sure that whatever circuit we use to design the G m should have sufficiently high are not and how high is it. It should be search that G m R naught is thousand for this particular example, now this is not the some fix number.

So, it could be that in some cases I want the gain to be controlled even better I wanted to be between 9.99 and 10.01. So, in this case the relative error is 0.001 which corresponds to find 1 percent, so obviously, for this particular example A naught by k should be 1 by 0.001 or 1,000 the DC loop gain itself as to be 1,000. So, that you get a 0.1 percent

relative error in the gain or 0.1 percent relative error in the DC output steady state output and this implies that A naught as to be 10,000. So, the more the accuracy you want the higher value of A naught you want, so which means that you take more care in the design of your Op amp.

So, that it gives you a high DC gain finally, the DC loop gain is the DC gain of the Op amp times whatever is the gain of the feedback network if you want to make an our non inverting amplifier of gain 10 the gain of the feedback network is 0.1. So, the gain of the Op amp has to be 10,000, so this put some additional constraints on the Op amp and also this is the reason why we have to go for more and more complicated topology in some cases. You may end up with having to need an Op amp gain of 100, 1,000 or a million in this case the structure of the Op amp can be very complicated.

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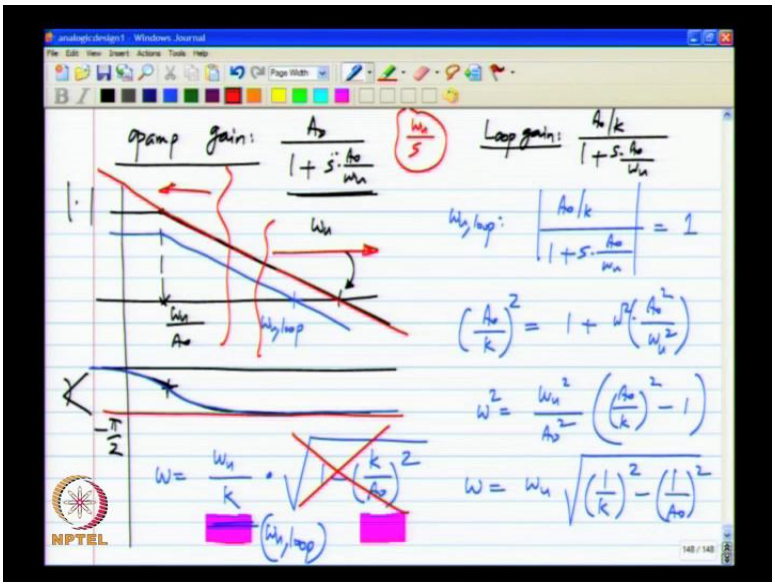

So, before going to a new topic, let us just see what happens because of this at high frequencies the Op amp gain is A naught by 1 plus S A naught by omega u. So, I will draw the magnitude and the angle of this one, so that is what it look like and ideally this should have been simply omega u by S which means that the magnitude gram in like that. Similarly, ideally the phase would have been that way and in reality the phase would be something like that where this frequency is omega u. We said that even for the Op amp with the finite DC gain it is approximately is omega u this frequency is omega u by A naught and this angle is minus 5 by 2.

Now, we have done a lot of study have to loop gain, so that the close loop system is stable. So, now we would also like to see if this problem of finite DC gains as an effect on that because we did a lot of hard work, lot of analysis. Now, if we have to go and change it all again because of this finite DC gain problem, it will be a waste. Now, let me specify the loop gain the loop gain is what matter is not the gain of the Op amp all have done this have taken this expression and divided by k this is the k is our proto type amplifier.

So, what does it mean as for as the magnitude is concerned is simply shifted down and I have to do is to shifted down that curve. In fact, it is better to pull down the same plot, I will do that and what happens to the phase as you can see nothing happens to the phase because I only divided to the loop gain by real number. So, nothing happens to the phase, so the phase follows the same curve and this is my unity loop gain frequency. So, omega u loop is where the magnitude of A naught by k divided by 1 plus S A naught by omega u becomes 1.

Now, the reason i am got it about it does I said is we get lot of hard work lot of analysis and we do not have want to have to re do everything. If we can help it we have to see what happens to our conditions etcetera because of the DC gain, now one of the things you remember is that from the Nyquist plot, first ability the area of interest is around minus 1, 0 that is the are looking at when the magnitude of the loop gain becomes close to 1. We are not interested in what the magnitude of the loop gain is when it is very large that low frequencies, the stability depended on like for instance if you recall the condition at greater than four times the unity loop gain frequency and it must beyond the unity loop gain frequency and so on.

So, what we are interested in is when in the region around where the loop gain becomes unity. So, let us solve for this you will get A naught by k square to be 1 plus omega square A naught square by omega u square. So, if I simplify this, I will get omega square to be omega u square by A naught square times A naught by k whole square minus 1 or I will take A naught inside omega to be omega u times square root of 1 by k square minus 1 by A naught square. I will further rewrite this is omega equals omega u by k times square root of one minus k by A naught whole square I wrote it in this form because omega u by k is the unity loop gain frequency. If we did not have finite output resistances, if we did not have finite DC gain if you had an infinite DC gain.

Now, we see that it is that frequency time something square root of a and minus k by A naught square and remember this k by A naught is a very small number, that is the relative error in the DC gain and by design we would make it very small. So, it is safe to neglect that one because by design we would make k by A naught very small.

So, the unity loop gain frequency even when you have at finite DC gain is approximately is omega u by k and that part has not changed. This is good news for us because all are stability criteria, which is specified something about the unity loop gain frequency are the same as before. We can judge stability by looking at this type of function omega u by k S, assuming that is an ideal integrator even without worrying about the finite DC gain, because the finite DC gain affects only this part of it and the stabilities determined by what is happening in this part where the loop gain is coming close to unity.

So, this means that is a very useful approximation for stability calculation to still assume an ideal integrator even if you have a finite DC gain as long as the DC loop gain is large. The DC loop gain will be large in any decent negative feedback system, that you design otherwise even at DC you will have a large steady-stator. So, that end this lecture we have looked at how to try and make the Op amp and it brings one particular non ideality, which is the finite DC gain.

We saw what the effect is it is effect is mainly at DC and we have to make the DC loop gain large enough to get a sufficiently small steady state error. Now, it can also affect the stability in general, but the examined it and seen that if we make the DC loop gain large enough the stability criteria are not affected. We can evaluate the stability assuming that it is still an ideal integrator. This is very good for analysis all the analysis that we did earlier, we do not have to modify them at all.

Thank you, see you in the next class.