Analog Circuits and Systems through SPICE Simulation
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Lecture - 09
Basic Analog Design Part III (Contd.)

Good afternoon everyone and welcome to.

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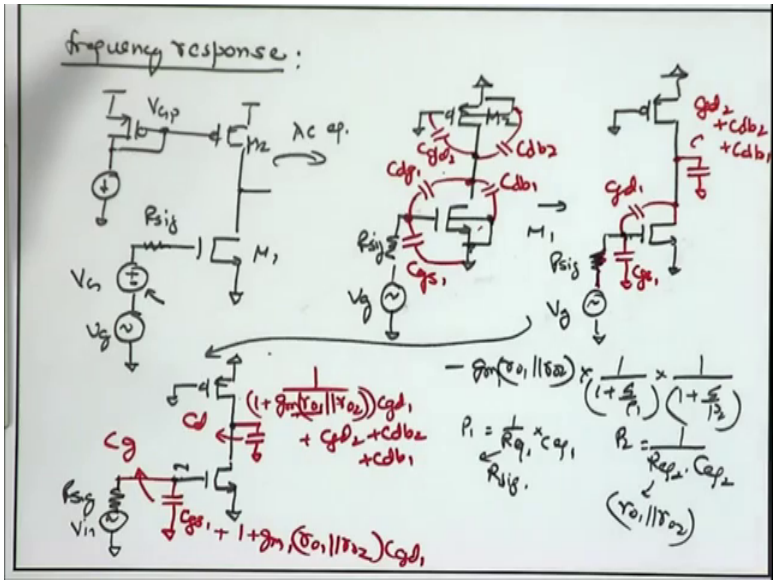

Now let us assume that the source is not an ideal source you have some source resistance. So, in general that may be driven by some other amplifier stage right. So, it may be coming from other common source amplifier or differential amplifier and we know that output port of such amplifier you may is represent it as say output for output port of an amplifier any other amplifier you can represent it as current source.

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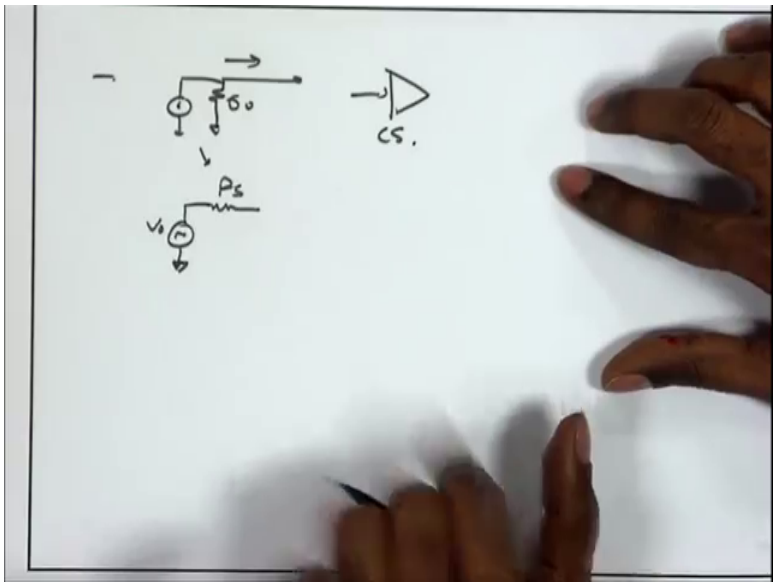

And the corresponding r o which is going to the next stage I can also represent it as equivalent voltage source V o and r s. So, in general when one of the amplifier is being driven by the previous stage. So, above this is going to the next stage amplifier that we are right now considering this is my active common active load common source amplifier this is my common source amplifier and it is getting signal from the previous stage.

So, I can model that previous stage as say equivalent model where the output signal is in series with the r s the source resistant active source resistance of the previous stage. So, I can represent you have the DC bias again we are not going to detail how you are getting this DC bias suppose if somehow you are able to bias the gate voltage. And then on the top of that you have the signal swing the AC signal with source resistance. So, you are having the r signal over here which is capturing this source resistance now in this case how do we find out the frequency response high frequency response for that we have seeing yesterday the shortcut to do this is to find out the r c time constants at the circuit nodes.

So, in this circuit we have already seen that this V G P is a constant this is the DC value ideally. So, I can comfortably treat this as an AC ground. So, AC point of view AC equivalent circuit if I want to draw the V G P is at AC ground the source of the m 1 m 2 is also at AC ground because connected to V d d I am setting the capital V g to 0 for AC

analysis. So, you are having r signal and you are having V g source is AC ground this is the AC equivalent circuit actual lower frequency now if I want to go for higher frequency in capture the effect of the parasitic capacitances once again you need to draw the variance capacitances contributed by m 1 and m 2.

Now, consider that the substrate of m 1 is grounded we have seen that for nmos is the substrate sub should be at the lowest potential ground in there I c and likewise for the PMOs the substrate should be at the highest potential that is also V d d that is also ground. So, that eliminates 1 of our capacitances between the body and the source. So, the c s b is eliminated because of this AC ground you may have DC potential between the body and the source, but both of them are constant they are fixed to DC potentials another result both of them are AC ground. So, there is no AC potential there is no change in this potential across V s and V b as a result the small single V s b is 0 and I do not need to care about the effective small signal capacitance between V s and V d.

Or I need to take care of others which is c d g 1. Now c g s 1 is appearing between gate and the source which is once again AC ground and finally, we have the c d b 1 appearing between drain and body which is once again AC ground. So, this is also appearing effectively between drain and body AC ground likewise for m 2 once again you have the c g d 2 between the drain and the AC ground and likewise at this node I have the c d b 2 between the drain and the body terminal of m 2 which is again and AC ground.

So, if I further I want to simplify this complicated looking high frequency model I can redraw the circuits little bit with simplified capacitance. So, if I look at the c g d 2 at this node that is appearing between the drain and AC ground also c d b 2 is appearing between drain and AC ground. So, basically we have an effective capacitance at this node between you know c g d 2 plus c d b 2 likewise I have the c d b 1 appearing between this node and AC ground.

So, what we can say is c g d 2 plus c d b 2 plus c d b 1 is the effective small signal capacitance between this node and ac ground. So, I can write this as total combined value c g d 2 plus c d b 2 plus c d b 1 on the input side we have c g s 1 between the drain gate and the AC ground. So, this is c g s 1 and then we also have c g d 1 which is appearing between the gate and the drain.

So, we have this c g d 1 between the gate and the drain and then we have the r s r signal and the a signal source now where we have seen yesterday how to tackle small signal capacitance appearing between 2 nodes we want to reduce the circuit to a simplified you know equivalent ac model where we having small signal capacitances appearing between the unknown node voltages and ac ground we do not want small signal capacitances between 2 unknown node voltages. So, here once again I can apply miller law on c g d 1 and further simply the circuit.

So, at the output finally, if I break this c g d 1 into and equivalent capacitor I get remember 1 plus a this is 1 plus mod a. So, this is going to be 1 plus in this case g m r o by 2 or basically more accurately r o 1 parallel r o 2 times c g d 1 coming into picture and plus all the previous term which is c g d 2 plus c d b 2 plus c d b 1 sorry, I am just sorry this is this is I have just in the opposite thing. So, here it is 1 upon whereas, on the opposite side on the source terminal we have c g s 1 and here we get the 1 plus a on the other side we get 1 plus 1 upon mod a here we have the equivalent capacitance coming as 1 plus g m 1 r o 1 parallel r o 2 times c g d 1 and this is my equivalent capacitance this particular node.

So, what I have done is I have found out the small signal capacitance between my 2 nodes and AC ground and now the remaining task is to find out the small signal resistance between the 2 nodes and AC ground that is going to give me the r c time constant at the 2 nodes at the first node and the second node and that is going to give me the 2 poles. So, remember what we did in the last class was we have the low frequency gain of the amplifier which is minus g m r o 1 m parallel r o 2 this is, but applied by the 2 factors the 2 poles because in this circuit node in the circuit we have 2 nodes. So, this is gets multiplied by 1 plus s upon p 1 and 1 plus s upon p 2 where p 1 and p 2 r 1 upon r equivalent 1 times c equivalent 1.

So, we have found out c equivalent 1 what is the equivalent small signal capacitance between the node 1 and AC ground likewise you have to find out r equivalent 1. So, what is the r equivalent 1 between this node and AC ground looking into the gate MOSFET has infinite impedance ideally. So, infinite small signal resistance looking into the gate on the other side we have small signal resistance equal to r signal that is between the gate and the AC ground that is r signal. So, I can just say this is going to be r signal what about p 2 what is 1 upon r equivalent 2. So, c equivalent 2 we have already found out.

So, this is the expression for c equivalent 2 which is given and I also need to find out what is the r equivalent 2.

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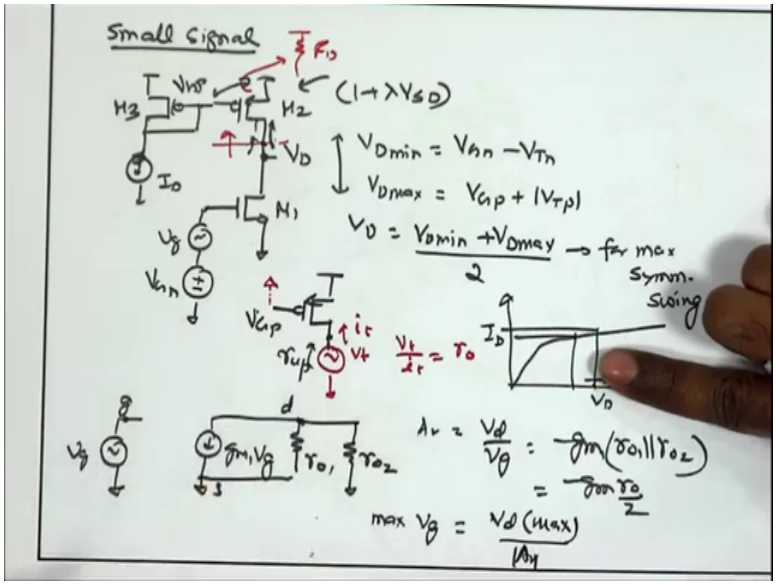

So, once again if I go back to my small signal model and I try to see what is the small signal resistant between the drain node that is this output node and the AC ground that is once again just going to be parallel combination of r o 1 and r o 2.

So, r equivalent 2 that is the small signal resistance between drain and ac ground that is just r o 1 parallel r o 2, so, we have write r equivalent 2 is r o 1 parallel r o 2. So, this gives me the value of the 2 poles we are looking at now depending upon the circuit 1 of these poles can be higher another one can be lowered. So, for example, if this previous source hap previous stage happens to be a common source amplifier where differential amplifier with resistive load where the load resistance is pretty small maybe 1 kilo ohm 2 kilo ohm. So, in that case despite this capacitor being large be despite having a large multiplication for this c g d 1 here and resulting in effectively large c g let me call this c g total value c g and let me call this total value c d.

So, despite having this large multiplication miller miller multiplication if I having r signal small. So, suppose the output in between the previous study small this can still be you know higher, but in general if it is being driven by a similar stage with this kind of active load the previous stage is also having similar output resistance r o 1 parallel r o 2 and here you are having large miller miller multiplication as a result this can be the

dominant pole because this can be the lower frequency as compared to p 2 where the total capacitance is relatively small. So, if I assume that the r equivalent that these 2 nodes are similar in that case this node is going to gives us dominant pole because of this miller multiplications factor.

So, once again this is going to be the frequency limiting or band width limiting node because if this is high impedance source r signal is high coming from a previous stage which is having relatively large output resistance we are going to have r c time constant over here large because of miller multiplication factor another result this node determines my 3 d b cut off frequency this is the lower of the 2 poles.

So, we will covered you know how to get the bode plot and do the stability analysis for multi pole that we have not covered yesterday we have just looking to the 3 d b cutoff frequency for a single pole system. And we have looked at the 20 d b cut role off that happens after the first pole, but in case of multiple poles once again you have 20 d b and after the second pole you have 40 d b per decades slope though those things will be covering tomorrow when we get to the stability analysis of our feedback amplifier for the frontend.

Now, this is about the frequency response and as we have did last time we are now going to look at the noise analysis. So, whatever we have doing here it is going to be directly applicable in the design of our differential amplifiers or the 2 stage amplifiers op amps. So, this is we will not repeat all these analysis we will just remind you that this is the thing we have already covered and this is use the result that we have obtained over here.

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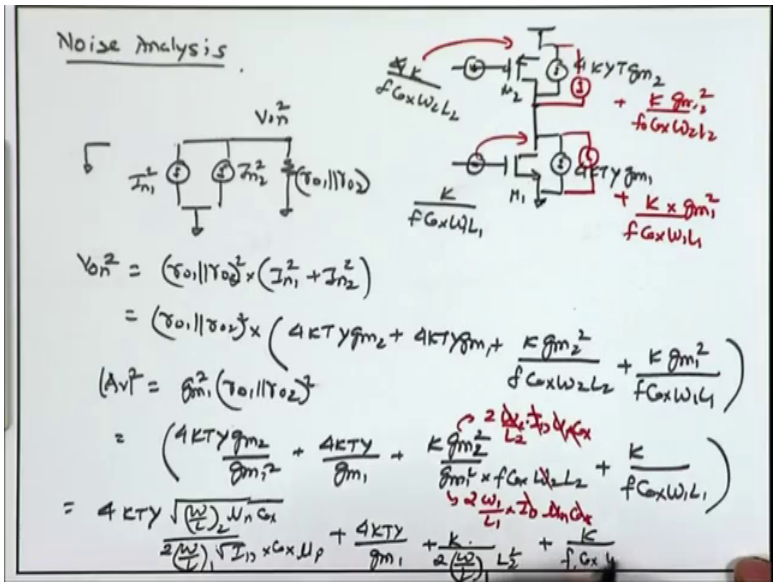

Now, let us look at the noise analysis. So, now, I can once again redraw my circuit I am not drawing the reference branch remember. So, in our previous analysis we have seen that the reference branch is constant DC voltage this is AC grounds.

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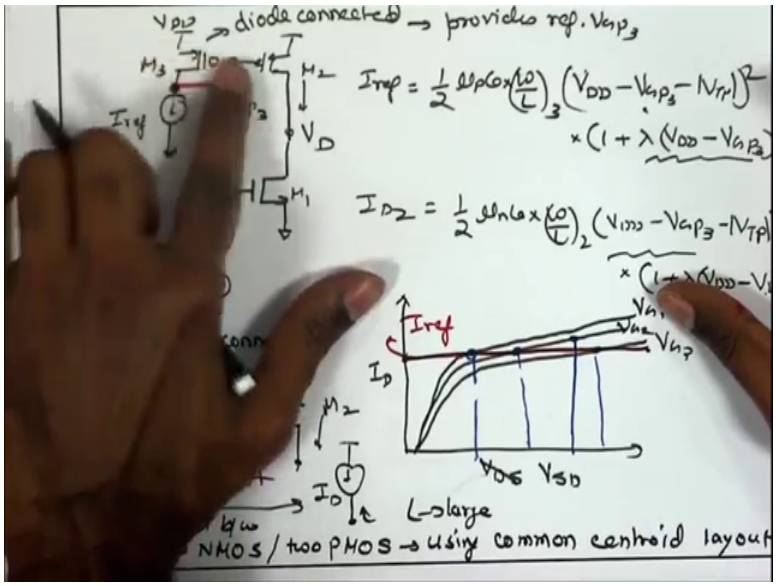

So, I am not drawing the reference branch this is a reference branch of the current mirror I am just ignoring this because this is the b c potential ideally.

So, let us just draw the 2 transistors the load transistor and the input device and now we are trying to see the effect of the noise sources in this 2 transistor, but we have seeing

yesterday the noise sources you have the channel current noise call this m 1 call this m 2 this is 4 k t gamma g m 1 now gamma can also be different definitely. So, we can call it gamma 1 g m 1 does not matter this is the constant quantity and likewise you have the channel current noise for m 2 again 4 k t gamma g m 2 and likewise you have the noise voltages 1 upon f noise sources k upon f c o x w l w 1 l 1 again k can be different k 1 k 2.

So, you can write this as k 1 k 2, but does not matter in the analysis we are just looking at the parameter 1 which we have control that is the w by l ratios and the g m and then once again here you have a k upon f c o x w 2 l 2 now we have seen that if the source is at ac ground I can reflect this small signal noise source at the gate into an equivalent drain current.

So, I can capture the effect of this noise voltage at the gate in form of a drain current by multiplying this voltage by g m square because remember this is the mean square values spectra density. So, I can just multiply this y g m square and reflected as the current. So, if I take it in the form of a current source and I add this in parallel with the noise current provide use by the channel I can add the term k upon f c o x w 2 l 2 time g m 2 square likewise I try to reflect this in a form of another parallel current source I can add the term k upon f c o x w 1 l 1 times g m 1 square.

So, in that case I have just 4 current sources with mean square values given by this expressions and now if I look at the small signal even without drawing the small signal I can find out what is the small signal voltage because if these are the total small signal currents flowing between drain and source in the AC analysis whatever we are going to get at this node we are going to have the small signal resistance of these 2 MOFSETs m 2 and m 1 coming in parallel just like we did in the previous case.

So, since we have reflected these noise voltages on the drain side inform of current. So, now, these 2 become AC ground. So, at the input side m 1 I can just put an AC ground over here and here I have captured the total noise current because of m 1, but I am replying the input source by g m square and likewise. So, I can call it I n 1 square and likewise I have also captured I n 2 square and we know from drain to source we are going to have the r o of m 1 between drain and ac ground likewise they are going to have r o of m 2 that is r o 2 between drain and once again AC ground which is V d d. So, once

again we have r o 1 parallel r o 2 and if you have to multiply and get the voltage remember this is I n 1 square I n 2 square we want to get the V o n square over here.

So, these 2 much apply this by r 1 parallel r o 2 square. So, I can just write down the total current equation total equations for the V o n square which is just going to be r o 1 parallel r o 2 square multiplied by I n 1 square plus I n 2 square now if I just expand this now once again another concept that we have seeing yesterday is a concept of input referred noise where we want to compare the overall noise produced by the circuit with the input signal appearing at the gate.

So, if we can reflect this total V o n square to the input port then you can compared this total noise produced by the circuit with the input signal that is the standard way of quantifying the noise in the circuit we can get the magnitude of input referred noise and to do that we need to multiply this V o n square by the gain of this circuit. So, what is the small single gain of the circuit from the gate to the drain that is just g m square times r o 1 parallel r o 2 square?

So, a V square if I look at the magnitude of the gain square that is just g m 1 square r o 1 parallel r o 2 square therefore, we need to find this entire equation by g m 1 square r o 1 parallel r o 2 square therefore, this r o 1 parallel r o 2 square anyway goes away I am just left with 1 upon g m 1 square. So, I have to basically divide this entire equation by g m 1 square let me do that 4 k t gamma g m 2 point g m 1 square plus 4 k t gamma upon g m 1 plus k g m 2 square upon g m 1 square f c o x w 2 l 2 plus k upon f c o x w 1 l 1. Now if I go further and try to look at the device parameters like how g m 1 and g m 2 are dependent upon the sizes of the transistors and try to figure out from their how the overall input referred noise of the circuit can be minimized what are the design parameters that is basically w by l and g m once again g m depends upon I d.

So, that as designers we have these options in hand we have the g m 1 g m 2 in hand we have the w and l in hand. So, mean to make appropriates prices for this parameter. So, thus this term can be minimized. So, to do that we need to convert these g m 1 g m 2 into the parameters on which it depends which are basically w l of the devices and the I d.

So, what is g m 2 equal 2? So, g m 2, so, if I write down g m 2 square w by l 2 times I d w by l mu p c o x are in called w 2 l 2 w 2 by l 2 I d u p c o x and what is g m 1 equal to 2 times w by l 1 times I d mu n c o x the c o x goes away we have I d going away if I

assume mu 1 and mu p are close we can we can get it of those as well which has because they are not really in our hand so well more interested in looking at the dependency in the parameters which are in our hand.

We see the w 2 also goes away in this term w 2 also goes away we are going to get l 2 square in the denominator l 2 over here l 2 over here l 2 square in the denominator and w by l 1 in the denominator this is the story of this term we just relatively the most complicated term other terms is simple to see this is just g m 1. So, basically we are going to get w by l 1 I d 1 and likewise g m 2 upon g m 1 square once again over here, so, once again w by l 1 over here. So, if I further simplify this.

So, I can write down 4 k t gamma now these 2 quantities I d gets canceled and therefore, you are left with c o x mu suppose I assume they are constant we are just with w by l 2 and here sorry does not get canceled you have suppose mu n c o x and I d goes to the denominator we have g m 1 square as 2 I d w by l. So, we have w by l 1 and you are having root under I d coming over here and you have the c o x and the mu p coming over here.

This is the first term second is 4 k t gamma upon g m I do not need to simply this because g m 1 I know dependencies on w by l and I d this term once again I have k times w upon l let me use a separate w by l 1 times l 2 square this is what I am getting in the denominator and likewise is the last term is k upon f c o x w 1 l 1.

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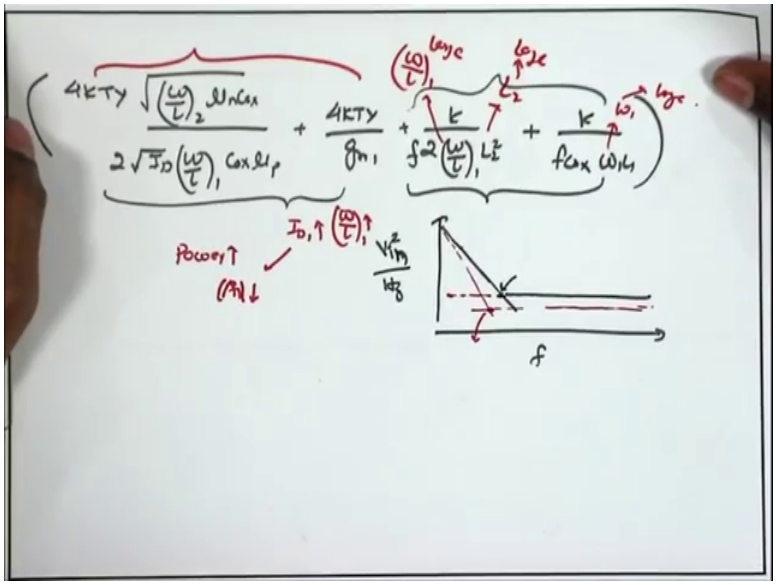

So, let me write it more clearly. So, that. So, let me just copy this and then from their try to conclude what is going to happen to the overall my expression. So, here once again 4 k t gamma w upon l 2 mu n c o x upon root under I d w upon l 1 2 c o x time mu p plus 4 k t gamma upon g m 1 plus k upon 2 w by l 1 l 2 square plus k upon f c o x w 1 l 1.

So, and of course, in the first in the first term also we have the f term the frequency dependent term. So, these 2 are the frequency dependent term 1 upon f and these 2 are the white noise term. So, yesterday we have talked about the concept of corner frequency where the white noise term and the 1 upon f term meet if I call say this is your V i n or V i n square which is the mean square of input referred noise per hertz and this is the frequency this is the corner frequency at which the 1 upon f term over here becomes equal to the white noise term this is independent of frequency this is just level constant level is going to be proportional to the first 2 term right. So, if I say this term is going to depend upon the first 2 term now if I say what is the dependency on this device parameters of w by l 1 and 2.

So, here if I look about look at the 1 upon f terms we see that it is advantages to go for larger w and l for the input device. So, input device if I making the w and l large I can possibly get a larger or smaller 1 upon f noise, but if I make l 1 large then if we here the l 1 is going to come in to denominator. So, making l 1 large may not be a very good option I can make rather w 1 large. So, to the minimize this term as well as this term I can rely on making w 1 large because if I make l n large the second term is going probably going to make problem we create problem l 1 will be coming in the numerator l 2 square is coming over here l 2 is also coming as 1 upon root l 2 in the first term. So, defiantly gives us the clear hind that if I make l 2 large the 1 upon f nice over here is going to be suppressed and therefore, we know we can reduce the increase the slope and therefore, reduce the 1 upon f noise of this term.

So, definitely we can try to make the l 2 over here relatively large this also tells us the w by l 1 you know we can try to keep it large. So, that this term is suppressed. So, I can have I can try to give w by l 1 large I can try to keep l 2 large likewise for getting larger w by l 1 definitely I can keep w 1 large the term over here tells us that larger g m 1 is going to suppress my white noise floor this is the white noise floor if I make the g m 1 larger which is either increasing the I d 1 or increasing the w by l 1 once again.

So, either I can make you know I d one large or I can make w by l 1 large to increase the g m 1 and hence reduce this floor further and same thing in the second term w by n large I d large basically coming from g m 1 I can afford to increase g m 1 that is increased a w by l 1 and keep the I d is slightly larger to reduce my noise floor white noise floor. So, basically why following these designs steps we can try to you know push this noise floor down I can also increase the slope of the 1 upon f noise terms.

So, that the corner frequencies also pushed away these are the favorable design steps or the directions to reduce the overall white noise as well as the 1 upon f noise for the system. So, far we have not considered; what is the significance of this 1 upon f noise we have just said that the signal that we are interested in processing may live very well in this domain which can be very strongly corrected by the 1 upon f noise.

We will see that how this choice of this corner frequencies going to affect our frontend amplifier design when we look at techniques to mitigate this is 1 upon f noise using chopper stabilization technique little later. So, we will come back to this concept of 1 upon f noise and try to see you are trying to minimize the thermal noise that is a white noise floor and also the you are trying to push the corner frequency further what are the pros and cons definitely you know here at least we have the starting point we have some information regarding the device parameters that are in our hand the circuit parameter that are in our hand that is the w by l of the input device the channel length of the output device and the bias current.

So, these are the parameters which are affecting my noise. So, of course, again we see that there is going to be trade off right if you are increasing the I d to reduce the noise what are the 2 things that are going to happen we have just seen increasing noise reduces the gain mod a V will reduce likewise increasing the i d power consumption we will increase bandwidth may also improve, but you know bandwidth is increases as a good point, but the disadvantages the power consumption re increases and the gain reduces if you are increasing the w by l. Once again we are having the parasitic capacitances increasing and therefore, you are going to get reduction in the bandwidth. And likewise if you are increasing the l 2 once again parasitic capacitances as well as you know the resulting bandwidths will be negatively impacted.

Likewise if you are increasing the l 2 we know that the signal swing at the output is again going to be impacted because if your l 2 is increased remember what is going to happen in the current mirror if your l 2 is increased the required V s g to produce the current I ref will be increased therefore, the V G P will be lowered if I am applying larger length of course, these 2 transistors are supposed to be matched. So, I have to use preferably same length of m there as well as m 2 and if I am increasing the a length of m 2 for a given I ref I will have lower V G P 3 and that implies lower maximum allowed value of V d. So, that is going to limit my swing.

So, once again we are trying to show we are trying to minimize 1 parameter that is noise it can have effect on many other parameters the gain bandwidth swing and so on. So, when we come towards differential amplifier there will be reusing this analysis for our design of the multi stage operational amplifier and the front end amplifier.