Analog circuits and Systems through SPICE Simulation
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Lecture - 07
Basic Analog Design Part III (Contd.)

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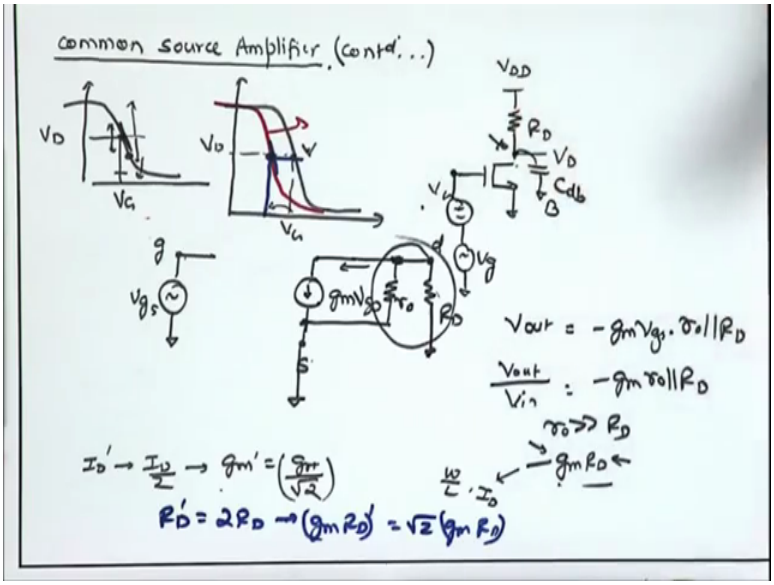

Welcome back, and the small signal analysis. Now what about the frequency response we already have a hint regarding the frequency response, we have already seen that this C db is going to play a role in the frequency response. How do we calculate? You know, in a comprehensive manner how do we do the more comprehensive response analysis? We just going to discuss some shortcut which is going to be a very handy in doing frequency response analysis for more complicated circuits.

So, all of you definitely might have come across the frequency response of simple circuits like common source amplifiers and for many of it may be redundant. But definitely as we said we have to cater to people even working in digital domain and for them it is important that we have the basics been covered, before going to the system level design.

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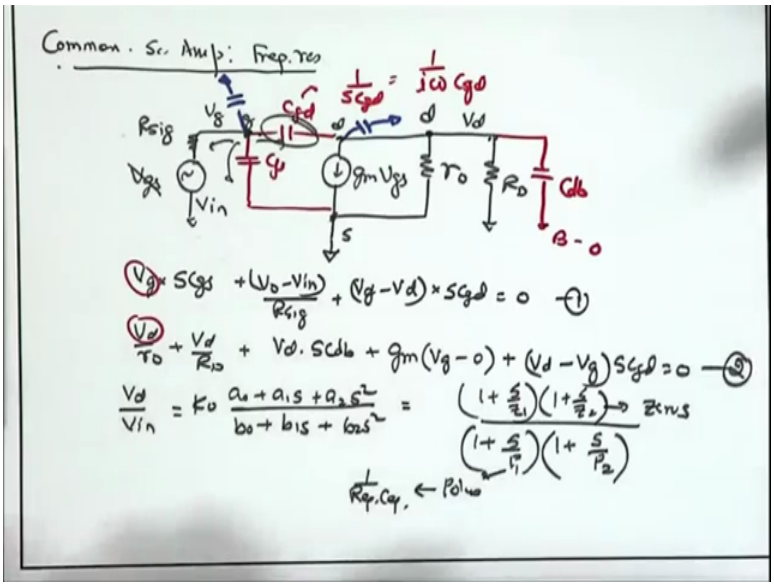

So, let me talk about common source amplifier frequency response; so for that once again all been to do is add the high frequency capacitance to the small signal model. So, I will redraw whatever I had earlier the same model, but with added small signal capacitance. So, what are the capacitances? Let me mark the terminals g, d, and s. And assuming that body is grounded, so you will have C gs, C gd, C db and C sb. Now B we are assuming that B is grounded S is also grounded. So, C sb is not considered only C db.

Now, here we have the overall circuit we can find out the, first you know cruder or you know, more complicated way of solving this question is to find out the differential equation solution. Write down the differential equation in time domain at this node and this node that becomes a couple differential equation. We can solve those to find the solution of the time domain signal. But in general it is much more convenient to do frequency domain analysis, where we replace each of this capacitance with their complex impedance which is going to be 1 upon S C gd, where S denotes 1 upon iota omega.

In general, in network theory if you are having any capacitance or inductance you know replace them by the corresponding complex impedance denoted 1 upon S C gd in case of capacitance. And then the rest of the analysis is just like K C l or K V l analysis right. So, here we can solve for these 2 node voltages unknown node voltages right. So, here if I add another complication suppose if I put another source resistance r signal in general a source will have some nonzero resistance, nonzero impedance. Suppose it is r signal. So,

in that case even the V g is not known to me. If I do not have r signal then V g is equal to V signal or V gs, but in this case V the V g is not equal to V in if I have a r signal.

So, V g becomes an unknown. Likewise V d is another unknown. So, my intention is to find out V d upon V in. So, I have 2 unknown voltages V d and V g. I can proceed with you know common analysis I can write down the K c, let this node and the second node I can solve those in terms of this complex impedance and I can get a overall transfer function. For example, you know at this node if I write down the expression for K C l V g times the impedance of this capacitor S C gs plus V g minus V in upon r signal plus V g minus V d into S C gd equal to 0. This is the overall K C l currents going out of this node V g into these 3 branches summed equal to 0.

Likewise, I can write down the equation at the drain node, so I can write down V d upon r o plus V d upon R D plus V d upon the impedance of the this capacitor which is 1 upon S C db. So, we get V d times S C db plus gm V g S which is once again V g minus 0. And then the last component which is V d minus V g upon 1 upon S C gd. So, S C gd this is the second equation. And here we have 2 unknowns V g and V d 2 equations we can solve them and find out the exact expression for V d as a function of V in.

So, we expect it is going to be you know some polynomial in S mabe a not plus a 1 S plus a 2 S square, second order because you have 2 capacitance. Likewise, B not plus B 1 S plus B 2 S square something of this sort this is a generic expression, I can you know further factor it into more friendly equation 1 plus S upon of course, there is going to be some constant term. So, there can be some constant term also.

So, we can factor it into the constituent linear terms 1 upon S plus p 1, 1 upon S plus p 2, 1 plus S upon z 1, 1 plus S upon z 2. So, this is the you know general way you know most common way of finding out overall, overall voltages gain this is a small signal gain, in terms of the frequency dependent parameters. Where p 1, z 1 they are call poles and zeros, poles and zeros, which are dependent upon the r phi time constant seen in the circuits right.

So, in general, this p 1 and C 1 they will depend upon 1 upon r equivalent C equivalent the r C time constant in the circuits. So, this in course a lot more combustion whenever we are trying to do this direct analysis it can be very combustion specially if we go for more and more complicated circuits, we are having more and more nodes we more

unknown voltages it will become more and more number of equations and we cannot do hand calculation based on that. A circuits simulator can do it, it is a running on a powerful computer, it can run many different solutions and find out the overall solution, exact solution and exact frequency response. But for hand calculation for doing quick analysis, we use some tricks we use some approximations we can, which can give us approximately good results fairly reasonably correct results So that we can get started with the design.

So, rather than going through this more complicated step we go for approximation. So, one of the key steps involved in that approximation and most of you might be aware of that is dealing with the miller effect. So, all we need to do is need to get rid of the capacitance connecting 2 different nodes and reduce them to capacitance connecting between those nodes and AC ground. So, here the C gs is between the gate and AC ground C db is between the drain and AC ground, but C gd is appearing between 2 nodes of the circuits and that is leading coupling between these 2 equation.

If C gd were absent then the equation of the first node is solvable independently and based on that V g I can solve once again the V g, gm V g as and get the V d independently. So, that decouples the 2 nodes I can proceed step by step and find out all the signal without doing this coupled solutions. So, that is the main motivation behind using miller theorem to decouple or disconnect the small signal parasitic capacitance connecting 2 circuits nodes and represent them by equivalent capacitance connected between the those particular nodes and AC ground.

So, what I would like to do I would like rid of this C gd and represent this as an equivalent capacitance between this node and AC ground. And likewise, between the other node and AC ground, this is what we would like to do. And miller effects come handy that is what we are going to use for doing the simplification. So, without going into the proof of miller effect which can be done in 2 lines, but I am just avoiding that.

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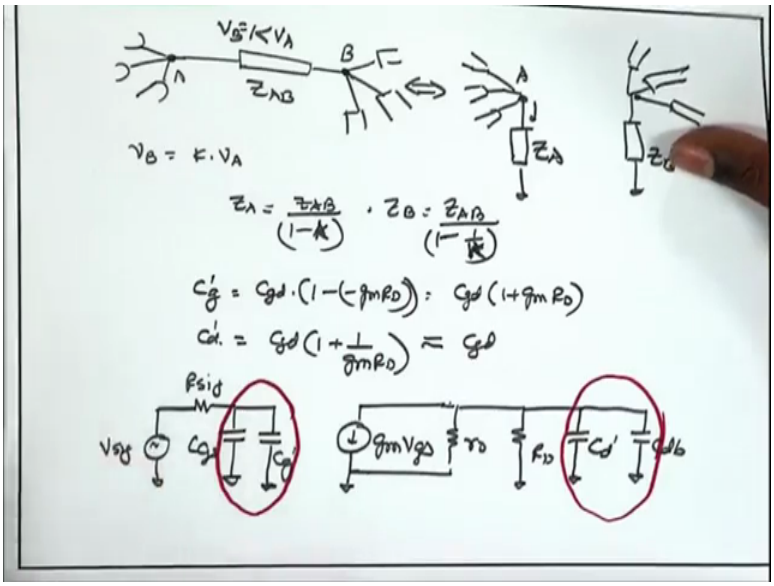

Miller effects says that you know, If you are having 2 nodes in the circuits suppose you are having some connections over here some blocks, I am just drawing 2 nodes node A and you know node B another 2 nodes these are also connected to some other branches and I am not drawing node B and we have Z AB connected over here.

If I am talking about the small signal, here you are having some relationship between the voltages at A and B. This small signal voltage gain at B as compared to A is suppose you know K. So, V B is equal to K times V A. Let me make it more clear. So, the small signal at B is K times V A. So, there is a voltage gain from the node A to node B and the those condition we can decompose this Z AB into an equivalent Z A connected between the node A and ground and likewise equivalent Z B connected between the node B and ground. And the where we proof the values we write the values just by equating the K C l. The K C l at node A should remain same as the K C l in this case. And then we shown that the Z A is going to be equal to Z AB upon 1 minus A likewise, Z B is going to be Z AB upon 1 minus 1 upon A.

So, if we apply this sorry K, I use the term K. So, it is really K that is a voltage gain from A to B. So, if I apply the same concept in this particular circuit that we have just arrived at, we can take an approximation we can say that the low frequency gain from gate to drain. Mind it, there is a low frequency gain, ignoring the effect of capacitance the low frequency gain between the gate and the drain. We know it is going to be equal to gm r o

parallel R D approximately equal to gm R D that is what we have done. We just read in the last slide so the low frequency gain is just gm times R D minus time. And therefore, the equivalent capacitance if I look at their impedance that is 1 upon you know, S C by this analysis the equivalent capacitance become multiplied by C if I have to find out C g that gets multiplied by C gd 1 minus A that is, minus times gm R D. And likewise this is the C g dash which I am putting here.

So, I am calling this at C g dash which is the blue capacitor, equivalent capacitor obtained by splitting this C gd into a capacitor between gate and AC ground, that is C g dash. And that C g dash is just going to be C g B times 1 plus gm R D. And likewise, if I call this the other blue capacitor C d dash which is obtained by decomposing C g dash into an equivalent capacitor between drain and AC ground then this becomes C d dash is equal to C gd times 1 minus 1 upon is basically 1 upon gm R D.

If I assume that gm R D is much, much greater than 1 then it is approximately equal to C gd only. So, basically what I can do is I can simplify this circuit. Now my new simplified signal small signal having C gs, it is having C g dash which I obtaining by breaking the C gd I A having gm V g S. Likewise I am having the C r and R D and on this I have C g dash which I have just arrived at by breaking the C gd once again, and I also have C db.

Now, these 2 capacitance C gs and C gd, C g dash can be combined together likewise, whether capacitance can be combined together into a single capacitance because they are appearing between this node and AC ground, and I can arrive at resulting simplified model for my frequency response.

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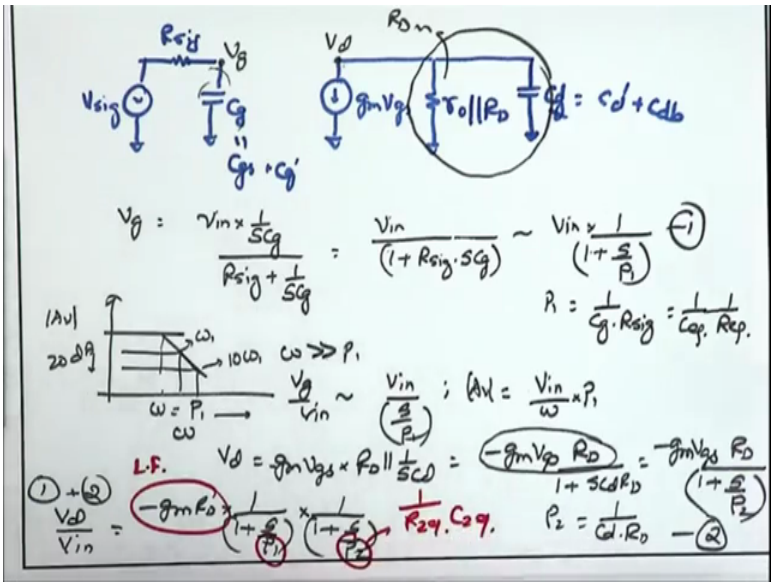

So, again call it C g which is equal to C g plus C g dash this is r o parallel R D and on the other side I have C d which is once again sorry, C d which is once again C d dash plus C db.

This is the much simplified model I have decoupled nodes. So, now, I have decoupled my V g and I have decoupled my you know V d. And then the equation for V g and V d become very simple I can just express V g as V in times the impedance of this capacitance that is 1 upon S C g upon r signal plus 1 upon S C g. That is just voltages division, this impedance of the capacitance impedance of the resistor r signal and this is the V g as a function of V in. We have simplified further V in upon 1 plus r signal times S C g. So, here we see that we are getting kind of, low frequency pole of the order V in times 1 upon 1 plus S upon p 1 right.

So, where p 1 can be written as 1 upon C g r signal which is 1 upon C equivalent 1 upon times 1 upon r equivalent. So, if I go towards lower frequency, the C g is almost open circuited because 1 upon omega C g is very large. In that case there is hardly any voltages division entire V signal appears at V g. Therefore, this equation is telling me S tending to 0, V g equal to V in. Whereas, if we go for higher and higher frequency the impedance of this parasitic capacitance C g reduces as a result the V g is going to fall. And that is also given over here the S increases as a result you even S becomes much

larger then p you are having a gain decreasing with S that is the magnitude of the gain is decreasing with omega.

As a result you get a fall in the overall gain after you hit omega equal to p. So, and what is the slope if I plot it in the log domain, if once I am having omega much greater than p 1 then the transfer function V g upon V in is approximated as V in divided by S upon p 1, because we can ignore this one with respect to S upon p 1. And then this means that once I am at omega much greater than p 1 my magnitude of this gain which is mod A V, V in upon omega times p 1 is going to reduce proportional to omega. So, if I go for 10 x increase in omega, my gain is go to go down by 10 x. In terms of d B again say, if I in this region if I increase omega by 10 x if I am going from omega 1 to 10 omega 1 my gain will drop by factor of 10 in d B it is 20.

So, I can say this will be a drop of 20 d B and therefore, I get a 20 d B per decade drop in the mod A V on the C axis we have omega y axis A v. So, if I just consider this transfer function, it says that after you hit omega equal to p 1 you are going to get a 20 degree per decade drop. Likewise if I go for the output pole, once again I can, once I have the expression for V in I can find out the expression for V d which is just gm V g S with the minus sign multiplied by the total z that is seen over here. So, earlier we had only gm V g S times r o parallel r d, but now we have gm V g S times r o parallel r D, parallel the impedance of this capacitor which is 1 upon S C d.

So, if I ignore r o and this is just approximately equal to R D then basically one again I have an expression which is R D parallel 1 upon S C d. Which is something like gm V g S R D upon 1 plus S r C d times R D. So, once again if I look at the first term over here, the numerator tells me the voltages gain is minus gm R D provided your S is very small. So, for very small omega, once again the term over here can be ignored with respect to 1 whereas, in that case my overall gain is just minus gm times R D.

But if I am going for larger and larger omega once again this starts dominating and once again you have the 1 upon S relationship coming. So, once again I can write this as minus gm V g as R D upon 1 plus S upon p 2, where p 2 is the pole given by 1 upon C d times R D. So, this is once again I can combine this V g S expression that we obtained earlier. So, V g S as the function of V in we have already obtained. So, if I combine this

equation 1 and equation 2 I can write down 1 plus 2 will give me V g or V d upon V in that is they are interested in.

So, first equation give me V g as a function of V in, second equation give me V d as a function of V g. Combining this I can just eliminate this V g by putting V g as a function of V in and therefore, I get minus gm R D into 1 upon 1 plus S upon p 1 times 1 upon 1 plus S upon p 2. So, what we say is that in this transfer function the gm R D term is the low frequency term which will come when you ignore the effect of this high frequency parasitic capacitance. But once you include the effect of this parasitic capacitance, then you have these 2 frequency domain frequency dependent terms coming into picture which say that at a higher frequency the gain is going to draw. And from this curve from this you know expression we can find out what is going to be the shape of this transfer characteristics mod A V with respect to omega.

So, in general if we carefully see what we have done in doing this simplification, we can observe a circuit and all we have to do is find out the low frequency gain. So, first term is the low frequency gain and then finds out what are the poles what are the high frequency poles or the r p time constants associated with different nodes. So, these are the poles and corresponding to that we are having the r p time constants associated with the 2 circuits nodes. So, at these 2 node voltages in the circuit, we have found out the r p time constants corresponding to the equivalent r and equivalent c. So, this is the step we are going to repeat for analysis frequency analysis for more complicated circuits.

Find out the low frequency gain and then find out the r C time constant at different circuits nodes. That is, find out the small signal equivalent resistance; call it 1 upon r 2 equivalents and find out the small signal equivalent capacitance C 2 equivalent. What is r 2 equivalent? That is the small signal resistance between that particular node and AC ground. So, at this drain terminal if you see; what is the small single resistance between drain and AC ground that is just r o parallel r D. Likewise, what is the C 2 equivalent? That is the small signal resistance seen between the drain and the AC ground that is just C d. That gives me the r equivalent, C equivalent corresponding to the pole arising at the drain terminal. Same thing applies at the gate.

At the gate terminal if I see the small signal equivalent capacitance between this gate terminal and AC ground is C g. And small signal resistance at this node between this

node and AC ground this is r signal, because V signal once we have taken out r signal out of it this is an becomes an ideal source, it does not have any resistance. So, these represent the internal resistance of the source. So, the equivalent small signal resistance between this point and the AC ground is just r signal, equivalent small signal capacitance between this node and AC ground is r C g. And therefore, 1 upon C g times r signal gives us the pole the p 1. And once we have this low frequency gain minus gm R D and we have this 2 poles we have the frequency dependent transfer function of the amplifier ready. From there we can do more detail analysis we can find out the transfer for the magnitude and phase response of these circuits.

So, we are, once we have this AC analysis done the last. So, we have done DC analysis, we have done the small signal analysis and finally, we have done the frequency response we will into little bit more detail of the frequency response, but just to complete the story we are also going to look into very quickly the noise analysis that we have just discussed, and how to you know link it with the circuit analysis. So, for doing the noise analysis once again we are going look into the small signal model and trying to see how to incorporate the noise signal at the MOSFET device. So, I directly draw the circuit we have R D and MOSFET which is going to have it is own noise.

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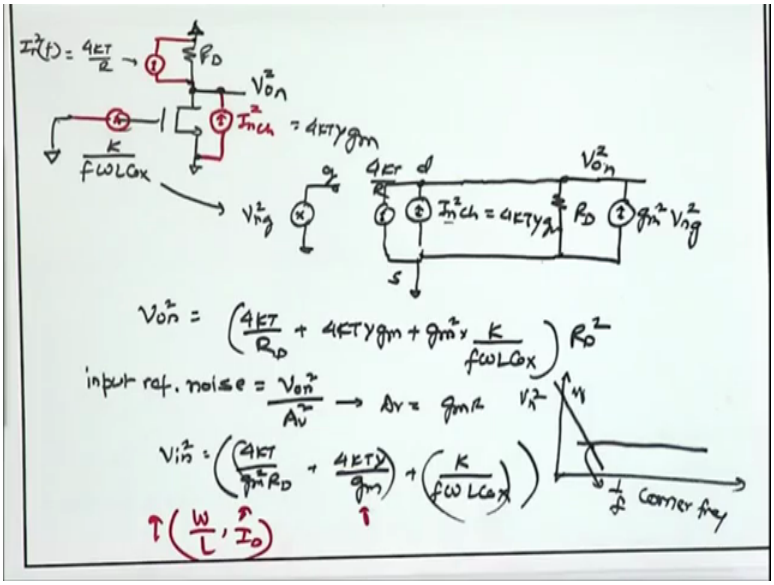

I can represent the noise source of the MOSFET as of the R D as the equivalent current source that is what we have seen, that is 4 K T upon R this is the i n square f. That is the

mean square noise spectral density of the R D. Likewise; I know I have a channel current noise for the MOSFET. I will call it i n square channel of the MOSFET which is equal to 4 K T gamma gm. And I also have the 1 upon f noise of the MOSFET coming in series with the gate which is you know K upon FWLCOX.

Now, if I want to find out only the effect of this noise sources I can set the input source as 0. I can set the input source to 0, I do not apply any external signal. I just want to find out because of these noise sources within the resister and within the MOSFET what is going to be my output noise voltages V o n square. That is the mean square output noise voltage. So, I can directly do the analysis here as well, without going to the small signal model, but It will be more convenient more clear if I go to the small signal model.

So, I am drawing the V n square g at the gate that is corresponding to the 1 upon f noise. I am drawing the i n square channel which is 4 K T gamma gm. We are also having the R D which is going to give you another noise source right. So, this is 4 K T power r, this is gate terminal source is grounded and we want to find out what is the V o n square. Remember these are noise square current square. So, we have basically first of all 2 current sources over here 4 K T by r, you have the channel current noise 4 K T gamma gm and we also have the trans conductance term which is going to convert this V n square g into another channel current, which is going to come because the gm term, gm square V n g square.

So, remember we have to deal with gm square because this is V n g square multiplied by gm square it will give you the effective noise current in the channel. So, based on this it is easy t o see means we have to just look at the square terms. We do not have to worry about the polarity of each of these current sources. So, this is the current which is coming between the drain and the AC ground. Remember this is V DD. So, from the point of view of the small signal it is AC ground.

So, we can ground it. So, this 4 K T upon is coming between the drain and the source this i n square channel 4 K T gamma gm again coming between drain and the AC ground; so i n square channel coming between drain and the AC ground. R D as usual between drain and AC ground, because it is drain and AC ground. And likewise the gm square term which is going to convert this noise gate voltage V n g square to V n g square multiplied

by gm square gives you gm square V n g square as a drain to source current source the current noise current.

So, there are 3 currents that are coming in parallel and all I need to do is some them up and multiply with R D square. Because these are current square and we need to add up the mean square values of these currents. So, basically what I have to do is output V o n square is equal to be equal to 4 K T upon r plus 4 K T gamma gm plus gm square K upon FWLCOX times R D square that is all. And now what we have seen is it is convenient to represent the noise as an input referred noise.

So, this is the output noise voltage V o n square that we are calculating. How to refer it to the input? What is the equivalent input noise at the gate which captures this entire output noise? So, input referred noise can be written as V o n square divided by a square or a V square where a V is the magnitude of the gain. What is the magnitude of the gain? At low frequency if I assume the low frequency behavior a V is gm R D therefore, a V square is gm R D square right.

So, then I divide the whole by gm r B d square and therefore, R D square gets canceled and V i n square will be 4 K T upon gm times R D plus gm square times R D times 4 K T gamma upon gm plus K upon FWLCOX. That is the input referred noise V in square. And we see some interesting results we see that the input referred noise is inversely proportional to R D. We would expect that if R D it is large, it is 4 K T r noise voltage will be large, but here we say that input referred noise is lower if we increase R D. Why once again the same phenomena: because larger R D also amplifies the input signal going to the output.

So, although it is producing some noise, but it is also amplifying the signal. So, that as compared to the, as compared to the input referred noise over here you know, the signal strength will be increased. So, if I talk about the signal strength at the output that will be amplified because of R D. Therefore, the noise or the signal to noise ratio that is getting improved if you are having larger R D. Likewise, we see that there is a strong dependence on gm. So, if you are increasing gm the first 2 stages definitely first 2 term definitely tell us, larger gm means large smaller input referred noise.

So, having as larger gm for the input device which can be obtained either by increasing I D or it can be obtained by increasing W by L. So, W by L or larger I D will help me in

reducing the first 2 terms. Likewise, the second term larger W as well as L will help me reducing the 1 upon f term, which is very significant not for low frequency operations. We will see that we have to reduce the 1 upon f noise that is going to be you know, taking care by choosing larger W and L.

But once again remember if you are choosing larger W and L, what is the issue? We know that larger W and L mean lot of parasitic capacitance. All the capacitance that we have discussed will scale up that will make your circuit smaller slower, parasitic poles will become lower and therefore, your frequency response the lower cut off the, the higher cut off frequency will be lower, bandwidth of the circuit will be limited. So, if you are trying to reduce the input referred noise it can you know, ultimately trade off with your area as well as the bandwidth or the speed of the circuit.

Likewise if you are relying on gm to increase your signal or reduce your noise once again larger gm means either larger W by L or larger I D. So, either it can you know increase you power consumption because of larger I D or once again if you are choosing larger W by L it can increase your capacitance and hence, the circuit can become slower. So, there is a lot of pros and cons the moment you try to fix one parameter try to adjust the noise, it trades off with your gain, it can trade off with your power consumption, it can you know trade off with your linearity, that we have not discussed in so much detail.

So, this is the step we are going to follow for rest of the circuits and you know, just to complete this discussion if I plot this you know transfer characteristics, if I try to see they are 2 terms. One is the 1 upon f dependent term and other 2 terms are constant term. So, the frequency at which this 1 upon f term becomes constant to become equal to this constant term is generally referred to as 1 upon f corner frequency of the circuit. So, this is your V n square and at this f, the contribution of this 1 upon term is becoming equal to the contribution of this constant term that is called the 1 upon f corner frequency. Beyond this point the 1 upon f noise is picking up it is contribution is increasing steeply. Above this point above this frequency the white noise term the frequency independent term that is more prominent.

So, in case your signal is in this region, that is below 1 upon f definitely, it will get corrupted by very large noise in this region. So, we need to take care of that. So, corner frequency happens to be another very important concern while doing noise analysis in

circuits. So, this is the analysis we are going to follow, this is the, this is the scheme overall starting from DC analysis DC biasing point go into small signal low frequency analysis, frequency response, transfer characteristics the you know, magnitude and phase response and finally, the noise analysis. So, they are the 4 basic tools we are going to repeatedly use in designing more complicated building blocks for our analog front end.

So, we will start our discussion on the front end amplifier, start with the building blocks the differential amplifier, with active load we will also look into current mirrors and when finally, develop the entire scheme with appropriate DC biasing, with optimization of noise we took optimization of you know, bandwidth and looking at the complete picture. And then we will use the front end amplifier with some other signal processing schemes to take care of some of the critical issues that is 1 upon f noise specially, in case you are dealing with very low frequency signals.

So, that is going to be covered tomorrow. And hopefully we will be completing the analysis of a front end amplifier based on the material that we have prepared today.

Thanks a lot.