Analog Circuits and Systems through SPICE Simulation
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Lecture – 58
Folded Cascode Noise (Contd.)

Welcome back. Let us resume our discussion on the noise analysis. And try to make certain other conclusion sort of it regarding the sizing of the devices and the conflict with other design optimization related to the bandwidth and king.

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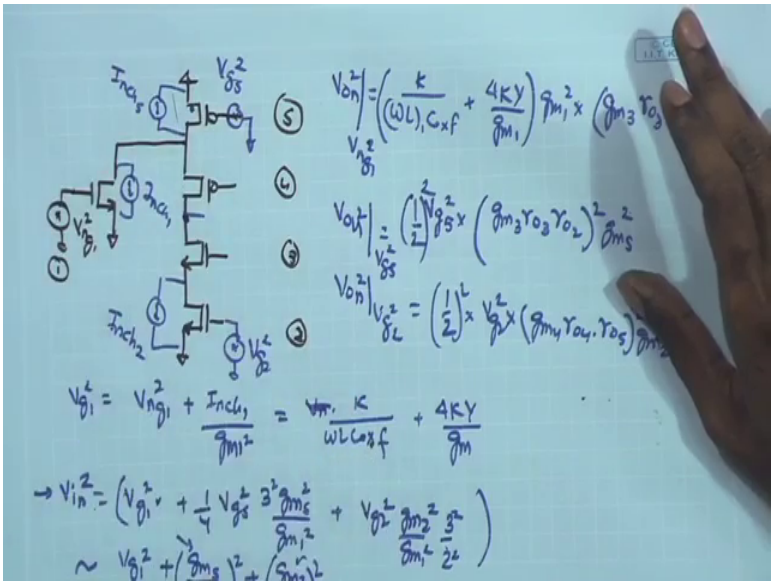

So, you look at the noise contribution of the 3 devices the m 1 m 2 m 2 and m 5. We have of course, not looked in to the noise contribution of the tail current source. And we have not looked in to the noise contribution of these 2. The analogy with the tail current source is that the noise contribution with the tail current source it is going to be divided equally into the 2 path. So, if we are looking at the tail current source.

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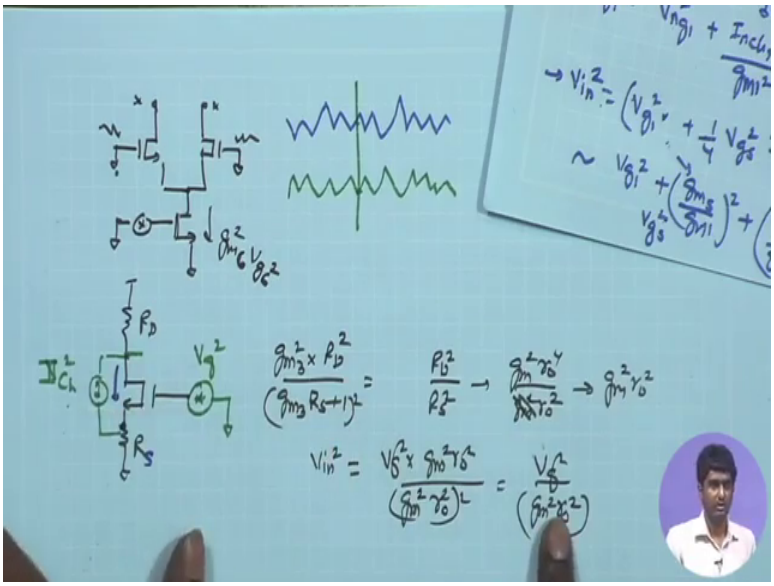

Whatever noise is produced by the tail current source that is going up the 2 paths. And is going to resulting equal and voltages at you know both the nodes. And in and the fully differential operation will be cancelled out therefore, we do not worry so much about the tail current noise contribution.

So, this is one point that we need to keep in mind. So, basically the 2 paths or the 2 noise signal that are going in up this channel and then getting folded and going out to the differential output. They are both these sources are correlated. So, if I assume that these are the 2 noise currents produced by this gm 1 square whatever I guess it was 5, let me see the number. So, I guess 6, this is was 6. So, gm 6 square V g 6 square. That is getting equivalently divided with 2 branches and getting folded down therefore, these 2 sources are correlated and when we take the differential output it was getting cancelled. So, it is affect is not appearing significantly in the differential output.

So, we ignore the contribution because of this gate noise as it is the channel current choice noise other important factor is we are using the differential operation only to figure out the overall noise. And the main issue there is that when we look at the noise signals at the 2 gates they are uncorrelated they are independent. So, whatever input referred noise is calculated we are coming from the different 2 different branches each of the devices are having different noise contributions they are uncorrelated. So, the 2 noise signals over here are uncorrelated. If we magnify these 2 noises they are going to result

in some random noise signals at the 2 gates. And as I result if I want to define the overall signal overall noise signal at any instance.

So, at any instance we can find out what is the instantaneous noise voltage at the positive input, what is the instantaneous noise voltage of the negative input and the difference of that gives you the differential input just like we do normally for differential amplifier operation any arbitrary signal can be broken down in the common mode and differential signal common mode signals does not get significantly amplified only the differential part gets amplified and appears at the output with a much magnified response. Therefore, we are considering only the differential response and doing that we look at this as an AC ground and then figure out the total output referred noise and the output referred noise. So, this is another point we should be taking note of with respect to the overall analysis.

Now, let us try to as another issue which is regions with a noise contribution of these cascode device the cascode PMOS and cascode NMOS. So, I can look at that both the noise contributions the gate noise the flicker noise which is model as a series voltage in the gate and the second one channel current noise. So, I can just look at the NMOS condition and the result to be similar to the PMOS. So, for the NMOS I have large impedance R D in the drain right. So, if I am considering the m 3 it is seen a large impedance into the drain which is gm ro times ro. So, I can call it R D which is a large value. Likewise m 3 is also having a large resistance in the source which is ro. So, I can call it rs. So, of course, R D is much greater than Rs in this condition. And then on the top of that we had the noise contribution because of this channel current if we can assume it and then you have an overall signal the noise signal at the gate I can call it V g square I can call it V channel square V ch square. And because of this I would like to find out what is the overall output voltage over here.

Now, if I here I cannot directly translate this V ch square divided 2 equivalent gate voltage, because for this case the source is not ground not an AC ground, as a result I cannot directly divide this V ch sorry ich. I cannot divide directly this I ch square divided by gm square and get a equivalent gate noise voltage, that can be done only the source grounded. And therefore, let us first consider the V g square.

Now, if I consider the effect of V g square and find out what is the output noise because of V g square. This is our common source amplifier this source degeneration and

therefore, definitely the overall gain from this input to the output can be written as gm of this device which is I guess gm 3. Gm 3 square times the R D upon gm 3 Rs plus 1. This is approximate expression this not exactly true when you are having very large impedance connected you get a slightly different expression over here, but approximately I am writing the same expression.

. So, you are having sorry gm 3 R D square upon gm 3 Rs square, this is the overall gain. And once again if I assume that gm 3 Rs is much greater than 1 which is 2 here. So, I am getting R D square upon Rs square. And therefore, we can see in this case you are reduced to gm square ro 4 upon gm square ro sorry upon ro square. And therefore, you are having an overall expression gm square ro square. And now if I look at the input referred noise this needs to be divided by the overall gain which is gm ro whole square. So, V in square because of this is going to be V g square times gm square ro square divided by gm square ro square whole square. And therefore, this is going to V g square upon gm square ro square.

Which is significantly smaller contribution much smaller contribution as compared to other devices. Even at the output if I look at it if you consider the for example, input device all the devices which are connected to the sources their V g square is directly getting multiplied by the gain of the amplifier, which is gm square ro square. So, there you are having a multiplication factor which is gm ro whole square. Whereas, the conclusion of this source is lower by a factor of gm ro if I am considering V g it is getting only multiplied by gm ro whereas, if I am considering the gate noise voltages of the devices which are connected to the vd and ground in our case the m 2 and m 5. And m 1 their noises are getting multiplied by gm ro whole square. And as a result the noise contribution of these 2 can be ignored as compared to the noise contribution of m 1 m 2 and m 5. So, this is one effect likewise I can look at the I channel what is the result of I channels contribution. So, intuitively we can see what is going to happen, if I assume I channel to be increasing or decreasing in a certain direction right.

So, if I assume that I channel is a random current rate is go up or go down in a certain direction ultimately it is going to subtract to the channel of current. So, assume that you are having a fixed current I dc and on the top of that you have this randomly fluctuating actioner it can go up and down. Suppose at a certain time instant it goes up; that means, the current is positive this is I channel is positive flowing from drain to source over here.

And therefore, it will increase the source potential right. So, if the there is an increased channel current will try to increase the source potential over here because of this r coming in Rs coming in therefore, we did not mention rs. So, here remember this was Rs and that is what I used. So, if I increase the I channel at a particular instance that will increase the r the vs over here. V g is a constant potential by analyzing the effect of this ch channel V g is AC ground constant potential. As a result when you when your source potential over here goes up it is reducing the V gs and therefore, will suppress the increase in the current.

So, it will whatever I assumption I took in the beginning that, because of the noise there is an increasing current. And that is causing those increase in source potential that will lead to reduction in V gs of this MOSFET and that will suppress that current. So, we are having kind of a negative path is cancelling out any increase. So, that this kind of negative feedback kind of is going to suppress the effect of I channel in this case same thing is true for V g also that can also be explained with the help of this negative feedback. So, ultimately when we are talking about a sporty generated common source amplifier that negative feedback action is present. So, V g going up try to increase the channel current and that will try to increase the voltage at the source of this device. And that will reduce the again V gs and hence try to suppress the increase in the channel current.

So, this negative feedback mechanism present in the cascode device it helping us in reducing the effect of noise contribution of these devices on the output and hence the input referred noise therefore, we are ignoring it. And analytically also we can try to in this circuit we can try to solve the kcl and figure out what is the expression for I channel. You can do that very quickly if I look at it if I look at this model. So, assume the V g is 0.

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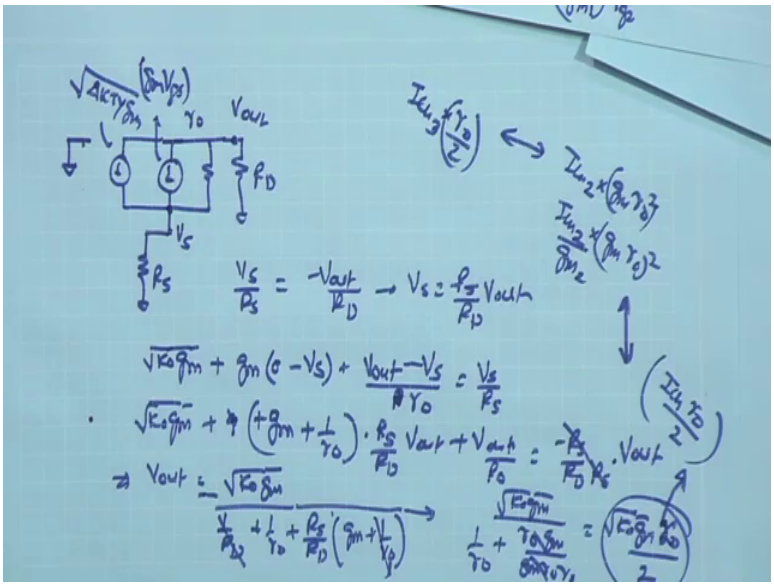

So, MOSFET gate is 0 gate potential is AC ground and therefore, I do not I can look at the gm V gs term you have the R D which is between the drain and AC ground and you have the ro and also you have the Rs over here. We know that R D much greater than ro much greater than rs. And here you are having the gm V gs definitely and apart from that you also have the noise current which is for kt gamma gm it is not dependent upon the V gs (Refer Time: 11:27) just the constant term which is having some rms amplitude. So, you can call it some constant times gm. So, this is for kt gamma gm this one and this is your gm V gs. V g is anyway 0 so it is just gm times vs.

And then based on this we can figure out what is going to be the output potential over here, V out and that is going to give me the exact expression for the V out dependency on the current produced by the channel noise.

Now, if I assume that this is vs the unknown voltage and this is vd, at preconstance we can assume that there is some polarity. Of course, over all the noise current is random it is not having any polarity, but for a particular instance we can say that it is spiking up and as a result the current is in certain direction. And therefore, let us see that if the current is in this direction given by the magnitude for kt gamma gm peak amplitude, times some constant of core depending upon the frequency of integration. And these are this is the value which is you know gm V gs it is just gm times vs. And remember that this is the current over here supposed to be the root of this quantity. So, this is the current

density the mean square value I nch square and when we add it we have to take the root under gm value.

So, root under gm times the bandwidth as we say. So, let us let us do it whether let us call it root under gm. So, some constant and root under gm this is gm vgf. And then we can figure out what is going to be the effect of this noise current I channel on the output. And let us look at vs first of all. So, vs upon Rs is the current flowing in that must be equal to the current going into the circuit I can call it minus V out upon rd. So, I can express vs as Rs upon R D minus times V out. And then I can write down the overall expression of current over here which is root under k naught times gm which is the current does dependent on gm plus gm times V gs which is 0 minus vs plus you have V out minus vs upon Rs sorry, ro this should be equal to vs upon rs. This is expression we have finally, and I can fall for vs you have k naught times gm root under plus vs I can basically replace by V out and then so for it.

So, you have minus gm minus 1 upon ro times vs which is if you get Rs upon R D times V out over here plus V out upon ro and this is equal to minus again Rs upon R D upon Rs times V out. And then you can cancel out. We are now I can I can take this on the other side and find out the expression for V out. So, V out is going to be given by root under k naught gm divided by with the minus sign divided by 1 upon R D, 1 upon ro plus Rs upon R D times gm plus 1 upon ro. This is the overall expression I am getting for the V out. Magnitude point of view I will look at the mod of this quantity only.

And now if I look at these quantities in the denominator I can take some simplification based on whatever assumptions I had. So, I know that R D much greater than Rs and therefore, this quantity is much smaller than 1. And then you have the gm and 1 upon ro out of these again I can ignore the 1 upon ro terms because in general I am assuming that it is much smaller than gm. And among these 2 numbers 1 upon R D and 1 upon ro we know that R D is much greater than ro. So, I can ignore the 1 upon R D term. And now if I look at Rs and gm to the denominator side I have 1 upon ro and Rs gm. So, Rs is just ro. So, you have ro gm upon you have R D which is once again large gm ro times ro. So, I am basically left with 2 upon ro in the denominator and root under k naught gm over here. So, root under k naught gm and 2 ro is are ro by 2 is what we are getting the root under gm ro by 2 and k naught is some constant number. So, the constant terms are going to determine my overall unit. So, we can see that the magnitude point of view it is this is

the noise term for kt gamma gm times ro. So, this voltage once again is proportional to the root under the vn square because or I ch square.

So, I can call it I ch times ro conclude. So, this is basically nothing else, but expression for I ch. So, I ch times ro by 2. So, this is the overall voltage I am getting. So, I can call this I ch this is a channel noise current magnitude times ro by 2. And then if I want to refer it back to the input once again I will divide this quantity by the gm ro whole square. So, here itself I at the output point I can compare what is happening.

So, if I talk about the I channel of the other MOSFET if I talk about the I channel of say if I talk about the I channel of the m 2, or I talk about I channel of and then getting multiplied by gm square or gm ro whole square. So, if I look at the magnitude I ch times gm times gm ro square. So, if I compare this type of contrast this width the channel current effect of m 2. So, I nch 2 is getting divided by gm 2 to give you the gate noise voltage of m 2. And then getting multiplied by gm ro square. So, basically I have I ch 2 getting gm times ro square. Whereas, the I ch of the cascode device is just having factor I ch call it 3 times ro by 2. So, here you have a ro by 2 and you are having gm ro times ro right.

So, magnitude point of view once again the same conclusion that the overall noise voltage at the output, because of the cascode device is gm out times smaller as compared to the devices which are connected to the V DD ground that is the m 2 and m 5. Therefore, as compared to the noise contribution of the I can see them I can call them common source devices because their sources are grounded and then noises are contributed in the form of a common source amplification. As compared to those devices the cascode devices noise are lower by 1 upon gm ro factor therefore, I can ignore them this is the analysis just to conclude this result.

Now once we have concluded that and we look back at this expression over here we can again correlated back to the analysis that we did with it to frequency response and try to see how these 2 requirements are conflicting requirement of lower noise and requirement of higher bandwidth and good gain if at all there is any conflict. So, before we go further any discussion on whatever we did with respect to the noise contribution of cascode devices? All right.

So, let us go back and look at the expression that we had for the overall output referred and input referred noise because of the main contributing devices. And also look at the corresponding frequency response analysis that we did with respect to these capacitances.

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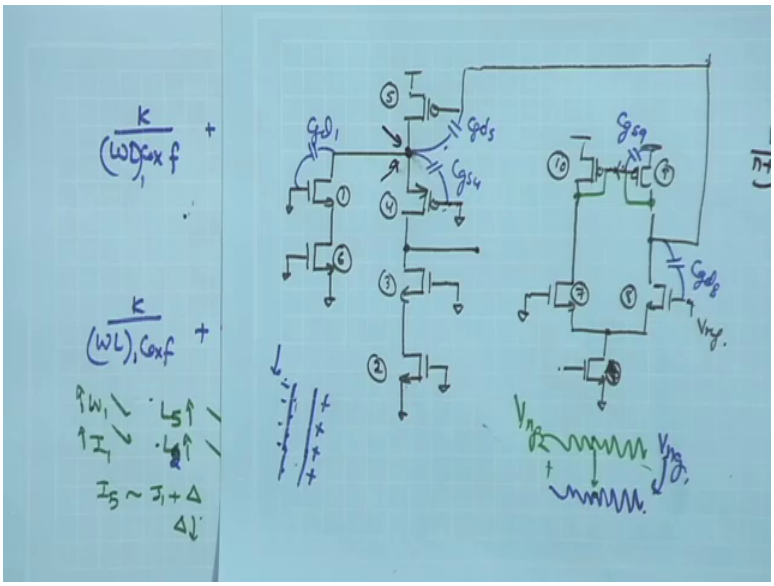

So, here once again we can see what is going to happen if I choose the device dimensions to minimize the noise. And one of the important factor that we mentioned in the beginning I need good gm for minimizing the noise and for that I need (Refer Time: 20:14) W by L or W 1 of m 1. Therefore, a large W 1 of m 1 definitely going to make the cgd 1 dominant it is going to increase the cgd 1 which is going to contribute this pole. Larger L 5 and L 6 as I said it is not going to increase cgd 5 significantly because cgd 5 depends upon the overlap capacitance. So, cgd is dependent upon the L overlap it is the constant parameter for a given technology time W. Therefore, it does not suffer or does not increase when we are trying to apply larger L 5 or larger L 2 I should call this 2 it is not really as 5 6 it is should be 2.

Because L 5 or L 2 because this is the bottom device we have talking about. So, L 5 or L 2 full increasing the L 5 or L 2 does not really increase their cgd decrease significantly as the result it does not have a significant fight with the compensation. And other another factor is that the cascode devices are not contributing significantly to the noise. And therefore, I can bring their W by L ratio down significantly without sacrificing my noise

figure. And as a result the cgs for effect can be minimized. So, that is not going to play a very important role. So, the main contributor is going to be cgd 1 at this node. And therefore, even for the differential response as well as common mode response the non dominant pole at this point is going to suffer because of the cgd 1. And other issue that we also figured out is the conflict between the swing and the gain and the noise.

So, if you are going for lower noise design then once again you are targeting larger L 4 m 5 and smaller W by L for m 4. And that means, that you are going to have poorer or much significantly larger overdrive voltages for m 5 and m 4. And that is going to reduce my available swing over here, same thing on the lower side I would like to have lower W by L 4 m 3 larger L 4 m 2 and both that is going to reduce the headroom on the negative side and going to impact my swing. So, lower noise is going to impact my swing in a negative fashion. So, that is another trade off we should be aware of. And for the point of view gain as I said the gain ultimately depends upon the gm and the ro products.

Now, ro if we see is coming as gm ro times ro of this particular device gm again depends upon the bias currents noise also depends upon the bias currents. So, increasing the current in the first device is going to help us in increasing the gain it is also you know going to help us in increasing the or reducing the overall input referred noise. Here if you increase the current over here of course, it also reduces the ro of m 5, but that can be compensated if you are having a larger channel length for m 5 significant additional length for m 5.

So, at least for the noise definitely I would like to bet on the I 1 I need sufficient I 1. So, that the noise input referred noise is reduced and at the same time what we discussed was if you are reducing the I in the in this particular stack, that is also in a way going to help us in reducing the input referred noise because we saw that the ratio I 2 upon I 1 or gm 2 upon gm 1 that was also helping us in reducing the noise. So, these are the factors we should be aware of while doing the design for low noise and make sure that while doing noise optimization going for lower noise their also meeting the required specifications for the gain and the bandwidth.

So, as next step you know since we have done this analysis for noise frequency response swing etcetera will take couple of examples, their the design steps will be shown algorithmically that given design spec specs at the higher level how do you come back to

the transistor level design, and how do you approach this sizing of these different transistors step by step, in a logical fashion, considering all these constraints considering all these you know design requirements in terms of specifications.

So, while addressing these specifications one by one starting from say bandwidth starting from the gain bandwidth product which is ultimately dictated by the higher application. Like we have discussed that the chopping frequency is going to mandate higher frequency that gives for the bandwidth requirement. And the position requirement gives us the gain requirement. So, gain valid product is coming from the higher point and from there we can see how the gain valid product is defined in this particular amplifier. So, we have seen for the 2 stage op amp how does the gain valid product get define. It is defined by the gm upon the cc. So, the gm upon cc the starting point if you need to setup particular gain bandwidth product for the amplifier where gain is said to be 10 the power of 4 for meeting a required accuracy bandwidth permitting required chopping frequency. We have this gain bandwidth product being determined by gm upon cc that becomes a starting point. And then you have the overall bandwidth or the cut off frequency means determined by the ro of the first stage basically the p 1 which is determined by the gm times gm ro time cc and the ro of the first stage.

So, step by step you know considering these constraints we can figure out the dependency of the sizing and resolve the designs resolve the sizing required for the different transistor in the first stage. In the second stage likewise in the cascode also we can start from given a specification and tracing back try to find out the dependency of each of these specification on the transistor sizes and try to set a compromise. So, generally analog then happens to be iterative. So, you once you set the transistors to meet a certain specs some other specs may get violated and again you can have you may have to go back and look at the design in iterative fashion fix them other specs again some third specs can get violated. So, it may take several iterations to arrive at the design which is meeting the given set of specifications within a reasonable margin.

So, we will take 2 such examples both with the 2 stage op amp that we have spent enough time on and also the folded cascode and that will facilitate that will help you in arriving at proper sizing. So, far in simulation assignments I have not ask you for going for appropriate sizing of the transistors. They have just given some starting sizing starting point for the sizes and have ask you to compensate those and get the loop stable.

So, another important factor is the sizing of the transistor that we will arrive at looking at this concept involving all these concepts and looking at the dependency or the sizing on all these analysis. Any question before we close?

Student: sir (Refer Time: 27:26) find out the noise we were taking only the differential period. So, one side of the differential (Refer Time: 27:31) input referred noise we have got with the differential input. So, this same input this same input referred noise with the negative sign of the (Refer Time: 27:46) this should be amplified

No input referred noise means you are having you know rms value of the noise, you are determining what is the rms value of the noise and what is the frequency content of the noise. So, that same magnitude of noise can appear at any of the terminals. So, what I discussed was ultimately if both the input devices are having certain noise and we are considering only the differential component of that noise. So, noise are uncorrelated at the both the gates and they are random and they are having a wide frequency range starting from low frequency to high frequency.

Student: (Refer Time: 28:16) must be exactly negative of the this (Refer Time: 28:20) you will get amplified?

Why?

Student: Because (Refer Time: 28:24).

Any arbitrary signal at the gate of the differential amplifier V 1 V 2 you can break it down into differential component common mode, component differential component gets amplified common mode component gets separates. So, not only in the last topic even previous topics, you can just go through very quickly. And if we have any issues we can discuss.