Analog Circuits and Systems through SPICE Simulation
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Lecture – 57
Folded Cascode Noise

Welcome back. Let us resume our discussion on the stability analysis for the common mode feedback loop for our cascode amplifier.

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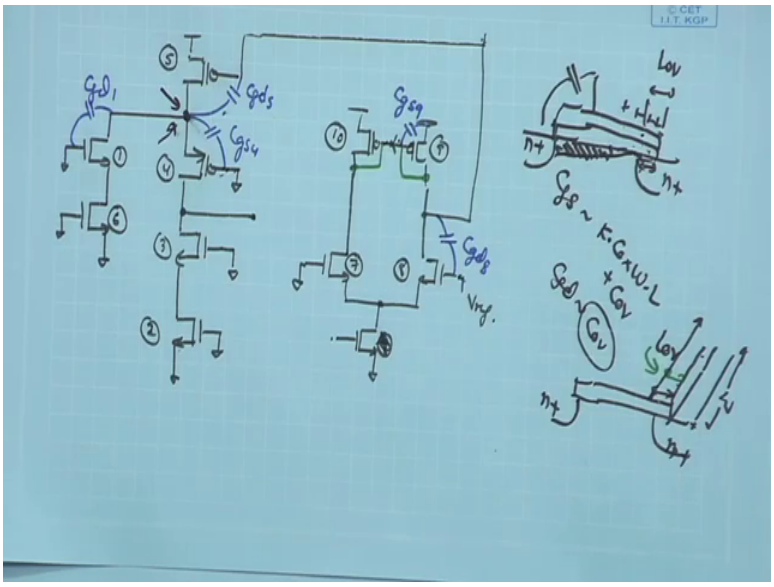

And we are looking into the parasitic capacitances that are going to determine the overall capacitance at the non dominant pole. And we are looking at the condition where we are trying to make the dominant pole at the output gm ro times the non dominant pole So that good phase margin close to 45 degree can be achieved. And towards that end we will the target is that the overall capacitance over here the compensation capacitance of the load capacitance that we are adding or which is coming by itself because of the next loading stage that is at least around gm ro times the net parasitic capacitance over here.

And therefore, if the capacitance over here becomes too large because of other design constraints the compensation capacitors to be added can become large. And therefore, we are just trying to see and identify the different components of the capacitances that are going to come in. And from there we will go to some other analysis like the noise analysis, which will enforce certain sizing constraints for some of these devices. And

there also you would like to make sure that those sizing constrain are not enforcing very large capacitance at this particular node. So, this is something we would like to make sure for the common mode overall common mode response.

Now these are the capacitances we have drawn and as I mentioned I am ignoring the source to substrate and drain to substrate capacitances assuming them to be relatively small and they also do not contribute to the miller multiplication, because they are also is going to appear between source and ac ground because assuming that all the body terminal for the PMOS and NMOS are at either V DD or ground respectively. So, they are the csb and cdb component of all the MOSFETs come between the drain and the ground therefore, they are not miller multiplied. And their values are also significantly smaller than the c g D component which is in turn smaller than the C gs component therefore, we are ignoring the cdb and csb.

So, in summary these are the capacitance that we have remember that we decided to use a diode connected load for the error amplifier. So, both of them are having low impedance node over here impedance given by 1 upon gm approximately for these 2 transistors. And therefore, if I look at the overall capacitance. So, we had the C gd of m 1 the gate is ac ground therefore, it appears directly between the drone drain and ac ground not having miller multiplication, C gs of 4 which is going to be significantly larger than C gd values over here.

Now if I look at the C gd 5 that is also appearing between this point and the gate of the m 5. And again at this point if I look at reverse miller multiplication factor that is not going to be significant for C gd 5 because it is going to appear as 1 minus 1 upon a gain from this to this point is you know large, but the miller multiplication from here to here is going to be going to include the reverse gain 1 upon a therefore, this is also not going to contribute heavily. Therefore, the dominant capacitances that we have over here is going to be C gs at this particular node the dominant capacitance that we are going to have is C gs 4 C gd 5 and C gd 1 and among these capacitance at the p 2 pole we can see that the cg s 4 can be the larger one, C gd 5 and C gd 1 can be relatively smaller. Both of them are coming as it is close to C gd 1 only therefore, they are contributing smaller factors.

So, here I would like to make sure that whatever sizing constraint we are going to have they do not increase cg s 4 too much. And for that we also should remember that what is

the dependency on C gs 4 device dimension. So, if I looking at this node the C gs 4 depends upon W as well as L. Remember the origin of C gs 4 depends upon the oxide capacitance. And therefore, the area of the total gate that you have for the MOSFETs therefore, larger W and L for this device can induced larger C gs 4. So, we would like to keep the W and L of this device relatively small we do not like to size this too large otherwise it will introduce larger C gs 4 as long as the other capacitance are concern C gd 1 and C gd 5 they are relatively small. And we will see that the sizing constraint for the m 5 and m 1 should be such that they do not enforce very large C gd.

Now, what does C gd depend upon C gd 1 and C gd 5. So, once again if I remember the dependency from the device structure the C gd is going to have 2 major components. One comes because of the overlap of the gate dielectric and the drain region. So, you are having overlapped capacitance, if I am let me forgive me for the bad drawing. So, on you have an overlap region between the gate dielectric and the drain, which leads to an effective overlap length L overlap and that also leads to a effective capacitance between the gate and the drain region likewise gate and the source region. Because what is happening because when you are putting some more charges on the gate the region in just below the overlap is attracting more electrons. And therefore, some charge on the gate is balanced by the electrons getting attracted in the n plus region where the gate is overlapping with the n plus.

So, that leads to a fixed C gd component coming from c overlap. So, that c overlap component is present on both side. And the for saturation region the C gd is dominated by c overlap and we know that the channel in the saturation region is q towards the source side and the drain side you do not have much of the channel charge coming therefore, if you change the Vgs the channel charge is mostly controlled by Vgs and a much lesser extent by the Vgd. Therefore, the C gd does not play a significant role in changing the channel charge in saturation. Therefore, the gate capacitance will be determined by the co x that is mostly ascribe to the source to gate capacitance.

So, in the saturation region the C gs is accounted by mostly the gate oxide capacitance co x times W times L. So, that becomes proportional to the gate capacitance. On the source side also you have overlap. So, the c overlap part is also there on the source side, but in general the oxide capacitance is significantly larger therefore, in saturation region C gs is some constant factor smaller than one times co x times W times L plus c overlap.

Whereas, the C gd is approximately equal to c overlap only. Because C gd side you do not have much control of the gate to drain potential on the channel charge. So, the effective capacitance for the gate to drain junction arises because of the c overlap in the saturation region.

And c overlap if I look at the geometry of the device the c overlap would depend upon the overall area of the overlap between the gate and the gate and the drain region. So, if this is the L overlap that I am drawing, L overlap showing the slight overlap between the gate dielectric and the n plus region the overall c overlap will depend upon this L overlap times the total W of the device right, L overlap will have the technology parameter that is feature of the technology does not change from device to device. What changes is the w. So, this is this direction of the W of the device I am drawing the 3 D projection. So, you have n plus n plus this is the channel and you have this is the gate and this way you have the W, this is the total W of the device, this region I am calling this L, L overlap. So, this is this is L overlap. And therefore, the C gd will be determined by the W of the device if you are increasing the W of the device C gd of these MOSFETs the m 1 and m 5 pair they will also go up increasing and as a result it will push this pole towards lower frequency.

So, I would not like to have large W for this device neither, I would like to have large W for this device. Likewise I would also like to avoid large L and W L products for this device. So, this is something we should keep in mind, while looking at the sizing of the cascode. If I look at the consideration that we are already aware of for example, if you want to have a good gain for a good gain from the cascode amplifier I would like to have the gm ro product to be large for that, I would like the W by L of the input pair over here to be large. So, that is again conflicting. So, you are having if you want to have larger gain for a given current you would like to make the W by L of this MOSFET large. But if you relay on the increasing W then the C gd is not strongly affected by the you know W that is coming sorry the C gd is getting strongly affected by the W and therefore, that is once again getting or increasing the overall node capacitances over here.

So, when you are trying to increase the gain by increasing the gm of the input device and hence the W of the input device, we can see that the overall C gd 1 is going to dominate. And this node can be ascribed or the total capacitance over it can be a to ascribe to C gd 1. Whereas, the other capacitances do not contribute or the W of the m 5 does not

contribute to the gain So much. So, here the W can be reduced significantly. And we will see that the noise constraint also forces us to have a larger L for this device, and poorer gm for this device. And therefore, the C gd over here may not be an important constraint. Likewise if you are looking for the other cascode device over here, the cg s it depends upon L as well as W. If you want good ro and overall good gain over which is dependent upon gm ro square, that depends upon 2 factors once again bias current and L. And if you want to have good gain one option is to reduce the bias current, and there you do not relay so much on L and in that case we can you know relay on increasing the or having a nominal W by L of this device by reducing the bias current So that the gs C gs 4 over here also may not be very you know dominant.

So however, the C gs 4 is having a value which is larger than C gd 1. So, these are the 2 which are going to dominate the C gd 5 may not dominate so much because here we will see that the major factor that comes in C gd 5 or m 5 it is basically the channel length you need to have a larger channel length you can sacrifice the W of this device. So, this C gd 1 does not matter So much. C gd 1 is a major factor likewise for this device the W by L may not matter too much. The cascode device we will see very shortly also does not play very important roles in determine and noise of the cascode configuration. Therefore, for the cascode device once again the gm does not play a very important role, and we can afford to sacrifice the gm of this device significantly by reducing the W of this device significantly.

So, you want good gain you know L can still be kept large say 2 micro meter whereas, W can be reduced. So, that the C gs 4 is within limit, because it does not the gain does not depend upon gm of this device just depend upon the ro of the device. So, by taking appropriate design decisions I can try to minimize this combination of these 3 capacitances. So, that they do not interfere with my dominant pole compensation. So, the summary out of this is we just identified that at this you know second pole over here, what are the critical what are the capacitances coming in? Then we looked at the dependency on the dimensions and then we are also trying to see that following other design constraints when we are trying to size different transistors, how those sizing issues are going to affect (Refer Time: 13:23) capacitance over here.

The worst case situation is because of this m 1, because here I do need a good W by L and hence good gm, and that is going to increase a C gd 1. So, that becomes the

dominant factor that is a becoming a dominant conflicting factor for the minimization of c at this point. Other 2 may not be so critical because the sizing of these 2 are favorable to reducing the C gs 4 in C gd. Because first we will see that the W and L of m 4 the product can be minimized can be reduced because the overall W by L does not matter for this device in the overall gain expression because gm of this device is not coming into picture. So, I can afford to have smaller W by L, and despite having a larger L I can reduce w. So, that the overall product C gs 4 is within limit it is smaller that is one thing, and likewise the W by L of m 5 also does not plan any significant role in determining the gain. Therefore, I can perfectly reduce the W by L of m 5 with despite without affecting the gain over here that is another point.

And another sizing constraint for m 5 will come from noise where I am telling you had of time it will require larger L or poorer W by L. So, here even if we have larger L for m 5 it does not degrade the C gd so much because it is dependent upon W and not upon L. So, we should be able to identify that if your other constraints coming into picture for sizing which constrain is conflicting with the stability requirement or compensation requirement. Here the major this filing constant which is conflicting the stability requirement is the gain factor, where I would like to have larger g m for this larger W for this. Otherwise these 2 transistor and they are sizing constraint coming from noise is coming from gain they are not conflicting with our compensation requirement.

So, it serves to have a better idea of the device structure. So, that we can think about which device is contributing to the dominant non dominant pole over here. So, that we can deliciously choose the sizing of the other devices while satisfying multiple criteria say the compensation and the noise together. Another very important factor that we have to also see is the swing, now if we afford to reduce the W by L of these devices as we just discussed what is going to be affected negatively is the swing. Because this once again if a W by L of these devices is reduced we know that overdrive voltage for a given bias current will be increased and then our bias scheme we know that the maximum potential that you can have over here is V DD minus 2 V overdrive. And if you increase the V over drive by reducing W by L swing will be hampered.

So, while you try to achieve or improve one metric the other metric get jeopardized. So, in general that trade off is always there and you have to make a proper try are you have to arrive at the swing spot which is basically catering to the set of specifications you are

trying to implement. And as far as this node is concerned anyway we have seen that the node capacitance node impedance is low and therefore, even if you look at all the other capacitances coming into picture even if it is having a miller multiplication for C gd 5 at this point. Because of the impedance being low it is not going to affect much, but only thing is we have to be careful that if we try to make the bias current of this stage too small to save power once again the gm over here can get reduced and it can become very small 10 to the power of minus 5 10 to the power of minus 6. And in that case the ro here can become the overall impedance over here can become significant.

So, you are trying to save the bias current in this stage by reducing it aggressively the overall small signal resistance over here will become maybe close to ro, because if your insubstantial region transistors are having very small current micro ampere or close to that the gm can be pretty poor especially if you on the top of that if you choose a poor W by L for this and in that case the overall small signal resistance over you can increase and then you also have this miller multiplication for C gd 5 coming. Those things can complicate the stability issues a little bit. So, you have to be aware that you know whatever design choice you make at one point example for reducing the bias current over here that can also influence your overall stability.

Because here also again can bring up a non dominant pole which is probably even lower frequency than this one because it is having a miller multiplication factor of the C gd 5 along with that impedance over here which is getting closer to ro gm is no longer or 1 upon gm is no longer much smaller than ro as you always assume. So, that will push this node even lower than this one. And that will start contributing as a dominant pole. So, rather than this being a non dominant pole this will become the non dominant pole. And create problem with this phase margin. So, although for overall analysis we ignored this pole, but for our particular application if you are looking at low bias current we have to be careful that this does not become the non dominant pole, otherwise it will fight with this one or it can become lower than this one and then interfere with our compensation we are trying to achieve with the help of a compression capacitor over here.

So, that will mandate that then you add another capacitance over here and then try to compensate this one as well as this one So, that this is does not become the non dominant pole this T is the non dominant pole this T is the dominant pole and this is significantly lower. So, all those constraints we can definitely look in simulations and although the

phase margin coming up. So, before we go further any question on you know what is the point be discussed. So, we have discuss a very high level that what is the overall compensation scheme and what are the issues which are going to complicate that compensation scheme. So, we are at the high level we are starting with a easy relatively easier compensation scheme which is dominant pole compensation, but I just tried to mention that what are the issues which can complicate it further. If you want to have a good dominant pole compensation, the sizing constraint of this transistor must be taken care of you should not make this capacitance too large otherwise it will require much larger cap over here.

And the second thing that discussed is that you should not make a end up making this one the non dominant pole. This pole should not end up being lower than this one otherwise you will have to compensate this one also separately by putting even larger cap over here, and then it can. So, any other issue? We have will see; that means, if you want to compensate the common mode loop, right, now we are you know constraint with the single loop and we the same c, c over here or a same cl over here is good enough for communicating both, but in other some applications you may have to keep the bandwidth of the common mode feedback loop much lower than the differential in that case complete more complications arise. And we can look into schemes where these 2 can be compensated separately all right.

So, let us look into the noise analysis for cascode amplifier and try to arrive at the overall input effort noise and try to see the sizing constraint provided by the noise. So, for noise analysis also I can basically go ahead with the differential half circuit. So, ultimately we are going to look at the 2 output nodes separately, because they are going to have uncorrelated in noise. I can look at the differential half circuit and look at the contribution of each of these transistors, we have to remember that the gate potentials of the other 4 transistors are anyway constant. So, they are DC bias points and we have to apply the MOSFET noise, that is a flicker noise at the gate and the channel can noise in parallel with the channel current source of the MOSFET. And then arrive at the final output noise expression divided by the overall amplifier of the gain to arrive at the input referred noise at the input point. That is what we are going to do in brief. So, let us do that and confirm the contribution of these transistors in determining the input of a noise.

So, the steps are pretty similar to what we have done for the 2 stage already.

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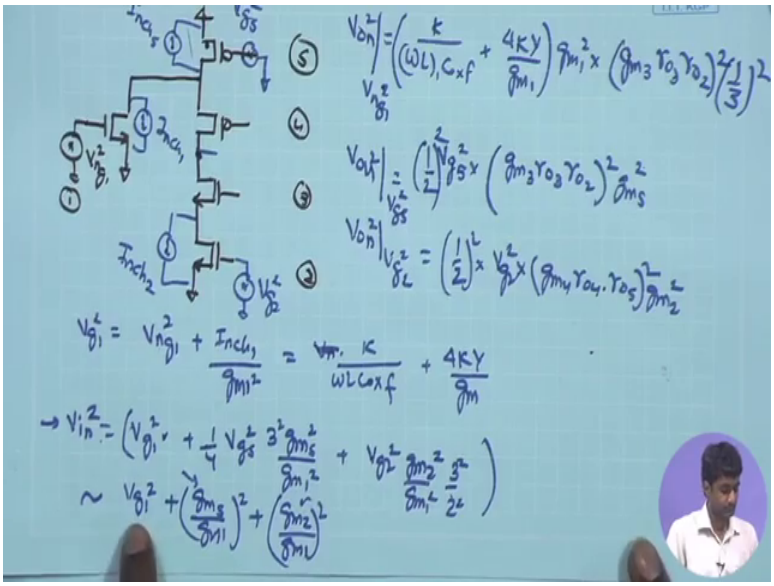

So, the more crucial ones will be the cascode one because we will have to conclude certain things about them. The NMOS and the PMOS connected to the V DD ground they are going to be relatively straightforward as we will see. So, the differential half circuit once again I am putting the source of the input pair to ground. And for the input pair once again I can have the V ng 1 square like where they can just number these let me call this 1 and this is your 2 3 4 5. Now looking at the fifth one and second one and also the first one. They are having their sources at ac ground and therefore, I can easily translate their channel current into an equivalent gate voltage.

So, if I model their channel current I nch 5 and likewise I can model this as I nch 2. Likewise I have I nch 1. So, these are the thermal noise current associate with the channel current for the 3 MOSFETs. And their sources are ground, and therefore, I can also convert this channel current into an equivalent voltage at the gate. And the conversion is simple you just need to divide this channel current value by the gm square. Because the equivalent noise voltage V ng square times gm square will result in this equivalent channel current. So, I have 2 sources of course, for the flicker noise anyway represented with the voltage contained in series with the gate because the mechanisms of flicker noise it arises because of the interaction between the careers and the dielectric and effectively results in an overall wave V T shift between our vt shift for the MOSFET. And that can be modeled as an gate voltage in series with the MOSFET. So, we try to model the flicker noise as a vt shift right, if you remember our discussion the basic origin

of the flicker noise is that it is arising because of the trapping of charges which is basically changing the voltage drop across the oxide and in effect it is changing the required amount of positive gate voltage or positive charge on the gate voltage to balance the equivalent of negative charge in the channel.

So, if you are having certain bias current and assuming that the bias current is fixed and therefore, the charge in the channel is fixed right. So, assuming that the channel charges remaining fixed and on the top of that you have the MOSFET gate where you are putting positive charges, what we have is the charges current is fixed in the bias current is fixed we assume that this is fixed and because of the trapping the trapping; however, you are having some additional charges coming in. So, this q is changing over time as a result what we say is the required amount of charge to have the same amount of channel charge over here, the required amount of positive gate charge to have the same amount of channel charge over here also keeps fluctuating.

So, what we can say effectively that the effective vt of the MOSFET fluctuating, and how do we represent that by putting a voltage in series with the gate of the MOSFET. That is why this flicker noise comes in series with the gate of the MOSFET. And so, you can effectively see is at the at of the noisy vt of the MOSFET whereas the channel charge comes because of the electrons transiting through the channel and having random fluctuation in the conduction path. So, if I want to translate the gate voltage or the noise voltage into current that is possible by multiplying it with gm square. Likewise if I want to convert the channel current into an equivalent gate voltage and again divide it by gm square, provided the source of the MOSFET is ground. Because only in that case I can say that this equivalent Vg square Vgs square times gm square would result in such a channel current. So, let us do that for each of these I can write down the Vg 1 square as the V ng 1 square which is inherently because of the flicker noise which is automatically modeled as voltage source in gate with the in series with the gate of the MOSFET.

So, I do not need to do anything for that, but I have the second one which is I nch 1 divided by gm 1 square. And I can do this only if the source is grounded. And therefore, I have the V ng 1 square which I can express this as the flicker noise. So, you have k upon W L co x times f plus I channel upon g m 1 square. So, we have 4 k T gamma g m which is the expression for the channel can noise divided by gm. So, this is the expression for the Vg 1 square. So, I will just call it the Vg 1 square the total Vg 1 square which is the

Vng 1 square because of the flicker noise plus this channel current divided by g m 1 square. So, this is I can I can just denote it like this. And likewise I can do it for others also I can express the total current total noise of this MOSFET as Vg 5 square and likewise for the 2 I can represent it as Vg 2 square and simple as that. And then for each of these I can see that they are acting like the input device of cascode amplifier.

So, if I take m 1 this is acting like the input device of the cascode, if I am calculating the effect of Vg 1 square the others will be set to 0 and I will just calculate the output voltage because of the Vg 1 square. And we know that the what is the gain from the input to the output we have already calculated that, we have a 1 by 3 factor times gm square ro square. So, let us write that down, but we should also be careful about picking the right, gm because ultimately we have to look at the overall input referred noise and we are divided by the overall gain of the circuit. Which is gm 1 square times ro square. In all these cases ultimately at the output point we are going to get the ro of this MOSFETs.

So, just in order to distinguish that which gm and which ro is going to contribute to noise in which fashion, I would like to preserve the subscript I should not simply write it down as gm ro wholes square I have to identify with gm in which I ro contributing in what fashion. So, let us preserve that for subscripts. And calculate the vo vo n square there is our total output noise because of the Vg 1 square, that is going to be a k upon W L 1 times co x times f plus 4 kt gamma upon gm 1 times gm 1 square times the impedance over here the overall output impedance that we get because of that the m 3 and m 4. So, that is basically gm 3 square we have to keep the square. So, gm 3 ro 3 times ro 2 square.

And we have the factor of 1 by 3 coming in also that also we have seen because the current gets divided you have r over here r over here and another ro here. You know that 1 by 3 factor comes in and then we have this expression. Now when we get the input reference because of vn g one we will be dividing it by the same factor. So, this will be divided by the same factor basically, this is vo n squared divided because of V ng 1 V ng 1 square. Likewise I can write down the vo n square output noise voltage, because of the Vg 5 square now for the Vg 5 square let me just write it Vg 5 Vg 5 square times the overall gain from input to the output. Now once again if we look at the overall operation if I am looking at the gate voltage of this one what is the impedance provided by this? We have just discussed while discussing the common mode response.

So, there I will not treat this as ac ground, because if I am looking at the signal over here and putting this signal at the gate of m 1 at a c ground; that means, both the signals the input signals at ac ground, and after that you have another current source which is also ac ground therefore, this will represent aspect NMOS which is having an impedance of gm ro square. It was not be just ro it will be gm ro square. Now, therefore, while considering the effect of this Vg 5 I will ignore this branch just like we would did in the common mode feedback analysis let distinguish that distinguish should keep in mind. When we are analyzing the effect of this Vg 5, we are ignoring this branch why because the input signal is 0 therefore, you have stacked transistors 2 NMOS with gate voltages at ac ground therefore, the impedance looking into that drain is gm ro square here it is just ro and therefore, I can ignore this safely.

So, I ignore this and therefore, this is our simple cascode amplifier with input signal at this PMOS and therefore, the input signal is Vg 5 square and that I have to multiply by the gain of this circuit resulting from this amplifier and we know that when we calculate the gain of the circuit we get a 1 by 2 factor because of the current division at this point ro up ro down or in this case basically ro of this m 5 and ro of the remaining circuit. And that multiplied by the overall impedance over here. So, that is again going to be gm 3 ro 3 ro 2 square So same factor. And also this whatever 1 by 3 factor that I have written that is also going to be 1 by 3 square because ultimately we are looking at the current square.

So, this is the for the first branch also current square and therefore, the division factor 1 by 3 also becomes square. So, I just missed a square for the 1 by 3. And now the last one is the Vg 2 So vo n So, this is because of Vg 5 and likewise vo n square because of Vg 2. So now, for Vg 2 situation is very similar. Only thing is we are going to get the impedance looking upward. So, for Vg 2 the expression for the gain from input output is same as what we have from the Vg 5 to output. Only thing is in terms of the MOSFET the impedance will be contributed by m 3 m 4 and m 5. This node is again not going to contribute much because when I am analyzing the effect of Vg 2 once again this MOSFET is going to represent the impedance of gm times out of square because of the 2 stag MOSFETs coming into picture it is not an ac ground for that operation.

and therefore, I can once again simply ignore this looking at the gate of this m 2 I can find out the output voltage over here which is going to be again 1 by 2 square. Square times Vg 2 square times the overall impedance looking up because remember half of the

current goes up and then it gets multiplied by this impedance which is basically gm 4 ro 4 times r of 5 square. So, this is the overall output voltage because of the contribution of m 5 m 2 and m 1. Now if I want to look at the input referred noise because of these 3 combinations I need to divide all these 3 components by gm 1 square times the ro 3 the basically impedance looking downward from here square. There is the gain from the input to the final output over here that is what we need to do and.

Student: (Refer Time: 34:54) gm 5 square and the cascode amplifier.

Yes sorry, you have missed the gm factor. So, Vg 5 gm 5 square yes yeah. So, ultimately we are looking at the voltage. So, gm 5 square likewise here also g m 2 square g m 2 square alright. So now, we have the expression for the output voltage, in terms of the gate voltages 2 5 and 3. And all we need to do for getting the input reference is divide this factor by g m 1 square g m 3 g ro 2 ro 3 square by 1 upon 3 square this is the again. And therefore, I can look at the V in square because of these 3 I have not talked about the other 2 let us discuss that later first we calculate this. And now if I take the assumption that these are symmetrically biased and the sizes are also symmetric under that condition I can assume that there are ro the similar just for simplicity. Remember that the bias current in this branch is different and you may have a basement over here which is double. So, the ro of this one may be lower almost half as compared to the ro of this, but just for simplicity just to keep the number simple I am assuming that these 2 r having similar ro and gm and these 2 are having similar sizes these 2 are having similar sizes. And therefore, I can replace the gm 4 ro 4 ro 5 by gm 3 ro 3 ro 2.

So, let us do that. So, I have the Vn 1 square given by the first term which is Vg 1 square this term gets divided as it is. So, you only get the Vg 1 square plus you have the second term which is Vg 5 square divided by this number and this again gives divided by 1 upon 4 you have Vg 5 square. And this term goes as it is you have the 3 square terms coming in. So, you will have the 3 square coming in over here and you have the gm 5 square term coming in gm 5 square. So, and the divides by gm 1 square. So, I have just divided this second expression by the gain g m 1 square times this number. So, this is the second factor which is coming in. And then I have the third term which is the V v g 2 square divided by once again the same factor over here. So, I am getting g m 2 square divided by g m 1 square and once again this gives me 3 square in the numerator. And you have the 2 square coming in any way in the denominator 2 square here.

So, that is that is the input referred noise vin square because of the 3 components. And once again these are the constant terms. So, they are not going to be very important the important factors are the dependencies on the gms of these individual devices. So, here if I look at the dependencies and preserve only the gm terms I am getting Vg 1 square plus gm 5 upon gm 1 square plus g m 2 upon gm 1 square. And if I look at this ratio definitely it means that I would like to increase the gm 5 upon gm 1 ratio, I would like to reduce the gm 5 and gm 2 as compared to gm 1. So, I would like to reduce the gm of 5 I would like to do the gm of 2 and I would like to increase the gm of 1 for getting a better noise. And likewise I have the Vg 1 square also coming as it is. And of course, I have to multiply it with the Vgs Vg 5 square and Vg 2 square respectively.

So, of course they are going to have their own divine dependencies on the devices. Why we can write the entire expression? But at least in terms of gm, but we can see is that definitely increasing the gm 1 is going to help us in bringing the noise contribution of these 2 down. If we look at the Vg 1 square itself there also we have the dependency on gm 1 upon gm, 1 because you have the channel noise is getting divided by gm 1 and therefore, you have the overall factor which is proportional to 1 upon gm bar. So now, we can elaborate the expression a little bit more and write down the expression for Vg 1 square we have already figure it out over here.

So, I can write down the Vg 1 square which is k upon The W L co x and f.

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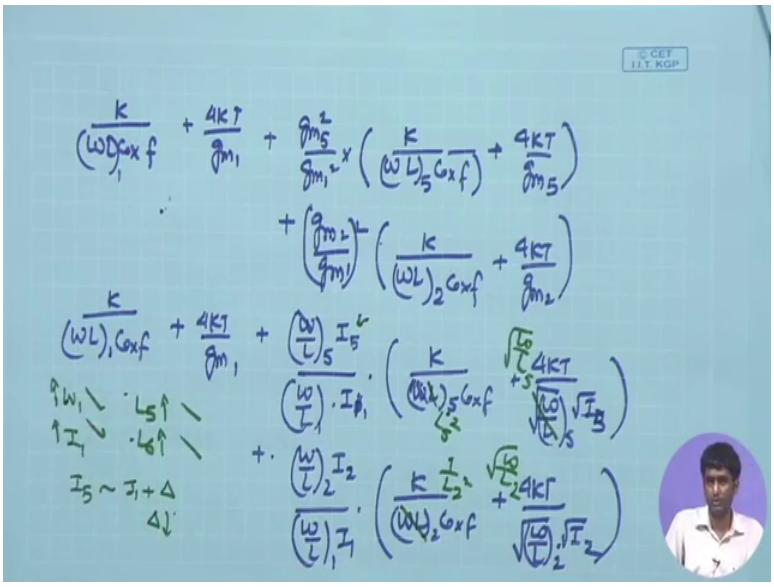

And you have the 4 k T upon gm 1 this is W by L 1. And likewise you have the second term which is gm 5 square upon gm 1 square times the Vgs Vg 5 square. And Vg 5 square, once again we know the stream factors are going to come there for k upon W L 5 times co x times f plus you have the 4 k T upon gm 5. And likewise you have the third term coming in gm 2 upon gm 1 square times Vg 2 square which is also having the same factor which is k upon WL 2 co x f plus 4 kt upon gm 2. So, these are the terms that you finally, have and I can once again break this gm also down into their respective expressions. And look at the W by L expression or W by L dependencies for all these individual transistors.

So, for the gm 1 it is clear we have the increasing the W and L 1 it seems like it can increase the if I increase the W of the input device that can definitely help me in reducing the 1 upon f noise. Likewise having a larger gm 1 is reducing the thermal noise for the input device. Likewise if they look at the other 2 expression definitely larger gm is helping us in reducing the overall noise contribution for all other device. So, without any doubt I can definitely say that increasing gm 1 is going to help and other components over here gm 5. And gm 2 also give us him that yes increasing reducing gm 5 gm to may be possible method; however, we are looking at the thermal noise contribution because of gm 5 and gm to they are coming in the denominator. And they can once again if you if you keep the gm 2 and gm 5 too small they can start dominating.

So, again there is a trade off with the 1 upon f component and the thermal component. Let us break it down further into W by L dependencies. So, get more clarity. So, gm 1 is having W by L dependency, and gm 5 square if I just look at the parameters we are going to have the I D 5. And you are going to have the W by L. So, if I look at gm 5 and gm 1 once again their currents are end of ratio. So, if I can assume that the DC currents in m 5 and m 1 and entire this pack they are kind of ratio they are not independent. So, for example, I can keep a total current I over here and I over here the total current in m 5 is going to be sum of these 2. And also the current in m 5 and m 2 are also proportional.

so however, if I look at gm 5 it may seem that it means having an appropriate division of the bias current in these 2 branches can help. So, if I am taking larger fraction of the bias current here in order to increase the gm 1 whereas, a lower fraction of the bias current coming over here at least it will reduce the gm of the m 2. So, we can write down this as W upon L 5 I D 5 and we have a gm 1 square which is W by L 1 times I D 1 likewise you

have the k upon W by L W times L 5 co xf plus 4 kt. Here you are going to get root under W by L. So, 5 times root under I D 5 I 5 whatever I have mentioned. And likewise in the last term I have the g m to m 1 g m 1 ratio once again W by L 2 I 2 let me call this I 1 2 keep same notation I 5 means the drain current in m 5 I 1 means drain current in m 1. And I have W by L 1 times I 1 and likewise you have the WL 2 co co fx kt upon gm 2 which is W by L 2 times I 2.

And So now, if I look at the W by L dependencies I can take this in and therefore, you will have the L square 5 coming over here. So, if I take this in I have L square 5 coming in this term. So, I have L 5 square in the denominator and here; however, I have once again root under W by L coming into the denominator. So, this gets cancelled with the term and I have root under W by L 5 coming in the numerator. Likewise in the denominator expression I have the W getting cancelled and this is going to give me the 1 upon L 2 square in the denominator and here when you are cancelling this you are getting the root under W by L 2 term in the numerator. And therefore, increasing the L 2 and L 5 definitely can help us in minimizing the noise contribution for the noise contribution of the m 5 and m 2 stacks.

So, these 2 transistors contribution for the overall noise can be suppressed by having a large channel length for these 2 devices. And at the same time if I look at the overall condition for m 1 having a larger W for m 1, and having a larger bias current for m in terms of I 1 it is going to definitely help us in reducing the noise contribution for the overall amplifier. And likewise it is also going to help us in increasing gm 1. So, larger W 1 larger I 1 is going to help us in achieving overall lower noise contribution. Likewise L 5 larger L 6 larger is going to help us in reducing the overall a noise contribution. And likewise if we look at the bias current contributions once again for I 2 and I 5 we can see if we take I 2 and I 5 inside both of them are coming in the numerator in the first one and in square root or I 5 and I 2 coming in the second expression.

So, they are not trading off that significantly and they are all proportional to I 1. So, if I just keep the ratio of I 1 upon I 5 and a 1 upon I 2 upon I 5 sufficiently large that can help us, but you remember that I 5 upon I 1 ratio is you know not in our control. So, I 5 is anyway going to be greater than I 1 I 2 if you make the I 5 say close to I 1. So, I 5 you make close to I 1 allowing a smaller current to flow in I 2, then you have this term overall getting reduced. So, I can what I can try to do is the tail current source I 5 I can

try to make it I 1 plus delta. And this delta if I had to reduce if I try to reduce the delta that will reduce the I 2 and hence I 2 upon I 1 ratio and therefore, it will reduce the contribution of this term further.

So, having a larger I 1 having a smaller delta which is basically I 2 which is determining the I 2 upon I 1 ratio can also help in minimizing the overall noise contribution of these transistors. So, we have arrived at the dependency of the overall input referred noise on the bias currents of these devices. And also the dimension of these devices and important takeaways with respect to sizing is a large L 5 large L 6 a large W 1 and significantly strong dependency on the input bias current. So, once again the bias current of the input stage is going to play an important role and if you want to especially minimize the 1 upon f noise 1 upon f noise corner. So, once again for that I will be equating this 1 upon f expression with the remaining white noise expression. And there once again we will see that the I 1 will be coming in the numerator. So, if I take away all the 1 upon f expression from this bracket and equate it to the other terms you will see that I 1 will be coming in the numerator and therefore, in order to reduce the 1 upon f noise once again I 1 is going to play an important role. Likewise W by L 1 is going to play an important role.

So, 1 upon f noise corner will be dependent upon I 1 and W W 1 of the input device strongly. And likewise thermal noise contribution we can look at the other dependencies reducing the I 2 reducing the gm of m 5 and m, m 2 by having a poor W by L or larger L for these devices, that is going to reduce the thermal noise contribution because these devices.

So, this is going to give us some additional you know design steps and when we are trying to optimize our folded cascode amplifier to meet overall set of specifications. This is giving me another set of constraints and is going to play an important role in fixing the sizes of input devices as well as just stack devices in the cascode. So, here you told you to go back and look at the constraint that we discussed (Refer Time: 49:47) stability that is what is happening when you trying to compensate the loop and which capacitance is dominating which device is contributing. So, once again from here we can go back and let us check that what happened to that compensation schemes. If we discussed if we go further noise minimization whether it is conflicting with my compensation scheme. And whether it is increasing the capacitance at the non dominant pole. And so far another

important point that you have not answered is the contribution of the cascode devices there is 2 middle 2 devices we have not counted to let us discuss that briefly.

Any question before you proceed? So, we can take a short break and then come back address the other implementing issue that is the condition of the cascode devices and the other design tradeoffs whether it to the bandwidth and gain. How do they conflict with the noise requirement.