Analog Circuits and Systems through SPICE Simulation
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Lecture - 56
Folded Cascode Biasing (Contd.)

Welcome back, and let us start with today's module we will continue with our discussion on folded cascode amplifier looking into the biasing schemes for the single ended output as well as differential fully differential output cascode amplifier. And along with that we will be going into the common mode feedback for the fully differential scheme. We will also look into a noise analysis for the cascode amplifier and try to draw analogy with whatever we did for the 2 stage amplifier. And we will look into some other variants of the folded cascode topology to get better input swinging and so on. And finally, we will look into sizing consideration to meet a certain specs like how to arrive at the required sizing for the input device cascode devices to meet specs in terms of say bandwidth gain noise output swing and so on.

So, we will focus only on the specs which are relevant to our example some of the specs which are applicable in general to an opam may not be very relevant to our example, but we will focus on those specs which are crucial for particular design example that we have started with the front end for our biomedical sense the interface. Let us get started with the folded cascode circuit we discussed in the last class and finish our discussion on the biasing.

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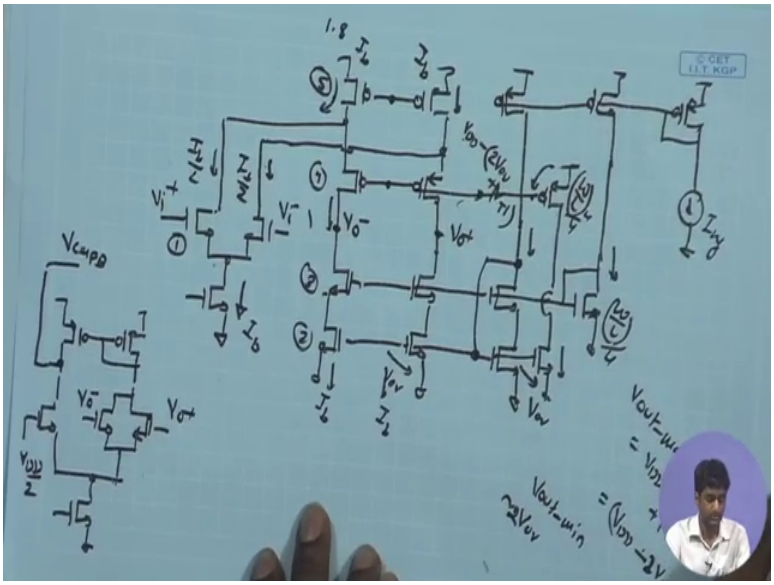

So, we discussed how to bias the NMOS transistors in the bottom stack. So, quickly let us read all that.

So, here using there is a jumper and for biasing the stack over here we can use the cascode scheme that we discussed, reduce swing cascode using that there is a I ref coming over here which is common to both these branches. So, you are having same I ref getting injected in these 2. So, I can just for the sake of completeness I can draw the I ref branches, suppose they are getting blurred with some reference branch. So, you are when I connect this it means of course, the gates are connected. So, whenever I am crossing these lines horizontally means the gate of the corresponding MOSFETs lying in that horizontal line are all connected otherwise whenever I have dot then they have a connection.

So, if the horizontal line is crossing through the gate; that means, the gates are connected. And here you can have a reference branch which is a generating the I ref. So, you are having a I ref over here, which is getting mirrored in both these branches and as we saw a yesterday this can be w upon l by 4 if these are all W by L. So, this way I can ensure that the minimum allowed signal swim over here is close to 2 V overdrive that is what we discussed yesterday. And we also need to look into the biasing of the top branches, and for that once again I need to first look at the PMOS over here let me call

the number of stacks as, let me number the input pairs has 1 2 3 4 and 5. And here I can bias the PMOS transistor over here using a similar scheme that I used for the NMOS over here.

So, I can use a PMOS with a similar bias current. So, I can take a bias current from here, and by the same bias current and with this I can try to bias the PMOS stack. And again I can try to make sure that the W by L of this is one upon 4 times W by L of this 4th pair. So, the W by L subscript 4 means W by L of 4 and upon 4 means the ratio W by L ratio of this particular transistor is 1 by 4 times the W by L of this. And of course, I could have used similar scheme just like you have the NMOS over here producing the gate bias of this stack. And you have the 2 bottom NMOS I could have used another bottom another you know PMOS pair to bias the voltages over here, but we will not do that because we need a scheme for obtaining a proper common mode DC level over here.

So, before we go there we can see what is going to be the overdrive voltage for this MOSFET and corresponding that what is going to be the gate voltage for this MOSFET and hence the maximum output a swing that you can achieve at this point. So, if I am having the same I ref flowing in this device and therefore, we are once again expecting that the overdrive voltage of this MOSFET will be 2 times the overdrive of the NMOS over here. So, if this device is having V overdrive. And you are having the same dimensions over here this device is also having V overdrive. Therefore, what we expecting is the V SG of this MOSFET is going to be V DD or rather a mod V T plus 2 V overdrive because W by L is 4 times. Therefore, this potential this DC potential will be V DD minus V SG which is 2 V overdrive plus mod V T. Assuming that the MOSFET parameters are similar NMOS and PMOS parameter are similar.

So, this particular gate voltage will be V DD minus V SG of this MOSFET. So, this is V DD and we assuming that this is 1 by 4 W by L as a result assuming that the overdrive voltage over here is going to be twice as a result the gate potential is 2 V overdrive we effectively basically the V overdrive of this particular device plus mod V T. And hence the maximum potential that you can have here is this V G plus mod V TP. And therefore, the V out max under the scheme once again is close to the maximum value that like to

have which is V DD minus 2 V overdrive plus 2 mod V T because you have this number plus another mod V T.

So, gate voltage plus mod V T is a maximum allowed value therefore, you get V DD minus sorry is a it has to be V DD minus. So, here basically you are having a V overdrive which is V GS minus V T and as a result if I am biasing this a gate potential to V DD minus V SG where the V SG is going to be equal to the V overdrive plus mod V T. And as a result the potential over here that you can have at the max is just. So, just what is. So, you have V DD minus. So, you have the overdrive voltage of this which is twice as compared to the overdrive voltage of this one. And as a result you are having the V G which is V DD minus V SG. So, V SG is basically the V over drive of this MOSFET is twice plus mod V T of this MOSFET. As a result you have the V G which is V DD minus 2 V overdrive plus mod V T. As a result the maximum potential that you can have over here is plus this plus mod V T sorry. So, you have a minus sign here plus. So, minus 2 V overdrive.

So, this is what we expect and as a result once again on the upper side I have the V out max which is V DD minus 2 V over drive. And lower side anyway we have ensured that it is going to be V out min is also going to be 2 V overdrive on the lower side. So, the gate potential of your the 2 PMOS over here for the 4th pair has been set accordingly. So, that we get the maximum potential over here. But now we also need to set the gate potential of the top most PMOS pair, and there we need to have some controls So that we can determine what is the common mode DC level. And there once again we can take the help of a common mode feedback amplifier error amplifier So that we can set a desired potential over here.

Now, since on the upper and lower side we are able to achieve symmetric swing as compared to the V DD we have a symmetric swing available over here on the upper side can go maximum to V DD minus 2 overdrive. And on the lower side it can go to 2 V overdrive. Therefore, the a good biasing point would be V out max plus V out min by 2 which is basically a V DD by 2 approximately. And therefore, if I am going for 1.8 supply volt I would I can afford to keep the output DC potential close to a 0.9 volt and in order to do that once again I can take the help of my error amplifier.

Now whether I choose an error amplifier with a current mirror load or a diode connected load that is another question. For that we need to look at the a loop gain. Once we apply that error amplifier in this particular circuit and try to obtain the bias point for the PMOS, we need to make sure that the overall loop gain is within limit preferably we can stick to gm ro whole square rather than going to gm ro cube. So, a good limit would be gm ro square. And also we need to see whether the same a compensation scheme for the differential operation is able to a stabilize the common mode loop.

Now, another question that I would like to ask about the common mode feedback whether to use PMOS load and NMOS input device or use NMOS a load and PMOS input device. And here we can see that arguing the bias point is supposed to be provided for the PMOS load. And therefore, the gate voltage over here the output of the error amplifier the DC point of the output of the error amplifier is supposed to be close to the DC bias point of this gate. And therefore, it is advisable to choose an error amplifier with PMOS load. So, that it is output DC point output bias point under the stable operation is close to the DC gate potential of the PMOS. Therefore, I will use a PMOS load error amplifier. And I can once again use the split transistors to obtain my, here using the split transistor becomes all the more important because the output impedance is pretty high and we may not like to redecorate the overall resistance over here.

So, since the overall gain is dependent upon the high impedance at this node we would not like to degrade it by putting a voltage divider. So, this becomes all the more crucial to use a split pair for extracting the common mode level. And then we have to decide the polarity. So, if this is if I call this say Vi plus and Vi minus. So, with respect to this if I say if the input signal Vi plus is going high we have an overall inversion over here. So, from here to here in this particular branch we are having V o plus at this point Vi V o minus at this point it is a overall inverting gain if Vi plus goes high this current goes up this current reduces and if this current over here goes up remember this is supposed to be providing a bias current it is fixed with some DC potential.

So, this current is going up; that means, the current in this branch is reducing. And as a result the current supplied in this particular branch is going down. So, if this is going up and hence this current the larger fraction of the current provided by the PMOS is being

sunk by the pair the input side over here; that means, the current going into the bias branch over here is reducing. As a result you will have this particular potential going down. And on the other side this potential will be going up, because if the Vi plus is going up and this is going down this current is reducing this current this current reducing; that means, the a smaller fraction of the total current provided by this PMOS is being sunk by the second input device. And hence the current in this branch is going to increase as a result this output potential is going to go up.

So, that to we can understand which one is the positive one and which the negative one. So, we have V o plus and V o minus. So, of course, the gain point of view we have done the analysis and we know that if I look at the single ended version I have a overall inverting gain. So, whatever side we are looking at if this is V I plus I get the V o minus over here because this is going to be inverting and this is going to be the non inverting. So, this is V o plus and from the point of view of current directions also we can look at the circuits. So, if you are having the total bias current I bias provided by this MOSFET and suppose the total bias current in the stack is also each of them is also having I bias by 2.

So, in this case under DC condition both of these input devices are assumed to have I bias by 2. And assume that you have the same I bias by 2 in the 2 stacks. Therefore, in the DC condition I would like to have I bias in these 2 MOSFETs also. And then if your signal excursion is taking place one of the signal is going up, we can look at the current value that we just discussed Vi plus going up means the input signal in this branch going up with respect to I bias by 2.

So, nominally it is supposed to have I bias by 2 I bias by 2, but Vi plus going up means this current going higher than I bias by 2. And hence the current flowing in the cascode branch will be falling lower than I bias by 2. Whereas, the current in this branch will be becoming higher than I bias by 2 definitely V o plus will be going up V o minus will be going down. So, using the current directions also we can arrive at the definition of the polarity at the output points. This is by V o plus and V o minus I can connect it over here V o plus and V o minus and then again if I am trying to set it to a particular DC potential I would put the V cm ref over here which is close to V DD by 2.

So, I will put the DC potential over here V DD by 2. And then I have to see what is the polarity required. So, if the V cm is going up; that means, I would like this gate potential to be pulled up. So, that it goes down. So, if the output common mode goes up, and corresponding to that if I make the PMOS gate potential go down it will try to reduce the currents over here. And as a result this the overall DC current flowing in this stack will try to go down. Where as the gate potentials of these MOSFETs are fixed and since the current is trying to go down, it will try to pull down the drain potentials such that the V ds reduces and hence the DC potential comes down.

So, I would like to connect the output once again over here, and this becomes my V cm fb common mode feedback. The common mode output going up; that means, this signal will be going up and it will be increasing the PMOS gate potential. That would reduce the total current over here. Remember this current is remaining fixed because this is bias with the help of I bias or another reference branch. So, this is remaining fixed as a result when this gate potential increases; that means, definitely the current going in this stack is reducing. And if current going in this stack is reducing and these 2 gate potentials over here they are fixed; that means, the drain to source potential must go down to support reduced current in this stack and hence it will try to maintain the same common mode DC potential as the reference DC potential over here. Is it clear and any doubt?

So, this is the way we have completed the DC bias for the overall fully differential cascode amplifier. We have to yet to we are yet to address the question of the load choice of the load. We have answered the type of transistor for the load the input is NMOS and output the load is PMOS. So, that we can get a DC bias point over here which is close to the gate potential of a PMOS. So, that is what we have just discussed and; however, we would also like to make sure that the overall loop gain is sufficient is within limit. So, a good number is gm ro square it should not be gm ro cube. So, that stability becomes an issue.

So, for that we need to figure out that in the overall common mode response, what is the loop gain? So, we can go through the towards the common mode half circuit analyze that before we go there any question regarding whatever we have done So far? And remember the input DC bias point is once again we can obtain it using large resistive

feedback from the output to the input. So, we are not worrying about the input DC bias point. And the advantage of the folded cascode is that having the output DC point remaining the input DC point does not affect the output swing we saw that if you are having a the unfolded case the normal stacked a cascode amplifier differential version there of course, the output one output DC potential it cannot be directly connected to the input DC potential because it affects the output swing negatively.

But in the case of folded cascode the output DC potential over here is not directly impacting the input swing over here. And therefore, it is convenient to directly connect the output DC potential to the input DC potential that.

Student: (Refer Time: 19:22) we will do not need any high resistance to (Refer Time: 19:25) connect a output and the input of input (Refer Time: 19:28) biasing.

Once again yeah. So there the high impedance resistor you are realizing using transistor. So, that is very high value. So, as compared to if you use such high resistors to extract the common mode they are very imprecise. So, for common mode we want that these 2 resistors should be matched whatever resistors you are applying over here. So, if we use such active devices operating in the sub threshold region and expect that it will be able to extract the common mode voltage that is not a very practical way, because each of these a active or you know a MOSFET based resistors will having will be having a lot of process variation it will not be very well matched.

So, it is for the biasing of the input we do not need them to be matched, because as long as the resistor is very high it will ensure that the overall frequency response is not significantly impacted at the same time it will also ensure that the gate potential over here DC potential over here is close to the output DC potential or basically to output DC potential there I do not need matching. So, even if there are 100 percent mismatched one of them is r another is r by 2, but those are very high both r and r by 2 are very high the DC potential here does not get affected neither the output DC potential get affected.

So there I do not need to worry about matching of those high resistance connected from output to the input to adjust the input DC bias, but when you are using the common mode feedback for that the common mode has to be extracted faithfully it has to be these

2 transistors have to be matched. Passive resistors you can match it using appropriate layout technique that will be discussing in subsequent classes may be in a trading also we can discuss briefly. So, that that can be well matched, but if you are talking about say this resistors implemented using MOSFETs operating in deep sub threshold regime, there the 2 devices though to the 2 resistor that you are trying to construct can have very drastic mismatch and that will not allow you to extract the common mode potential faithfully.

And hence it is not a suitable technique to do that. So therefore, we are relying on this active devices which is well matched which can be well matched and they are helping us in extracting the common mode signal faithfully, while those crude resistors high value crude resistors can be used to just obtain a proper DC point at the input because at the input you do not have any other current path. So, you should once the moment you connect this output with any very large value resistor even if these 2 are different it does not matter it will set the input DC point sink any other question? Ok.

So, let us look at the common mode loop and consider the stability. So, half circuit point of view we will once again we can visualize what are we going to do So for the half circuit these 2 nodes are going to be DC potential. So, I am going to set these 2 AC ground this is also a DC potential this is also going to be set to AC ground. And I have the output of the common mode feedback amplifier coming over here. What should I do? The input is also AC ground and this currents was is also an AC ground. So, input point of view also we are just going to have a overall impedance looking into this drain because these 2 are set to AC ground I am just analyzing the common mode feedback loop.

So, effectively if I just want to preserve the exact numbers and take care of the multiplying factor whether 2 is going to come or not I should be a clubbing these 2 devices up. So, if it some these 2 up I am going to get 2 times gm one over here. So, let me club these devices 1 by one and construct the common mode half circuit.

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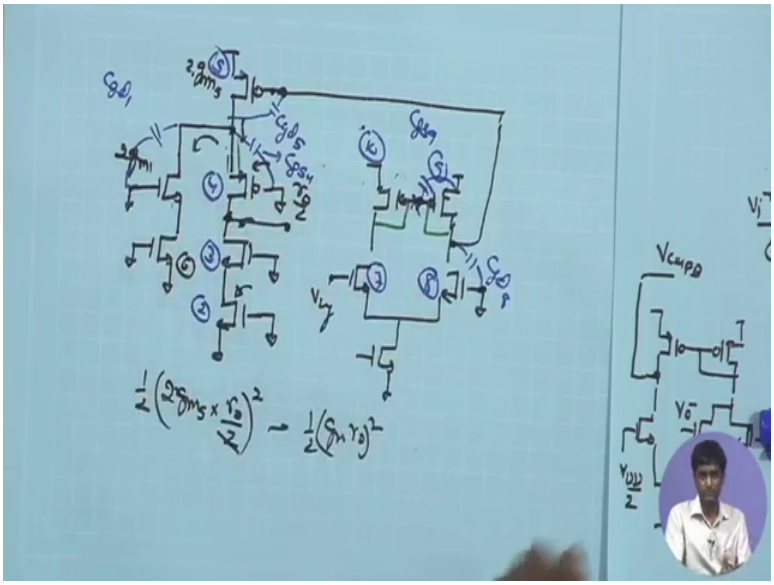

So, this is going to be 2 times gm one because after clubbing these 2 common mode we had W by L getting twice and I getting twice therefore, 2 times gm one and gate is anyway AC ground and you have the you call this six. So, you have the m 6 also the gate being AC ground.

So, this is your m 6. And on other side you have the PMOS once again you are clubbing these 2 PMOS. So, you are going to have gm 5 twice gm 5 coming over here. And the gate is supposed to receive signal from the error amplifier. For m 4 once again if I club the 2 m 4 over here we are going to get the overall bias current getting doubled and hence the ro if you are looking in for m 4 is going to be ro by 2 of the individual m 4. So, we just be careful about the ro of the m 4 and then you have the m 3 and m 2 also getting clubbed together with gate set to AC ground because they are all DC potentials. And these are also going to be having just half the ro by 2 each of them are also going to have a half the ro by 2.

Now if I look at the error amplifier you have the let me decide upon the load connectivity later right now, connected than anyway. Now once I have connected the outputs this was my output have opened the loop over here suppose and I have connected the 2 outputs together therefore, the split transistor also becomes combined. So now, I have these 2 combined and the gm of both devices are same and here I have I am putting say in AC

ground over here. And I have the V ref coming over here which is a V DD by 2 and the output is supposed to be coming back to the potential over here.

So, once again I can trace my gain from this input point to the final output coming over here. And based on that I can decide whether to choose a diode connected load or choose a current a mirror load. So, if I look at the I know the gain of this stage if I choose a diode connected I know what is the gain and if I choose a current mirror load I know what is the gain. So, let us first see the gain from here to here. So, this is nothing else, but simple a stack cascode amplifier single ended cascode amplifier. The only factors if you want to be accurate is that here if I look at the impedances at this particular point you have a large impedance coming over here.

So, if I want to get the exact value of the gain once again here you have a small signal current produced by this m 5, which is going to be getting divided between this branch and this branch what is the impedance looking in downwards? Just arrow here gm ro square this is much larger other I can all together ignore the presence of this branch in comparison with the signal going down. And as a result I am left with basically my only the cascode stage this may not play an important role because there is providing a much larger impedance at this point. And as a result the overall gain from this stage we know it is going to be gm times ro whole square by 2 and we know that the overall ro has been clubbed together.

So, it is basically 2 times gm of m 5 if I want to accurate. And then you have the ro by 2 coming for all the MOSFETs together they have been divided by half. So, 2 times gm 5 ro by 2 square by 2 is the overall gain that I can expect from this loop. Therefore, the order is gm ro square that that is what we can see. So, same as one upon 2 gm ro square. And also now based on this we can determine what should be the connectivity over here. So, this is a gain provided by this stack is gm ro square. I would like to restrict the loop gain to gm ro square. So, that the compensation can be achieved much more conveniently. And therefore, I can choose this to be a diode connected load. So, rather than having a current mirror I will disconnect these 2 a gates and connect them separately using diode connection. And in that case again of this stage is just close to

unity and hence the loop gain will be close to gm ro whole square by 2 which is a desired number.

And So, this is the overall open a loop the overall loop gain for this common mode feedback. And once again we have discussed what are going to be the critical poles in this loop gain. So, these 2 are going to be now high frequency nodes because they are diode connected. So there I am going to give you dominant poles. We have of course, the dominant pole over here because the impedance at this point is pretty large gm ro square, and here you have approximately ro. So, this is the dominant pole these are the non dominant poles and we have seen that just by putting a capacitance over here we can make sure that the overall loop is getting compensated.

So, we can we can use a capacitor value here which is a gm ro times the parasitic capacitances over here, and that can facilitate the stability of the closed loop. So, that is what we have discussed yesterday and we have discussed that the total parasitic capacitances over here can be close to say around 100 femtofarad at the max and for a technology, if you even if you use larger MOSFETs the total capacitance over here can be limited to 100 femtofarad. Of course, you have to be careful because a some of the devices are going to contribute a strongly to the overall capacitance, which one of these 2 PMOS is going to contribute more to the capacitance? Because that compensation criteria is also important to me, because you are assuming that the capacitance over here is small therefore, nominal capacitance value of few pico farad is sufficient for compensating that.

And if you are assuming that this is few pico farad is sufficient I would have to make sure that this total capacitance over here is not more than say a 100 femtofarad close to that, So that gm ro if I am targeting a gm ro of around 100, this a few picofarad of capacitor higher than order of magnitude couple of orders of magnitude higher than this 100 femtofarad is able to compensate this. So, remember our overall brain criteria is around 10 to the power of 3, 2 to the power of 4 and therefore, what you are expecting is this gm ro whole square factor is going to give this something around 10 to the power of 4. And hence the a parasitic capacitance ratio that ratio of this capacitances at this point

the cl the cc that will put for compensation versus this capacitance should be of that order gm ro.

Because what we want is the dominant pole should be gm ro whole square times smaller than the second pole. And here we have the impedance which is gm ro times the impedance at this point and hence the other option that you make the capacitance gm ro times larger at this point as compared to this point. The target is to make the capacitance over here gm ro times larger as compared to the capacitance at this point that is what we discussed yesterday while discussing the stability. And in that case if I my gm ro is expected to be around 100 I would like this capacitance to be 100 times larger than this, and in order to make sure that that happens and I do not have to put a big capacitance over here I should also like to limit I would also like to limit the total parasitic capacitance over here. And for that I need to be carefully see these transistor is going to dominate the total capacitance at that point.

So, towards that end we can see the overall contribution of the capacitances coming at this point. Because ultimately it is going to play an important role in compensation of both the loops the differential loop as well as the common mode loop. So, we can just look at the overall parasitic capacitances at this point in the common mode loop. For the common mode loop we can see there is definitely going to be a effective mirror multiplication between the gate and the drain of this particular MOSFET, the gain factor is sufficiently strong it is gm ro therefore, this can introduce a significant capacitance at this node right.

So, at least for the common mode feedback loop what we can see is it is going to introduce a sufficient mirror multiplication. The other transistors gate is AC ground here also gate is AC ground. So, if I look at the parasitic capacitance component I was just try to draw and understand which one is going to be the dominant one the cgd of this MOSFET gate drain gate is grounded therefore, the cgd of this MOSFET is going to appear as it is if I look at say the cgs or cs a cgs of the second MOSFET over here let me just copy the numbers once again this was 2 3 4 and 5. So, this is basically c g d of 5, which is experiencing a miller multiplication on the factor gm ro this capacitance; however, if I see this is gm this is just cgs of the m 4. So, I can call the cgs 4 is going to

appear as it is, likewise the c g d 1 is going to appear as it is because this also appear between this particular point an AC ground.

And on the other side also you have some parasitic capacitances coming from this side. So, in this particular amplifier we have the cgd of this MOSFET, I can name this say 7 8 cgd 8 and 9 10. So, you have the cs, cgs just for the sake of completeness I can put these also. So, the cgs of m 9 also appear between this point and AC ground because if you look at the contribution of m 9. The gate and drain are shorted. So, at this point you have the cgs 9 also coming into picture. So, I have cgs 9. So, we have just drawn the parasitic capacitances corresponding to the different transistor that are contributing at this node remember this point is disconnected. So, you do not have a connection between this 2 node.

Therefore that capacitance contribution is going to come from the m 9, and the cgd of this transistor. I am ignoring for the time being the cgs cdb and csp component assuming that they are relatively smaller otherwise the picture will become more messed up. So, assuming that the cdb and cfb components are ignored for the time being I am considering only the cgd and cgs. So, in general that is true because the cgd component the cgs component can be the dominant one the junction capacitance can be literally smaller that you see between the c d b and csb and moreover they do not under a miller multiplication as such. So, this can go miller multiplication it is important to consider this cgs is the largest one in magnitude. So, it is important to consider this these 2 are it can be smaller than even the cgd. Therefore, I am not considering those 2 in order to complete this we will again come back and complete this discussion.