Analog Circuits and Systems through SPICE Simulation
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Lecture – 55
Folded Cascode Biasing

Welcome back, let us continue our discussion on the cascode amplifier. And we are going to look into the folding cascode configuration which can help us in achieving better signal swing at the input node. And also a facilitate better biasing for the overall amplifier.

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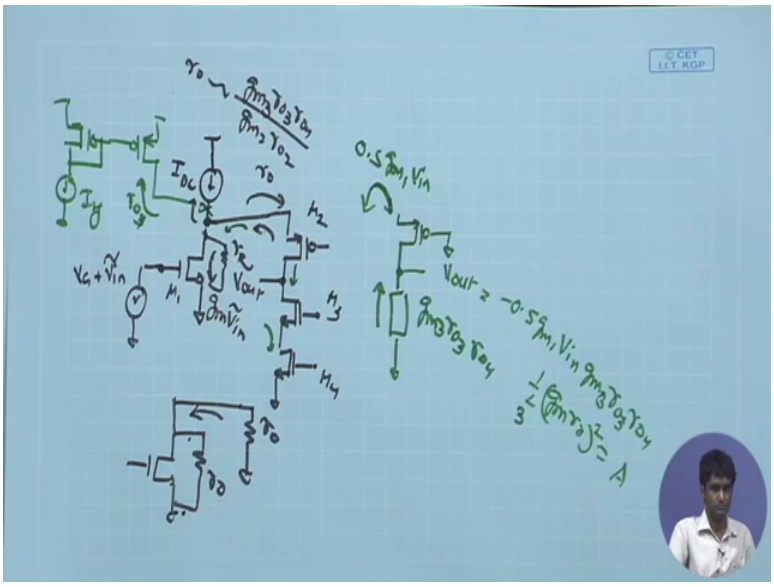

So the basic operation involved in the folded cascoded is you can start with the ideal current source, where our input device is the NMOS and you are having the cascode operation being provided by PMOS device and then you have another NMOS load. This is a single ended cascode we were looking into the differential version of that also. But it is important to look at the functionality here once we are comfortable with this we can go for a differential version.

So, here you have some input signal which is some gate bias plus the AC signal V in, and we are looking at the output voltage over here V out. And we to look at the overall signal gain from here to here what is happening in the overall signal propagation from the input point to the output point. These are again some gate bias voltages, if I call this m 1 this is

m 2 m 3 and m 4 with certain gate bias voltages. And now if I look at the overall operation if I assume that this is a DC bias current and which is an ideal current. The current the small signal current provided by m 1 this is gm 1 V in right. This is the small signal current provided by m 1 if you are applying an AC signal at the gate of m 1.

If this is an ideal current source the small signal impedance of the IDC is very large infinite ideally. And therefore, this entire small signal current will be flowing into this direction right. So, the entire gm 1 times being flows here because for the AC analysis this ideal current source is going to be open circuit it is not going to have any small signal current flowing. As a result this entire gm 1 V in goes in. What is m 2 doing over here? If I forget about the first part of the circuit m 2 is acting like the a common gate circuit where the input signal is at the source gate is at AC ground as a potential fixed potential. And therefore, whatever small signal current flows into the source of m 2 will be injected at the drain of m 2. And whatever impedance it sees over here at the drain that current will be multiplied by that impedance and give you a voltage, that what we have study for the cascode stage.

So, if I look at the situation of m 2 it is having some small signal resistance contained in the drain, what is that impedance?

Student: (Refer Time: 03:13).

This is m 2 with gate AC ground you are having some signal which is gm 1 times V in. And it is having a large impedance given by the impedance looking into the drain of m 3 which is gm 3 ro 3 times ro 4 right. The impedance looking into the drain of cascode device it is going to be gm 3 ro 3 times ro 4. And as a result whatever signal comes seen over here. So, if I draw the draw the directions correctly the gm 1 V in is from the drain to source. So, the gm 1 V in direction is this. And as a result the same current whatever current enters into the source of m 3 should be coming out of the drain of m 3 and as a result I will be this current will be getting are divided by this factor. One factor that I you know missed was the ro of the m 1 itself. So, you know that you have also have a ro of m 1 over here right and looking into the direction of the source of m 2 what is impedance? Ro we have discussed right.

So, that will be given by this large impedance gm 3 ro 3 ro 4 divided by gm 2 ro 2. So, impedance looking into the source is equal to the drain impedance divided by the

intrinsic gain which is gm 2 ro 2. So, this is going to be of the order of ro. So, impedance looking into the source of m 2 is also ro. And for this m 1 therefore, the scenario is that the m 1 itself is having it is small signal ro from drain to AC ground because the ro p between drain and AC ground drain and source is at AC ground. And the DC current is anyway op amp. So, it does not give you the ideal. So, this does not give you any impedance that is infinite.

And then you are having the overall impedance looking into the source of m 2 which is also ro. So, whatever gm V GS is produced by this MOSFET, half of that only goes into the ro which is looking into the source of m 2. Therefore, I have this 0.5 factor coming over here. And as a result the V out can be given as minus 0.5 gm 1 V in times this gm 3 ro 3 ro 4. And of course, we are having an overall gain of 1 upon 2 gm ro square, this is your gain. This is again giving the same functionality same behavior as our normal stacked cascode amplifier that we saw. Only difference is that we have applied input signal to the gate of NMOS and greater than sending the current into the stack of cascode of NMOS and stacked PMOS load we have folded the current the small signal current have been folded down.

And now it is going to the stack of the NMOS cascode load and a PMOS cascode device this is a cascode transistor this is a PMOS cascode device and you are having a cascode load. So, the small signal current have been folded down therefore, we term this as the folded cascode. And of course, we can look at the overall DC potential over here, now if I replace this by a non ideal current source then we can talk about the DC biasing point over here and a signal swing over here. So, let us replace this by the by an non ideal current source and then look at the modified gain and then the signal swing at the output point at the input point.

So, what is the difference in the signal analysis if I replace it by an ideal sorry are a non ideal current source realize with the help of just simple PMOS transistor. Suppose to supply some fixed current. So, I can realize it with the help of a PMOS transistor and this is in turned bias with some reference branch that we can construct right. So, is there any difference we are going to encounter in the resulting small signal analysis, what stage you are going to have the difference? So, we can see that this is going to give you another impedance ro 3 sorry, ro whatever number. So, here you have an ro looking into the drain of this PMOS, and now you have another ro over here and ro of the m 1 also.

Therefore, only one third of that small signal current goes out and therefore, you are going to have one third factor coming over here.

So, this basically gives us the overall modified gain because of the folded cascode with a non ideal current source. Now once we have this we can also look at the other factors like the signal swing DC bias conditions and all. So, let us do that in a fresh diagram any questions before you proceed and look at that DC biasing signal swing. Bandwidth point of view or frequency response under view again we have similar scenario even if you have this configuration the overall amplifier is where going to have this one as the critical or the high impedance node, because if you look at the impedance over here once again it is going to be the impedance looking upward r up are r down r down is still gm ro square gm times ro square r up what is r up. So, only difference is that in the source of m 2 rather than having ro not you have ro by 2 and therefore, the impedance will be gm ro of m 2 times ro by 2 order is similar gm ro square by 2.

So, therefore, you are going to have similar magnitude of the small signal resistance over here. And hence the pole magnitude also remains similar and other points you still have impedance is given by close to ro by 2. So, at this point you have ro of this MOSFET ro here and the ro of the PMOS m 2, as a result you having ro by 3 over here also you are having similar values. So, at these 2 points once again your non dominant poles and the output point you have a dominant pole. So, from the point of view of frequency response the behavior remains more or less similar. Is it clear? The small signal analysis and frequency response. Any question before we look into the signal swing once again?

Student: Sir where we need the drain voltage of first NMOS also is defined (Refer Time: 09:46)

So.

Student: Voltage of first NMOS.

Drain voltage yes so.

Student: because it is going to PMOS source. So, how means (Refer Time: 09:59) if it is small length there will be problem.

No that has to be defined properly. So, of course, you know it has to be sufficiently high So that we are able to directly connect to the PMOS source. Any other question? We will see that how are you going to do that.

So, let us look at the signal swing with the real current source that we have.

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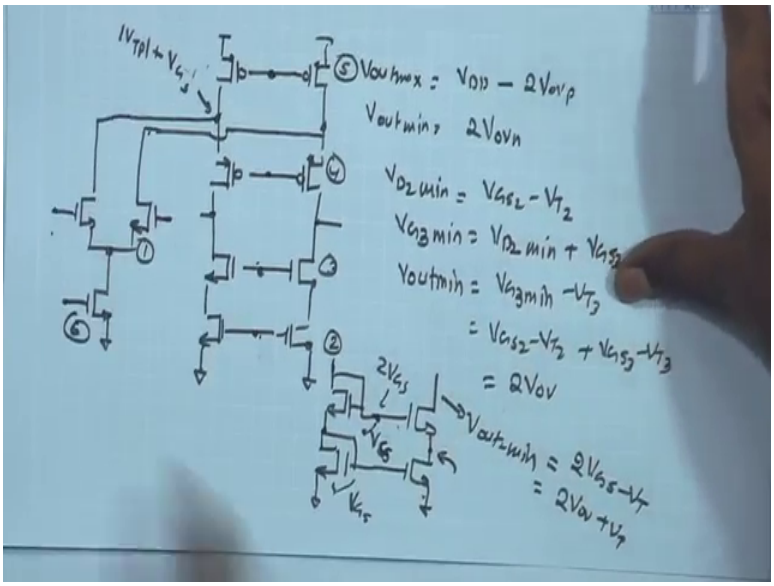

I am not discussing how we are biasing this source suppose it will bias a and at the input side you are having the it will be prudent to directly go to the differential topology. So, rather than going for the DC analysis here since we are going to ultimately will be the DC analysis of our differential scheme. So, let us go for the differential (Refer Time: 10:45) write ahead because all the DC biasing and the signal analysis that we have to do ultimately it is more meaningful to do it for the differential scheme, because we do not use this kind of single ended amplifiers anywhere in our circuits integrated circuits.

So, let us apply the same scheme for the differential operation and apply at the arrive at the full rate cascode differential amplifier. So, if I do that I can as I just mentioned here I can implement this current source using the PMOS transistor over here, and this stack remains as it is only thing is will be differential you have the 2 pairs coming. So, let us do that. So, the time being I am not discussing how these will be biased I will arrive at that very soon. So, this is the overall differential scheme that. You have assumed that these are appropriately DC appropriate DC biases. And this is again till current source for the differential pair and if I look at the similarity between the single ended one and the

corresponding differential topology once again if I look at the differential half circuit. So, this becomes AC ground as a result this is your m 1 the current source over here is being realized with the help of the PMOS over here. And then you have the other PMOS and 2 NMOS in stack coming over here.

So, the differential half circuit will be exactly same as what we just discussed. Is it clear? No issues with the translation 2, the fully diff the differential topology? Now right now I am drawing it as a fully differential topology I can also convert it into a differential to single ended version. So, we look at the 2 schemes. So, so far we have been discussing the differential fully differential topologies let us stick to differential one and then it will also discuss briefly the single ended output 1. So, in those cases how does the signal swing is setup change or how does the biasing scheme change that will discuss briefly, but let us stick to the for the differential.

So, here once again the output points are over here, and we can look at the output common mode level that is required for maximum symmetric swing. So, this is now symmetric on the upper side in the lower side. So, the stack is symmetric for PMOS and NMOS. So, you do not have a tail current source over here. And therefore, as per our earlier analysis we can and conclude that the maximum and minimum output voltage that you can have is going to be V DD minus 2 V overdrive on this side lower side you can have 2 V overdrive. And therefore, the V out max is V DD minus 2 V overdrive, you can call it V overdrive p is assuming to be close to V overdrive of n also. And we out mean is 2 V overdrive and again if you want to verify you can just trace from the bottom most level. So, the voltage over here is going to be the V GS of the MOSFET. So, if I say call this the m 1 m 2 well let me call this 1. So, both together are 1 and this is together you know 2 3 4 and 5 this one 6. So, I am just numbering the pairs.

So, here if I look at the bottom most level. So, you are having some V GS 2. V GS 2 the minimum allowed potential at the drain that you can have V D 2 V D 2 min is V GS 2 minus V T 2. And corresponding to that you have a minimum allowed gate voltage at g 3. So, V G 3 min is equal to V D 2 min plus V GS 3. And as a result output V out min is going to be V G 3 min minus V T 3, and hence this is nothing else, but V GS 2 minus V T 2 plus V GS 3 minus V T 3 hence is equal to 2 V overdrive. This is the best you can have minimum allowed potential provided the V G 3 is also equal to V G 3 min. And the source potential of m 2 is also equal to the V D 2 min, but if you achieve that then you

can have the maximum minimum allowed potential at the output equal to 2, V overdrive likewise of the upper side you can have V DD minus 2 V overdrive and the verify that by tracking it from the top most level coming to this point.

So, for a given V G 5 you will have V G plus mod V T correspond with that the maximum value we can have over here is V G minus plus mod V TP minus V sg again minus V G plus mod V TP. So, again you will get the same expression. So, from the output side we have this particular scheme.

And we are trying to go to have a we are going to have a bias which is going to help us in achieving this maximum and minimum voltage level that is one target for this design. And now we can also look at the input side. So, input side this is similar to our differential amplifier with current source load. So, you are having input pair and the drain side is connected to PMOS and therefore, the limitation on the input common mode range or the input signal level is input common mode level is mitigated. Because here the output DC point can be pretty high the maximum value that you can have over here is V GB plus small V TP in order to get maximum possible swing at this node you would like to push this DC point to maximum possible value which is going to be V G 5 V G 5 plus mod V TP right. And as a result the maximum value that you can here have over here is going to be V G 5 plus mod V TP plus mod V TP which is which can be pretty large. And as a result the limitation on input common mode range on the upper side that we had in the original design in the original example it has been mitigated it can go to a much larger value lower side. You have similar case the lower side. You can go to the minimum value that you can have is V G minus V T plus V GS.

So, lower side similar, but the severe constraint was coming on the upper side because you had 3 stacks on the top of that that has been mitigated. Now I can go to a much larger value on the upper side. So, as a result I can have a feedback operation where the input common mode range can vary a lot and if you are having you are for example, going for the direct DC biasing of the input from the output that is also very much feasible over here. Because even if you put this V DD by 2 it is not going to be severely you know it is very much acceptable even if you having V DD by 2 over here it is not severely affecting my output common voltage right.

So, the input DC level is not directly link to the output common mode output common mode value or the output DC point or the output range. So, these 2 are getting decoupled. So, V DD by 2 over here does not necessarily have any influence on the DC point here. In the previous case we saw that if you are putting a DC point V DD by you are trying to put up V DD by 2 over here one volt over here.

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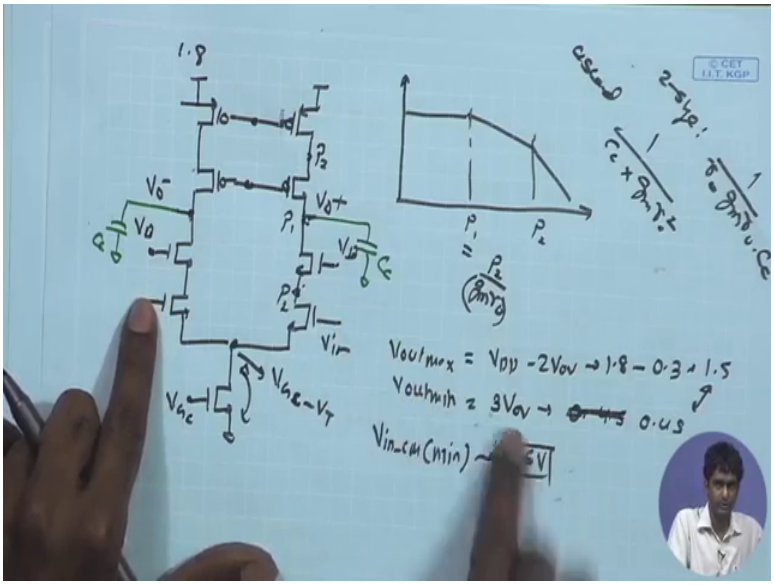

Then it was you know violating my minimum allowed same voltage level over here which was point 6 volt, but here that is on the case I can allow I can have a input DC point which is not conflicting with my output common mode level.

So, now any question is looking at the overall signal overall biasing scheme for the differential operation and looking at the biasing for the input side as well looking at the biasing of these individual mirrors. So, for that we need to look at the biasing scheme which can help us in generating minimum load potential for the gate voltage of the m 3, for a given biasing point for the gate voltage of m 2. So, we have discussed one simpler scheme what we have seen here is that one of the very simplest scheme can be to use a cascode mirror just like we do it for a simple current mirror we can use a cascode mirror. And you can put a reference current in the cascode branch and that is going to develop V GS over here another V GS over here sorry, V GS over here. And that is going to provide the right V GS for this to MOSFET. That is basically our simple cascode mirror where

one side you are having a staggered diode (Refer Time: 20:22) transistor and that is giving you an appropriate value of V GS to bias these transistors.

So, I can imagine that I have a reference current getting injected into a direct connected branch like this, and I have the gate voltage is developed over here I can put it over here I can bias the stack of the NMOS using this scheme. Likewise for the PMOS I can have a similar you know DC bias and you have a PMOS diode current sorry your PMOS cascode current mirror and with the help of that I can generate the base points over here that is very much possible. But here we have also seen that this particular scheme does not give me the minimum allowed DC potential over here. Because this is if this is V GS the DC point over here is also V GS and as a result the DC potential at the gate of this MOSFET you are getting is 2 V GS. And the minimum allow DC potential that we had was V GS minus V T plus V GS. So, it is basically 2 V GS minus V T, but now it is 2 V GS and therefore, the minimal out potential here can be 2 V GS minus V T. So, here the V out mean in this case if I use this kind of biasing it can be at the max at the min 2 V GS minus V T, which is basically 2 V overdrive plus V T because V overdrive is really V T V GS minus V T.

So, I have V T higher V the V out mean is larger by V T and V T can a produce significant 0.3, 0.4 volt and hence the V out min has been increased by that value. Therefore, this is definitely not the best case I need to look for alternates schemes where I can intentionally force this node to the minimum possible value which is going to be V G minus V T. So, this is in this particular configuration, but is this particular potential I can expect? If this is 2 V GS and you are having same current in these 2 branches I would expect this potential to be close to V GS minus V GS. So, there is also V GS. So, it is not really the minimum value, which is V GS minus V T this is V GS this is also V GS.

So, is it unnecessary based in some voltage headroom? I can afford a significantly smaller voltage over here. Right now it is V GS because of the stag MOSFET 2 PMOS wire connections. This is V GS this is V GS as a result this 2 V GS and as a result if these 2 are matched is they are identical having the same current this will also have gate potential minus V GS. And therefore, this is going to be same as V GS whereas, the minimum potential that can have here is V GS minus V T. So, I would like to have a

biasing scheme which can let me have that minimum allowed potential which is V G minus V T.

So, let us see one possible scheme to do that.

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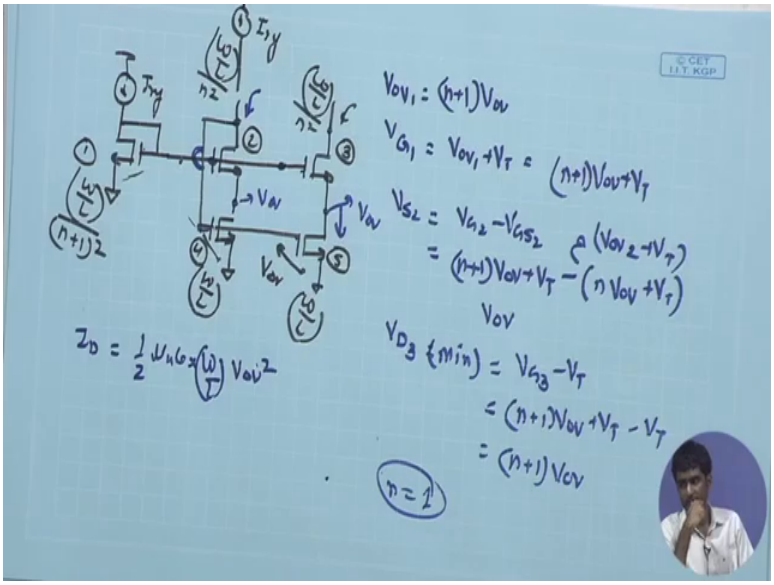

You call this if m 1 m 2 3 4 and 5, any question before we proceed further you can you can let me know before we can go for the alternate biasing scheme? Right so, here assume that these devices have W by L ratio W by L and here this one is having W by L upon n plus 1 square where anyone integer. So, this W by L ratio is W by L upon n plus 1 square, if these 2 4 and 5 are in W by L W by L this is W by L upon n plus 1 square. These 2 are having W by L upon n square, this is also having W by L upon n square. So, this is the biasing condition of arrived at. So, you have W by L W by L W by L upon n square W by L upon n square. And here you have W by L upon n plus 1 square. And as a result I have I have to look at the require I have to look at the DC gate voltage generated over here with respect to the reference current and also look at the DC potentials at these 2 points. And figure out that this is my output branch this is my branch will bias with respect to these potentials what is the minimum allowed potential over here.

So, what I am assuming is this 3 and 5 is like my transistor over here, this is 3 and 5 assume that I am trying to generate an appropriate value of gate voltage for biasing transistors stack or 3 2 over here. So, this is my output device I am trying to find an appropriate gate potential for these 2 devices. Now if I look at the V overdrive let me

look at the V overdrive of this guy I I can call this let it be V overdrive. And enforcing same current in this. So, assume that this branch is also having the same current I rf that is easy to do I can just mirror the same current into this, and same current over here. So, these 2 branches are having same current. And if I say that this m 4 and m 5 is having V overdrive that is V GS minus V T of m 4 and m 5 is V overdrive, what should be the V overdrive of this? What is the V overdrive 1? V overdrive 1 this is going to be n plus 1 times V overdrive because I D is the V overdrive proportional to be V overdrive square. And times W by L and therefore, here you having n plus 1 square. So, id is 1 upon 2 nu n cox W by L which we are changing by factor of n plus 1 square and then V overdrive square.

So, here if I have a ratio of W by L n plus 1 square, the V overdrive will have ratio of n plus 1. Therefore, the V overdrive of one is going to be n plus 1 times V overdrive of these devices. And therefore, what is the V G, 1? V G 1 is V overdrive plus V T because V overdrive is V GS 1 minus V T s is 0 therefore, V G one is going to be V overdrive 1 plus V T. So, V overdrive 1 plus V T, which is n plus 1 V overdrive plus V T right. And that is the same gate voltage is applied at the gate of m 2 as well as m 3. Therefore, now what is the source if I assume you have the same current flowing through m 2 what is the source potential of m 2? Vs 2? This is going to be V G 2 minus V GS 2 right. So, basically V G 2 which is same as n plus 1 V overdrive plus V T, minus V GS 2 what is V GS 2? V GS 2 is once again I can write it down as the V overdrive 2 plus V T what is V over drive 2? It is having W by L upon n squared will be n V overdrive n V overdrive plus V T right. V GS is V overdrive plus V T for MOSFET and the V GS 2 is having W by L ratio which is 1 upon n square another result I can write the V GS 2 as n times V overdrive plus V T this is basically same as V overdrive 2 plus V T 2, I am assuming all the V T s are same.

So, I can see that you will get the n V overdrive cancel V T cancel you are just left with the V overdrive. So, the source potential of m 2 you are forcing it to V overdrive. So, this is now V overdrive. And if I now look at the gate potential of m 3 and source potential of m 3. Now m 4 and m 5 are having same gate potentials therefore, it will try to enforce the same current in the m 5 V GS of m 4. And V GS of m 5 is same it will try to in for the same current in m 5 the gate potential of m 3 is same as gate potential of m 2 and therefore, it will try to enforce the similar V GS if m 5 is time 2 enforce the same current

that will enforce the same V GS for m 3 as m 2 because their gate potentials are same m 5 is force to carry the same current as m 4 because their gate potentials gate to source potentials are same. And as a result you are having the V GS of m 3 going to copy the V GS of m 2 therefore, this potential is also going to be V overdrive therefore, we wanted we wanted that the DC potential at this point should be close to the minimum potential which is basically V overdrive. That is achieve in this scheme.

Now, what about the drain potential of m 3? So, V D 3 in this if we see minimum V D 3 min if I want to say V D 3 min what is the V D 3 min I can have under this condition that is going to be V G 3 minus V T. What is V G 3? That is same as the V G of this device m 1 which is basically n plus 1 V over drive plus V T minus V T. Therefore, you are having n plus 1 V overdrive. So, V D 3 min you can have n plus 1 V overdrive. So, what should be the n to get the desired minimum output swing that we wanted? One So that you know you have the minimum output potential possible equal to 2 V overdrive.

If I put n equal to one I can ensure that the minimum over all potential at this mirror is 2 V overdrive. And that would mean the W by L of these 2 transistors are same and here you have just 4 times 1 upon 4 W by L of this transistor. You are enforcing I rf here I rf here and with the help of that you are generating or biasing the gate potentials over here with that current, is it clear?

So.

Student: (Refer Time: 31:00) gate of n 4 is connected with the, so it is.

M 4 is connected to the drain of m 2. Here you do not have any connection this is not connection not anything. So, here this gate this gate this gate are connected. This you can say the jumper over here, just to make it clear there is no connection in this line. So, this is the gate of m 4 connected directly to the drain of m 2. Can you tell me what is the small signal if I ask you to find out the small signal impedance looking into this node what is it? If there is a question that we get find out the small signal impedance looking into this.

Student: (Refer Time: 31:46).

Why?

Student: because you controlling the (Refer Time: 31:49).

Anybody else? Every call it along response, anybody else?

Student: (Refer Time: 32:08).

Why?

Student: (Refer Time: 32:13).

Yes tell me.

Student: (Refer Time: 32:17).

Now if you if you increase if you put a test voltage over here. And you increase that what is going to happen V GS is going to change? And that is therefore, the small signal current will be gm V GS therefore, you are going to have the current change corresponding to 1 upon gm. So, in this branch is going to have impedance very low 1 upon gm he is this branch same, whatever it is just discuss that devices gate constant gate a different DC potential constant therefore, this is good to have high impedance gm ro square. And that is going to be applied here in our you know, cascode circuits this 2 can be you know bias with help of the scheme still have large impedance. Is it clear? Any question?

So, let us see, but how can incorporate this in our cascode amplifier to complete the biasing.

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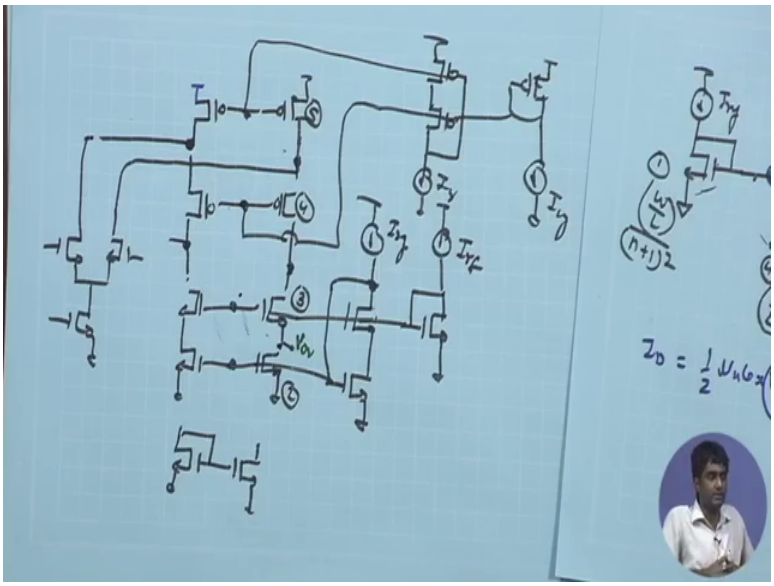

Student: (Refer Time: 33:13).

So, the NMOS part is more or less there we can use the biasing scheme that we just discussed, you have this part in. So, for the NMOS we have just discussed the biasing scheme where I need to use the cascode device to get the biasing. I can go ahead and have the reference branch being injected with the I rf, the same current coming here with the help of a mirror and I am producing the gate voltages for this 2 PMOS. So, I can set these 2 to the required values and therefore, I am going to get minimum allowed tension over here.

So, the minimum lower side it is serving the purpose I am going to get the minimum allowing V G over here the minimum allowed source potential for this transistor over here if I follow the convention I had 2 this is 3 and this is 4 and this is 5. So, lower side the scheme takes care of my minimum allowed potential. So, this is allowing me to have the DC potential over here close to let me use this V overdrive. And this is this DC potential is going to be close to be V overdrive, and minimum potential over here is going to be 2 V overdrive. I can allowed, I allowed to have minimum potential over here equal to 2 V overdrive that is what we have see in this particular scheme. On the upper side also I would like to bias it using a similar scheme.

So, this 2 PMOS is also carrying an a similar current. So, I can construct another mirrors or biasing this PMOS as well. So, again imagine that I can have the similar structure for

the PMOS. I can have PMOS reference branch which is basically supplied the same current I rf. So, whenever using I rf of first we can mirror it we do not need to have. So, many reference current one reference current will be there and mirror at all these different points. And then I can have a PMOS very early which is going to be taking the bias voltage here and another PMOS which is connected over here. And I have to enforces same I rf over here, and I can possibly use this gate voltage of the PMOS generated over here to possibly bias this is one possibility. Can I use this gate voltage to bias this? 2 reasons means forget about common mode feedback suppose you know we have common mode feedback and everything even in that case about output DC potential is controlled can we used this biases directly assuming the ratio that we just figure out.

Any issue that we can see here? Remember, here when we looked at the overall scheme we discussed we assumed that the current in these 3 branches are almost similar and therefore, we are having certain ratio over here. But if you look at the current here. So, I can assume that the current here and here is similar and as a result the current here I am trying to make it similar. But the current in this device is not same because current is this device supplying the current over here and also the current over here. So, the current in this 2 PMOS devices they are not same as the current in this once. So, I cannot directly you know connect it over here and say that my overall biasing condition is made. Because the current matching is not satisfied as we used it for the NMOS case.

So, we need to do something else and apart from that another serious issue is the common mode feedback that we also need to account for. So, I must make sure that the output common mode level over here. That is close to the desired value. And for that once again I need to apply a common mode feedback for the fully differential case and make sure that we are able to control certain means one of these transistors in the stack So that the output common mode DC level is achieved. So, that will require you know additional discussion. If out of if we want to say construct a single ended version. Single ended version means just like your differential amplifier with diode connected load it has a single ended output. So, if you want to do that what modification can be done in the lower part.

So, rather than taking this as the you know as the load branch, I can use this diode connected this is effectively diode connected as I said the impedance looking into this one is you know 1 upon gm. Because if you are changing the voltage over here trying to

see what is the impedance over here changing the voltage over here by a small amount is changes the V GS of this MOSFET. And therefore, the current is going to be gm V GS and therefore, this is acting like a diode connected branch. So, I can replace one of these size by the diode connected branch and another one remains as it is. So, this will be something similar to or analogous to our you know current mirror load.

So, if I replay if I place this here and keep this as it is it becomes a cascode kind of current mirror load right. So, that you are having on one side output impedance given by the gm ro square. And on the other side is just 1 upon gm and then we have we are going to get a functionality which is close to our current mirror load differential amplifier. So, we will discuss that in more detail that that leads to our differential input, but single any output cascode. But if you are going for fully differential cascode then we need to use a different biasing scheme we need to first of all bias the load transistors and at the same time we need to take care of the common mode feedback to stabilize the DC bias point for the overall output.

So, let us discuss that in the next module before that, any other question related to whatever we have discussed So far? So, biasing is not complete ready to the both the schemes for the differential input single ended output and the fully differential scheme which is going to require common mode feedback. We are going to discuss both of that and for the common mode feedback once again a little bit of discussion on common mode feedbacks loop stability. Will be coming into picture and in this case it will be relatively simpler, because you are having self cast self compensation present in this amplifier.

So, once again both the common mode and differential loop will be satisfied with the same dominant pole. So, here that advantage basically is missing that you can separate out the differential common mode loops. So, here is because you have a single dominant pole you will end up compensating both the loops by the help of this dominant pole. But still we need to figure out the common mode feedback configuration the configuration of the error amplifier where to apply the input where to apply the error amplifier output and so on. So, any questions in whatever related whatever we have discussed So far?

Student: (Refer Time: 41:45).

So, starting from the biasing the current mirror and how we are applying it to the bias the bottom 2 transistors, any anything any part which is not clear especially in this biasing?

Student: (Refer Time: 42:11).

Because it is having a difference current. So, this current is not seen as you know current in this branch. So, here we assume that the current ratios are different. So, you can W by L different size and accordingly you can do it, but another factor that major factor that I told is the common mode feedback. So, you need to take care of the common mode feedback.

So, probably you can still use this you are still bias this PMOS with the help of this, but then you need to have at least one port where the commode feedback will be coming. And this can be one port over here. So, I can I probably like to control this one with the help of common mode feedback, I can apply common feedback in other ways also I can also control this 2 by common mode feedback and control these tutoring through a current mirror biasing that like did here. So, I can do either way I can either control both these using common mode feedback or both these using common mode feedback or one of these using common mode feedback all those possibilities are there, but at least one point I have to leave for common mode feedback if I am using a fully differential scheme.

Student: Sir input a input a current and output branch current as same or (Refer Time: 43:21).

They can be different, because important point is that here you need to have a good gm and the ro is over here. So, in order to get good gm or in order to get good noise performance I can afford to have a larger current here. That is not degrading my ro that significantly, it will affect ro because if the large is there is a larger current over here this will degrade the ro of this definitely, but you also have a gm ro square factor over here. Therefore, I can try to reduce the bias current in this stage, but retain a sufficient bias current over here So that my gm of the first stage is good, W by L as well as bias current is good, So that gm is large and at the same time in this stage I can reduce of bias current. So, that the ro over here is large.

Student: (Refer Time: 44:12) having gain (Refer Time: 44:14) there only.

They are coming right. So, overall you whatever your gm ro square product is coming ro r up parallel r down. If you will reduce the ro of this ultimately the gm ro times ro that comes to determine the output impedance that is going to be affected.

Student: (Refer Time: 44:31) NMOS can be PMOS.

Both the ros are contributing this ro as well this ro.

Student: (Refer Time: 44:37).

If you lower both of them ultimately it will affect your gain also noise consideration again becomes important, because noise point of you will see the just like our earlier case, the noise in forces larger gm at the input device. And you know the gm of the second stage devices are not important. So, they are the gm 1 upon gm ratios over here gm 1 comes in the you know the overall noise input referred noise the gm 1 of the input pair comes in the denominator all others in the numerator. So, would like to have a larger gm over here as compared to the stage and output the output transistor. Any other question?

Student: (Refer Time: 45:22).

So we can stop here. And in the next model you can take up the rest of analysis and complete the DC biasing, and common mode feedback.