Analog Circuits and Systems through SPICE Simulation
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Lecture - 54
Folded Cascode

Welcome back; let us resume our discussion on Cascode Amplifier; that we started last day.

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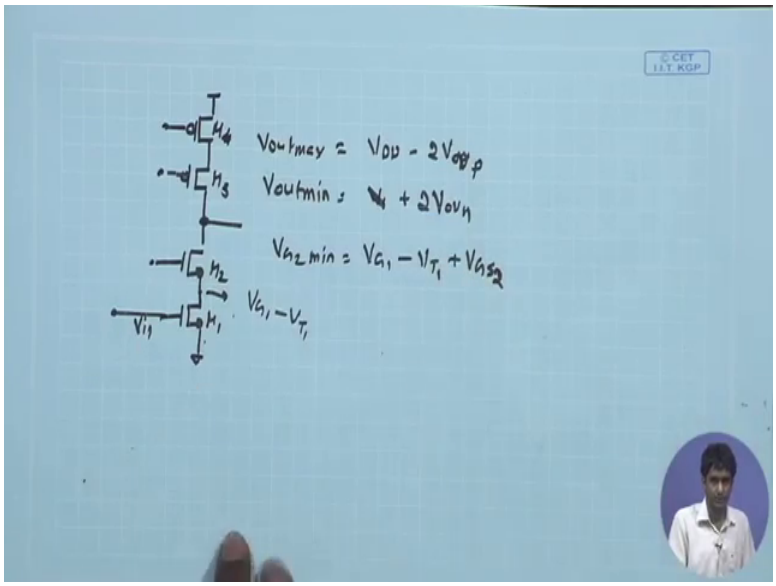

So, we have looked into single stage, single ended cascode amplifier where the input single is applied at the gate of M 1 and the output is taking at the drain of M 3 and M 2. You have some appropriate bias point over here, we also saw one easy way of biasing the gate of M 4 and M 3, so that you can get an appropriate signal swing over here. And we also analyzed the output signal swing, what is the maximum and minimum output signal swing. In order to arrive at this before that we looked into the small signal impedances; looked into the drain and source of the mosfet under different loading conditions and we derived expression for that, which was useful in understanding the operation of this cascode amplifier.

And what we concluded the basic conclusion out of this was that in single stage, we are able to get the gain GM; RO whole square; which is comparable to the gain of the two stage op amp that we used open loop gain of the two stage of that we get.

We also know looked at the poles; so, the here we saw that the output pole is going to be the dominant one; because here the impedance is GM; RO square; GM times RO squared, which is much higher than RO. As a result, this becomes the dominant pole other two are having an impedance just given by RO.

So, as compared to the two stage amplifier, where the two poles P 1, P 2 are comparable. Here we have a dominant pole; one of them is already dominant and it is having value GM; RO times lower as compared to the other one; if I just depend upon the parasitic capacitances. And therefore, if I have to compensate the closed loop operation involving such amplifiers; I would like to just compensate this dominant pole; I would like to just push it towards further lower frequency and obtain a overall field margin of 45 degree.

So, that is one of the advantage of this stage; you are having self compensation. One of the poles is already dominant and you want to just push it by another significant factors that it goes down. You are getting a larger gain, the overall gain is comparable to the two stage. The disadvantages as we discussed was the swing; the input as well as output single swing will be limited.

So, output point of view we saw that the best that we can do is to get overall swing of Vdd minus 4 V over drive; that is the overall pick to pick (Refer Time: 02:59) and get because what we saw is that the maximum side V out max that you can have; assuming that this gate voltages are in our hand and you can set them. So, V out max that we arrived at was equal to Vdd minus and V out min that we can have is simply 2 V over drive of n mos. So, this is the minimum and maximum output level that you can have provided I have the freedom to control the gate voltages.

Therefore, if I look at the overall swing that you have V out max minus V out min; we have Vo; Vdd minus four V over drive and V over drive depending on the bias current, it can be few tens of millivolt, 200 millivolt in this application. Specially, if you are trying to get better gain then that case we would rise; can be reduced by having a lower bias current and having a larger W by l. And once again there is going to trade off with other parameters like the bandwidth; we will see that the V over drive is also having a strong trade off with noise. So, when we do the noise analysis for the cascode amplifier; we will see that it is also going to have a significant an important trade off with noise of the cascode stage.

So, we looked at simple biasing scheme where we bias the P mos stage with the help of current mirrors; a cascode current mirror. Likewise, we look at the biasing of the gate of the M 2 also; so, that was not the best case; the best case would be to have the DC bias point the gate of M 2; which is lowest possible. Likewise, have the gate voltages of M three and M four which are highest possible.

Because if I keep the gate voltage of M 3 and M 4 highest possible, then I can get the maximum possible output swing over here, the output V out max can be highest possible. Likewise, if I keep the DC volt bias voltages at the gate of M 2 to the lowest possible value I can get the V out min to the lowest possible value.

So, in order to minimize the V out min; I would like to keep the gate voltage of M 2 to the lowest possible and I would also like to keep the gate voltages of M 3 to the highest possible value; so as to maximize V out max. That was a summary of the discussion that we had last day on signal swing. So, just to recall the V G 2 min; that I can have is going to be V G 1; the DC bias at the gate of M 1 minus V T of M 1; that is basically the minimum drain potential that you can have at the drain of M 1 and hence the potential at the source of M 1; that plus V G S, I am assuming V G S is same for all provided W by L are same. To be clear, I can just started plus V G S 2 and likewise I can determine the maximum gate potential for the M 3 (Refer Time: 05:54) or allowed.

Now, once I have this V G 2 min that would imply that the potential over here is V G 1 minus V T. So, if I force this DC potential equal to V G 1; minus V T 1 plus V G S 2; then I am assuming that the potential over here is the minimum allowed potential of the drain of M 1, which is V G 1 minus V T 1. And the assumption there is that signal swing over is much smaller, even over here if it is close to 1 volt; here it is going to 1 upon 100; so, 10 milivolt are smaller than that.

Therefore, the swing is not a major constrain; even if this is bias at the edge of the triode region; that means, the DC potential over here is equal to V G 1 minus V T; edge of saturation, below that it can intend to triode. So, still I am happy with that because assuming the signal swing over here is very small and is not going to push this in triode; signal here is weak. So, this is the minimum drain potential that I can have for M 1 and then corresponding to that; I can see what is the signal swing that I am allowed to have.

Now, signal swing over here of course, depends upon the overall signal swing over here in the open loop case. So, I am just using this amplifier in the open loop; I do not worry about signal swing because the signal swing over here will be; dictated by the maximum signal swing over here divided by the gain. Maximum signal swing is you know maybe 1 volt, for 1.8 volt supply. Suppose, we are able to get a one volt which is not very difficult to obtain and that divided by the overall gain GM; RO whole square by 2 which is pretty large, it can be you know several thousands

As a result, the input signal swing that you are allowed to have possibly millivolt or lower than that. So, that is the allowed; this is how I can find out the allowed input peak to peak swing, maximum output swing divided by the overall gain for the open loop case. But when we look at the differential operation and try to apply such a high gain single stage amplifier in feedback, then of course, the closed loop gain will be smaller; this stage will be just providing other mechanisms for building a high gain op amp; through which we can realize closed loop systems with well defined gain.

In that case of course, the output; input output gain will be limited may be few 10's or 100 at the max. In some cases, when you are using this as a voltage follower, the gain from here to here closed loop case can be just unity and in those cases of course, the input string becomes important. And what we can see here is that input swing will be severely limited because you are having the DC potential over here pretty small; V G 1 minus V T 1 in this example. And therefore, the maximum potential that you can have over here you just going to be V G 1, the minimum DC potential here plus the V T of this. So, it will be very small swing allowed over here; if you are trying to push this to the minimum value.

So, in that case it will not act like a good voltage follower or it will not be able to cater to closed loop gains, which are limited with few 10's. So, we need to take care of the closed loop operation; if you are playing the differential scheme for this casecode for realizing op amps and building feedback amplifiers with the help of this high gain stage.

So, let us straight ahead go to the differential scheme; which would just imply that we use that another alternate branch, the differential branch and put a current source over here just like we do for the simple common source stage.

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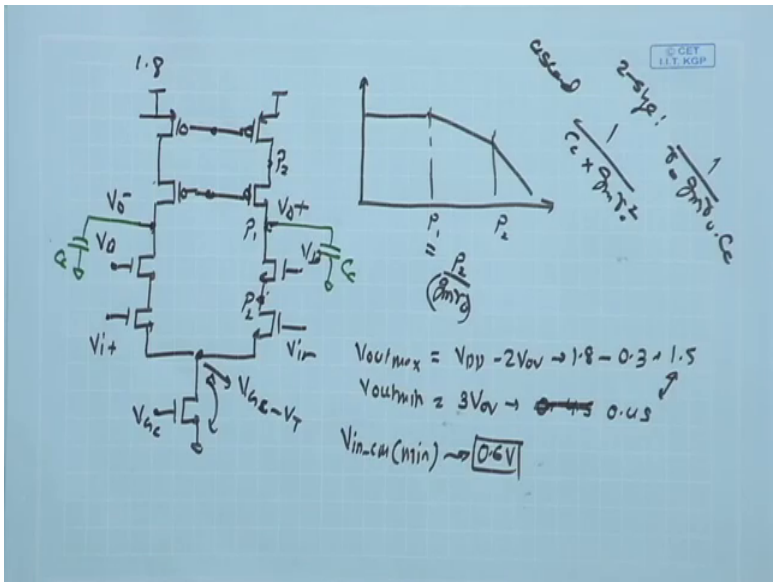

So, just like in the common source stage we club the two differential pairs; I am just going to do the same for this one. So, that would imply that I have the cascode branch and the input branch and along with that I have the tail current source. So, this is possible scheme; now these two gate voltages, they can be bias with the help of some common mode feedback scheme that we can discuss; just like we do it for our normal differential amplifier with the active load and again I need a proper bias point over here.

So, I need a proper bias point for these devices and also I need to set up the bias point of the gate. And then I have my outputs over here V o minus and V o plus; if this is the V i plus and this is a V i minus. So, this is the corresponding differential scheme for the cascode stage and once again the analysis boils down to the similar process that we have for the differential amplifier analysis. For the differential gain you will just put this an AC ground; and then find out the gain from the input to the output which is just going to be g m r o whole square by 2.

And therefore, the overall gain differential gain V o plus minus V o minus upon V n plus minus V n minus its g m r o whole square by 2. So, the analysis for the differential mode remains more or less similar, only thing is we have to look at the other considerations; frequency response, swing, bandwidth etcetera. Now, whatever we discussed with respect to the frequency response and the bandwidth that remains more or less same, but whatever is applicable for the single in that case. Because for frequency response once

again this is AC ground for the differential operation, you have a dominant pole over here and non dominant pole at these two points. And if I am using this particular circuit for closed loop operation, I would like to compensate the output node over here directly because this is a dominant pole; I would simply like to put some mode capacitor over here so that dominant pole gets shifted further towards lower frequency and I can get a better phase margin.

So, here we have the dominant pole compensation coming into picture. So, here we are not going to rely on miller capacitance; we are not going to use miller compensation, but going for dominant pole compensation. So, you are having the first pole P 1 and the second pole P 2; where I already have say without any compensation; I have the P 1 coming over here and the P 2 that 2 P 2 poles here and I can call this also P 2; they are going to be remain relatively close because what we discussed over here the impedance at these points are almost similar. And as a result, the capacitances are also similar because they are coming from the parasitic of the devices; I do not have any additional capacitance put over here.

So, these two points are going to have similar poles in the overall response and so I can just put them as P 1 and P 2. And then I can look at the ratio of these two poles, if I do not have any additional capacitance input; it is going to be of the order of g m r o because we know that the impedance over here of the order of GM RO.

So, this may be P 2 upon g m r o and in the closed loop; if you are trying to build a closed loop amplifier with the help of this, I would once again like to have the P 2 to be much lower than P 1 by the vector of g m r o whole square; this is the overall gain. So, I need that P 1 times the g m r o whole square; that is the open loop gain of this amplifier is equal to P 2. So, I need to put an additional capacitance of this value GM or I need to make sure that the capacitance ratio over here, the capacity capacitance upon or the ratio of the added capacitance over here; upon the parasitic capacitance over here is also having a ratio of G M RO.

So, whatever additional capacitance I put at these nodes; I can call this C c or it can come from the load capacitance of the next stages. There I need to make sure that the ratio of this C c and the total capacitance over here is close to the g m r o factor. And it is not very difficult to achieve; if I look at 180 nanometer technology; for example, 1

micrometer with device 1 micro channel length and 1 micro beads; they provide you total parasitic capacitance close to say a few femto; 1 femto around and as a result say even if you are using a larger devices; say few 10's of micro.

So, the overall parasitic capacitance over here can be close to a few 10's of femto to 100 femto; it will not be more than that close to that range; so, a small fraction of pico farad. As a result, if you want to make this say g m r o time this; where g m r o is say 100 or larger than that. I can use a few pico farad capacitance over here so that it is easily say 100 times larger than the parasitic capacitance coming over here.

And I may not even need to put a separate C c because if you are having multiple stages and next stages is having a capacitive input; like we did for our front end amplifier. So, the C c will be basically coming from the input capacitance of the next stage, where the gain is determined by C 1 upon C 2. So, it will be basically C 2 of the next stage which is automatically giving me the required compensation capacitance.

So, that way we can say that this is self compensated; this cascode amplifier is having a property of self compensation, you do not need to worry about the insertion of miller capacitance, which leads to other complications. We have discussed other complications related to; arising of 0 and then we need to figure out techniques to cancel out those 0's by inserting buffers or by inserting the nulling register; which again has to be controlled.

So, it leads to a lot of complications definitely, but here we see that it is able to self compensate and mitigate the instability issue. And of course, one of the limitation that we have seen is that the output swing is relatively limited in this case. Now, once you have added this tail current source; output swing gets further limited because now this is not longer at source, you need another V overdrive voltage for this current source.

So, if this is V G of the current source V G C; the minimum voltage here that you can have, the minimum absolute voltage here you can have this V G C minus V T; that is basically V overdrive. We call this term V overdrive, which is V G minus; V G S minus V T. So, here once again I have another V over drive added and we know that for this stack, we have another 2 V overdrive.

Therefore, the minimum level that you can have over here is going to be 3 V overdrive and on the upper side Vdd minus 2 V overdrive. So, again the swing is getting further

limited; output swing is getting further limited and once again if you are operating this as feedback amplifier, then the input swing may need to be close to output swing. For example, a unity gain buffer; where the input output are change in the same fashion. Or even if you are having a relatively smaller gain factor of say just few 10's; in that case the input swing may be just around 10 times smaller than the output swing; output swing is say target swing is 1 volt peak to peak

So, here I want at least say around 100 millivolt input range and with 1.8 volt supply; I would to make sure that the required input swing is the achieved. And apart from that input common mode range is another important factor, where the input DC level of this stage may be come from some other stage. And if in a cascade of analog stages, the input DC level of this point is coming from some previous stage; which can you know change over time; I need to make sure that the input common mode range or that is basically the range of input DC bias point that this amplifier can tolerate, that should also be sufficiently large so that it is to tolerate any change in the input common mode DC level.

In our example that we are dealing with; we have anyway stated that the output DC common mode is being determined by common mode feedback; if it is a fully differential case, if there is fully differential operation. And then with the help of that, we are fixing the input common mode level. If we do that here, once again in that case basically; you will be pushing the input common mode DC level or input bias point close to the output DC level. Now output DC level, if we look at it in this particular example we are seeing that the maximum signal swing.

In this example V out max that you can have at a single end is equal to say Vdd minus 2 V overdrive and the V out min that you can have is 3 V over drive basically or V over drive of these two transistors plus this one. So, of course, they are not equal because it is not necessary that the current in the W by l are equal; here we can say that the W by l in the currents over here can be different from that of this one. But I am just taking this number V overdrive where the common factors, it is around 3 V overdrive. And this can be 1.8 volt minus overdrive even if it is 0.1 volt or you know or 0.15 volt; this can lead to 0.3 volt over here and the maximum maybe around 0.3, so, 4.5 volt sorry; 0.45 volt over here.

So, you are having from 1.5 to 4.5 and therefore, we can say that 1 volt can be achieved 1 volt peak to peak can be achieved. And then I would like the output DC point to be close to midway of this. So, we are seeing that the output DC point for a 1.8 volt supply can be close to 1 volt. So, I would like this to be 1 volt and then in that case, if I try to apply that same 1 volt over here; means using our earlier scheme; where we are using resistive feedback and try to apply the same 1 volt over here, whether this is going to be a good bias point for this one. There we can see that, if we apply 1 volt over here then basically, this potential we were trying to keep it at the minimum allowed DC level so that I can have maximum possible swing.

So, if I look at my minimum allowed DC potential that I arrived at; what was that? That was the V G minus V T plus V G S and V G minus V T once again because it is low current biasing. So, the V G minus V T can be close to say 0; maybe 0.1 volt or something and then you have V G S; which is again close to V T. So, that is again going to save a 0.5 volt; so, 0.5 volt plus 0.1; so, it is around 0.5, 0.6 volt. But, if I am allowing, so the V in; I would say V in CM min that I have estimated is around say 0.6 volt; this is the estimated value in order to allow maximum possible swing at the output.

But if I use the output DC point in this case to bias my input DC; then I am going to have midway of this. So, desired output; DC point at the output is 1 volt in order to allow that maximum swing and I am going to allow that over here by that large resistor and that definitely is much higher than what I want for best swing at the output.

So, it is not going to serve the purpose of having best possible swing at the output because I cannot apply the relatively higher output DC level over here; output DC common mode level over here for biasing the input DC common mode for my input pair. Therefore, this may not be a very good scheme I may have to go for some alternate biasing scheme for the input and complicate my design further. So, this is one of the main issues the DC biasing for the input can become problematic for our application. And in general if you are looking for feedback operation where you are having a voltage follower operation; there also you can see that ultimately the DC point at the output will be affecting the DC point or setting the DC point at the input. So, you cannot even build a good voltage follower using this scheme. And in our particular example, the main concern is that we are setting up the bias point over here with the help of output common

mode; which is not very feasible here because it is going to drastically affect our swing; this point is clear? What we are trying to mention over here.

So, the good points with this scheme; with this perimeter circuit is good differential gain in a single stage of getting g m r o square, self compensation property with the help of which without even adding very significant; very large capacitance you are able to achieve a good phase margin. And we will see that on the other side is a negative points that you have is the limitations on output swing and more severely the input biasing.

How will you use the output DC common mode for maximum symmetric swing to bias the input DC. There are some other advantages also; like we have discussed the concept of PSRR; Power (Refer Time: 23:18) Rejection Ratio. There cascode devices do have advantage as compared to our two stereo op amps; that we have not discussed in detail probably in another class we will try to address that as well.

So, any question before we try to look at alternate scheme, which is a folded cascode scheme which can resolve this issue of DC bias and the swing; at least the input swing. And then also we have to look at biasing scheme through which we can get best possible output swing. This is the next discussions; looking at the folded cascode topology where the constraint on the input swing and the input DC biasing is resolved. And second the output swing considerations, where I need to set up the appropriate bias point for these transistors so that my output swing is maximized.

And once again we can look at both the topologies; the single ended output one, just like our different amplifier with current mirror load, where you have single and output. And the second one where you have fully differential output and you need the common mode feedback. Any question before we proceed further.

Student: Can you explain (Refer Time: 24:28) why 1 volt input supply DC not suitable?

So, what we said is that if you look at the minimum allowed DC potential that we found out for this. Why did we found out minimum allow DC potential? Because if we put the minimum allow DC potential, then only you can have maximum allowed swing. If you put this DC potential or the DC bias lower and lower, it will allow the output V out min to be lower and lower.

So, from our analysis earlier we found out that V in C M min; that is the input DC point; minimum value of input DC point will be governed by the minimum DC potential allowed here which is V G C minus V T; plus V G S and which is close to 0.6 volt; assuming this rough number that V overdrive is lower than 100 milli volt; 0.1 volt and V G S is close to V P; which is say 0.4 volts. So, I am just taking rough numbers and telling you that overall the minimum DC level that you can have at the input is 0.5 volt; close to that, in order to allow maximum possible swing.

But for maximum possible swing, the allowed or the desired output DC level is 1 volt, but that 1 volt; if I put it over here definitely violates my condition means it is much higher than the minimum DC potential that I can apply. So, that is not going to let me maximize the swing at the output.

Student: So whatever (Refer Time: 25:56).

So, bandwidth if I look at the overall response, you are having the total bandwidth after compensation even if you add C C; the total bandwidth is given by g m r o square. So, if I look at the overall C values, so what is that C C; times the g m r o square; this is the pole overall. So, if you compare it with what happens in the two stage op amp; when you are having compensation, there also ultimately; this is your cascode and two stage also you are having the RO and you are having the gain factor g m r o and you are having the C c. So, the bandwidth is it can be similar both the cases; any other question, before we go to the next module alright.

So, the main take away from this is you should understand the advantages of this particular scheme and the limitation that we are going to solve using the folded cascode scheme and then look at the biasing and other analysis in the (Refer Time: 27:23) frequency response noise etcetera. So, let us take a 2 minute break and after that we will start the next module.