Analog Circuits and Systems through SPICE Simulation
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Lecture – 51

Welcome back let us resume our discussion on the transistor level implementation of our flip flops.

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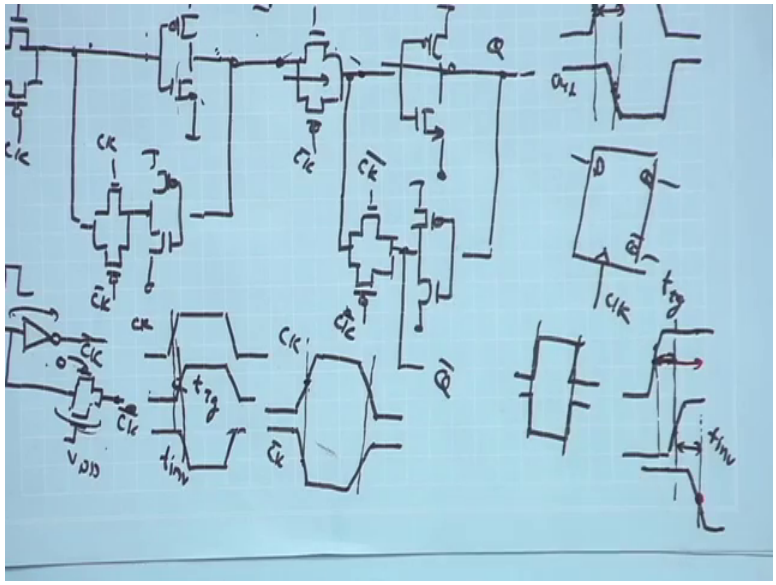

And look into the characterization of the flip flop in terms of the delay definition. So, we just ended last time with the discussion on delay that if you are having an inverter and looking at the input which is having a finite rise time and fall time. The output is also going to happen at I 7 fall time and also a delay because ultimately there is a rc time constant associated with charging or discharging of the output capacitor at the node. So, roughly we can depict these waveforms with rise time fall time of the waveforms and associated delays. Ideally we would like to have the clock and clock bar to be exactly out of phase. And for that if you are having a gluon global clock signal generally we like to make the clock bar or generate the clock bar using inverter we would also like to make sure that this clock bar is exactly out of phase with the clock.

So, the there is no significant delay between the rising and falling edge of the clock. So, in general in the circuit you may have a digital signal which is single ended it is not a

fully differential signal. So, the source may be single ended and from there you may be generating clock and clock bar at different points. So, just one point to be noted is and that condition people generally use a combination of T g and an inverter. So, you can put a T g over here which is always on. So, it is going to be V DD and this is set to ground the PMOS. So, that if this is clock and you are having the clock appearing here as well. So, when there is a transition in the clock over here there is some delay for the T g also because T g introduces some rc delay. As a result sorry, this point will also have some delay as compared to the input clock. So, in that case I can have the phases or the transition points of the clock and clock bar matched. So, the purpose of introducing this T g is to match the delay between the clock and the clock bar whenever you are generating the clock bar using an inverter.

So, the inverter has it is delay t D likewise the transmission gate will have some delay tb and to some extent these 2 delays can be matched not exactly, but to some extent if you size it properly the NMOS PMOS over here the NMOS PMOS here has similar dimensions and they are size properly the delays of the pg and the inverter can match. So, the pg output will be looking like if you are having the input waveform coming like this. The T g output if this is the ck the T g output will be just the same waveform, but delayed by a small amount given by the distance between the midpoints. Likewise the inverter waveform we expect this will also be a little bit delayed and inverted. And once again the delay will be corresponding to the midpoint. So, what we expect is that the T g delay t T g is equal to t inverter. So, that the waveform generated clocking clock bar are not having shift with respect to the transition points.

So, this is another point we should note while generating clock and clock bar from a single signal in a circuit. Now once we have this definition of the delay based on that we can try to categorize this flip flop in terms of 3 important quantities that is set up time whole time and c 2 Q delay. So, we are already familiar with the consequences of the c 2 Q delay we have seen that if you are having a ripple counter you are going to have n times c 2 delay in the entire chain the output final output bit will settle after n times cq tcq delay. So, in this case if I want to assess what is going to be the c 2 Q delay? For that I have to see the slave phase this is a master stage this is a slave stage. Remember when the clock phase is negative in this case suppose this is a positive edge triggered flip flop, because when the clock goes high here then the Q changes picked. So, at the positive

transition of the clock the Q over here will be changing state. So, this is the positive edge triggered and we have seen that negative edge triggered means you will have to just flip the clock polarity, here it will be clock bar by the clock. And here it will become clock and clock bar that will be a negative edge triggered flip flop.

Now, in this case if you if you have a positive edge triggered flip flop in the negative phase of the clock this latch was on this slash was off this data was stored and this was transparent to the input data whatever data was available here it was this latch was on and it was transparent this entire chain; however, this was off and now when the clock is going high then finally, this data will be propagating to Q this will also have the transmission through this inverter and storing the data over here. So, that when the clock is going low again this is going to turn on and I am going to have the feedback. So, the c 2 Q delay if I want to define that after the positive edge of the clock here, what is the time taken by the Q over here to settle? So, that will be given by the time taken by the data over here to propagate through this pg and finally, through this inverter to this final output. So, at that point I can say that is the tc 2 Q of the inverter that is the time or the time delay after the positive edge of the clock, taken by the output over here to settle that is going to be that t g plus t inverters.

So, if I draw the waveforms over here if this is your clock wave from the rising edge of the clock, the T g will have a certain delay and therefore, the data stored over here it will suppose this is V DD. So, it will have a certain delay and with respect to this midpoint it will it will rise after certain duration. So, this is the this is the delay of the tg. So, I can say t T g. And after that you have the inverter which will again have some delay. So, after the transition after the data is passed to the T g and available over here the inverter will have some additional delay with respect to this midpoint. This is the t inverter and therefore, the tc 2 Q from the positive edge of the.

Student: Clock.

Clock that is the midpoint of the positive edge of the clock the midpoint of the data transition is given by the total tc 2 Q delay this is going to be t T g plus p inverter. So, this is one important delay parameter for the flip flop after the positive edge of the clock I in taken by the sample data to reach q. So, this is the tc to Q because the towers are already available over here. And the only one T g delay and one inverter delay it reaches

the final output. Now therefore, when you are trying to characterize the if the flip flops and trying to see the total delay in the ripple counter it is going to be there it is going to depend upon this 2 components. Now let us look at another very important decision definition which is the set up time.

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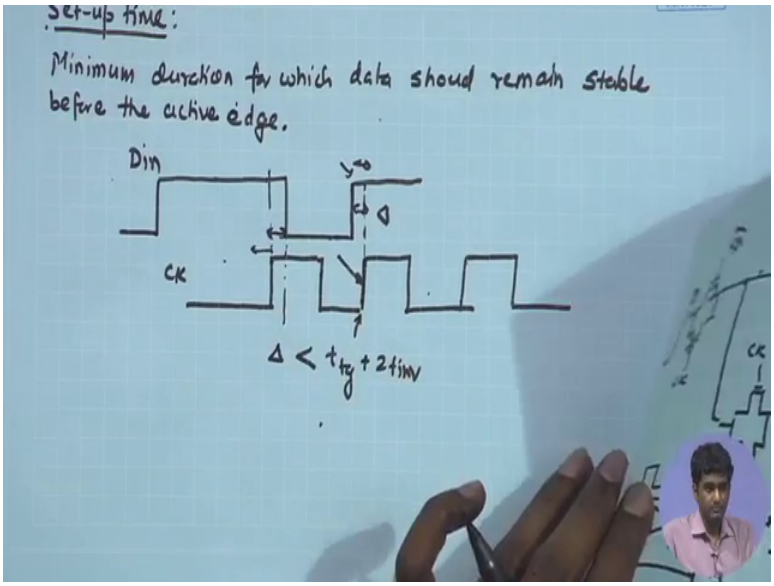

Now for set up time is the by definition which is the minimum duration for which data should remain stable before the active edge. Activate means the sampling edge, in case of a positive edge triggered flip flop the active edge is basically the rising edge and in terms of the negative edge triggered flip flop the active edge is the falling edge. So, here if I look at the definition. We are trying to see what is the minimum duration for which the input data over here D should remain stable before the positive edge of the data.

So, this means that if you if you are looking at the data. It is it can change at any arbitrary point suppose it is coming from some logic gate it can change at any arbitrary point, and the positive edge of the clock is coming immediately before the eta transition. This is the clock. You have the clock continuously running. And at this incident is going to happening is just before just immediately after I can say in order to denote that. So, here I can say just I will have to draw in this a different ways. So, that mean and all the data transition it is some other point where you have the data transitioning just before the positive edge. So, that my definition is that before the positive edge of the clock what is the minimum duration for which the data must remain stable. So, here again see the

suppose the data is transitioning here. So, this is the D in and the way I have drawn the clock suppose you have the continues clock waveform going in it will going on.

Now, here just before the positive edge of the clock the data is making a low to high transition. And ideally we would expect that the Q output of the flip flop that we have here that should finally, make transition to 0 to high accordingly, because as per the definition of the flip flop operation right at the positive edge whatever is the de available it should be sampling that. But physically there is going to be a limit. You cannot expect that if this delta is turning or tending to 0, 0 plus even then the flip flop will be able to latch the data. So, where is that physical limit coming from what is the minimum delay it can handle while a while being able to latch the data correctly.

That depends if I look at this circuitry what is happening when that clock is going from low to high when the positive edge is coming. Before the positive edge the data over here is supposed to be stationary and when the positive edge comes right over here is supposed to propagate to the final output or being sampled by this particular transmission gate, but when the data over here itself is changing just before the positive edge of the clock; that means, before the positive edge of the clock came and this one completely turned off the data in over here flip the polarity; that means, it was expected that this data would also flip the polarity accordingly from low to high if this was going from high to low this should also have flipped the priority from low to high So that the final data can also be low according to the input.

But of course, there is a finite delay from this D input to the final output it will take some finite delay for this output to settle over here. And not only that you also have a feedback transistor and here we also need to make sure that before the switch here turns off this input level is able to propagate through this feedback transistor and arrive at this point So that after this turns off you have a stable feedback operation established and the data over here and here is stable. So, I would like to make sure that before the positive edge of the clock, any change in the data has been conveyed till this point it has passed through the transmission gate it has passed through the first inverter and also it has passed the third inverter it is second inverter it is coming over here, So that the moment this is turned off you already have that stable data available over here and it will be establishing the latching and retaining the data. So, for the t c 2 Q delay we did not consider the latch over here we did not consider the second inverter over here, because there the condition

is that the data should be available at the Q point the moment the data is available in the 2 point; that means, you have a the final output equal to the sampled input available at this point for reliable operation of course, we can also include the second inverter delay. So, that after this is turned off this data is retained, but when the positive edge of the clock is coming see that after the positive edge this is going to remain off and therefore, this is not going to play a role in the propagation of the data from the input to the output.

Therefore we are not considering the second inverter when we are looking at the delay from the input to the output from the input of the slave latch to the output of the slave latch; however, when we are looking at the set up time that is the time taken by the input data to propagate till this point we are concerned with the latching operation means after the positivity of the clock when this turns off the data over here should be stable and therefore, we need to traverse this 2 inverters and arrive at this point.

So, that is giving me the set up time. So, before the positivity of the data if there is any transition in the input sorry before the positive edge of the clock if there is any transition in the input it should be able to propagate through this inverter and a second inverter arrive at this point So that and after the positive edge of the clock that change level can be copied to the output. So, here what I can say is if this if at this particular point the data transition happened too quickly because this delta delay this delta is less than the this delta is less than the T g delay plus 2 t inverter delay; that means, if this delta duration is lower than the this path delay from the T g the first inverter and the second inverter; that means, before the positive edge of the clock when this turned off the data has not propagated fully in this loop that has not been stabilized at this node. And as a result when the T g over here gets off and this particular clock over this particular T g over here gets on the data at this point can end up having the reverse polarity it can end up having the opposite polarity.

And therefore, we will expect that rather than sampling a high level it can end up having a low level. So, for this particular configuration of the flip flop this T g plus 2 t inverter gives us the set up time. That is the time taken by the input data to traverse the first inverter the latch the first inverter and the second inverter and be stabilized at this point.

So, that the moment this is turning off you have both these data stable. And as a result when this is turning off and this T g is turning on that stable data is propagated to the

second stage. If this data itself is transitioning it is not stable and this one is also transitioning it is not stable it is in the transition phase, and then you are turning this one on. Then you do not have a guarantee that this one being turned on and this is in the transition phase you do not have a guarantee that it will settle to the right level and as a result it can end up being in the wrong phase. The data which is getting to the output it can end up being the in the wrong phase. So, this is the definition of set up time and looking at the circuit operation this is how we can arrive at the definition of setup time. The other in order to look at the set of time in a little bit from a different angle we can also see that if the data over here is not settled and you are having the clock edge going up and the clock bar going down, and of course, the amount ideal all says they are having some overlap in this region.

So, there is a region in which both of them are on. So, there is a transition region rise time of fall time the other which there will be some small region where both of them are remaining on. And in that region of course, you have the transparent you have the first latch open and you have a second letter also partially open. So now, them are fully closed. And if the data over here is not settled the data over here this has some transition when it is not settled well. This is not settled well and this is getting closed. As a result you can have this particular gate turning on and the data over here can end up driving the data over here. It can influence the data at this point, because this is turning off if this turns off fighting more quickly as compared to this and we have the data over here well settled. And the data over here is not settled. So, whatever the data was available over here it will have it will be having the on path and it will try to drive it towards the higher value. So, the value over here can get dictated by the output node rather than this point writing to the output node this can end up writing to the master latch.

So, thereby reversing the master slave operation. So, that is that is another issue. And here one of the reasons why we are including this T g is to prevent or to minimize that possibility. Because if you do not have this transmission gate and you have this inverter only directly connected to the output. And you have some overlap between the clock phases and therefore, these 2 are getting on simultaneously, there is a higher possibility that when this is trying to get off and there is the data transition and this is trying to set it to some value this is not settled properly this is just a again to some intermediate value, and both of them are simultaneously turning on in this small duration. As a result you can

have this inverter output influencing this output this first latch output, rather than the data over here writing the data here and then finally, copying into this output can end up writing the data here. So, it will flip the masters state.

So, this will be the opposite operation we do not want the slave to influence the master even the master turns into slave. But because of this overlap you can end up having the opposite operation. So, this T g to some extent minimizes that effect because it is getting on when you have the clock (Refer Time: 20:17) for the T g getting off. But once again if you have some overlap they can be on for a given duration all of them can be on for a small duration together. And in that case there will be a fight this node will be trying to influence the node over here. If this is not settled well because of the transition in the input data if it is just transitioning while the clock transition has arrived.

Then this is at some intermediate value because the data has not settled this has just made a transition before the positive edge of the clock this is also transitioning while the tgs together are getting on because of this overlap of the clock right. So, in that condition this is just transitioning it is that intermediate value therefore, this acceptable to be written by the previous by the slave stage rather than following the masters input. And therefore, this is very undesirable it can once again lead to wrong latching of the data. So, we can see that if the data has arrived at least 2 inverter plus T g delay before the positive edge we can make sure that this data has settled to the right value. And after that if we are opening the after that is the positive the clock is coming and this is going on then reliably it can be copied to the next output. So, that gives us a definition of set up time. And any question? You getting the definition of set up time in terms of the transfer level operation how is it coming from this particular circuitry.

So, high level definition is this is the definition of the rep time the minimum duration before the positive edge of the clock before the active edge of the clock at which the data should become stable. If it changes after the set up time t edge minus set up time if the data changes, after t edge minus t set up, then the latch up or the data latched weather flip flop can be wrong, that is the conclusion out of this set of time discussion.

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No the data transitioning is the major reason for set up time evaluaton. So, the data is transitioning just you know before the positive edge of the clock and data has not been

able to propagate till this point. Then this is you know this is not settled to the right value. It is some intermediate value and therefore, you are not sure that once this gets off what is the value going to be here. What is adding more to the damage is that this overlap of the clock can you know further impart the influence of Q to this point? Even if you do not have the influence of Q to this point and this data has not settled you do not know where it will end up it can end up high or low because it is in the transition point. And likewise here what can aggregate the problem is that you can have some overlap because of which this Q is having an open path and it can this inverter can influence this data and that is adding to the trouble, but the set up time evolution is coming because of the you know is the change of a transition of data just before the positive edge of the clock.

So, it should transition sufficiently below sufficiently before the positive edge of the clock then only the value will be latched correctly. And then the other important definition is whole time which is just the opposite of set up time.

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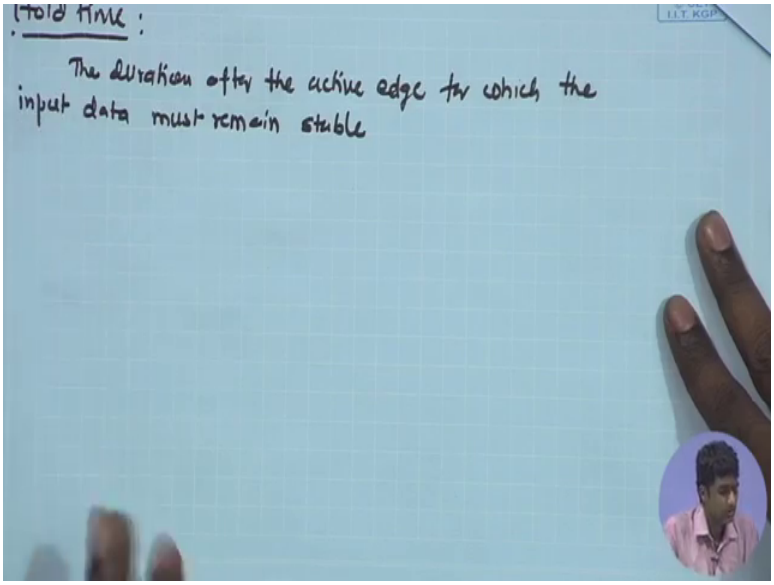

The Duration of the active edge for which the data must remain stable or the input data must remain stable; that means, if I go back to the waveform and look at the first case that I have drawn over here. So, here the data is transitioning just after the positive edge of the clock. And here I have to see that what is the minimum duration if the data is transitioning just after the positive edge of the clock whether the flip flop is going to be able to latch the correct data over here. For that once again I need to go back to the

transistor level circuit and try to see from where this whole time is going to arise. Ideally if I have these transmission gates driven by very idle clock pulses means, which are not having any rise time fall time clock is extremely steep and clock bar waveform is also equally steep.

So, if both of them are equally steep clock and clock bar having very negligible rise time and fall time ninety degree drop, and under that condition when this T g is getting on immediately at that point this is getting off this is getting off immediately then this is getting on. Therefore, if I say that that after the positive edge of the clock this is anyway disabled. So, this does not have any influence on the data that was stored over here. And after immediately after the positive edge of the clock this is getting on therefore, whatever was the data level available at this point it is going to propagate to the output. So, if the clock pulses are having negligible dice time and fault immediately after the activate that is immediately after the rising edge this is getting on and this is disconnected from the input the input is no longer is going to influence this point. And as a result whatever data was sampled over here at the, but whatever present over here before the rising edge of the clock it will be reliably latched to the output.

So, for ideal clock right time fall time 0 right time and fall time the whole time will be 0, because for this particular configuration for this particular latch as soon as the clock transitions to high value. This is cut off from the input data input data cannot influence this node. And at that time you have the whatever data was available over here it is contributing to the output is getting transmitted to the output. So, for this latch if the rise time fall time of the clock is very sharp. We can have close to a very small whole time negligible whole time and ideally 0 whole time circuit, but once again the moment we are start having finite rise time and fall time for time for the clock. And you have the overlap between the clock and clock bar. Once again any data transition over here just after the clock edge can propagate through the clock through the circuit over here because of the latches being on simultaneously.

So, during this overlap phase if the data is transitioning just after the rise of the fall or during the rise of the clock edge. If the data is transitioning you can end up having the transition in the input data being propagated to the output. And as a result the whole time will be dictated in this case by the overlap or rise time fall time overlap of the clock in clock bar. So, if you having a larger overlap between the rise and fall time if the

waveforms are much sluggish. Then you are having a longer duration for which the output is directly transferring to the input. And during that point despite the transition happening in the positive edge you can have the data from D propagating to the Q. And therefore, you can end up latching the wrong data. So, the whole time will be bad in your case you are having more overlap in the clock; however, in case you are having ideal clock edges the data even if the data over here is transitioning just after the clock edge. It does not matter because this has been cut off. And the data over here is stable, but only in case we have overlap this particular latch can give you a finite whole time data must be stable before the clock edge start transitioning.

So, that will be given by t overlap. So, this is the third important timing definition with respect to the flip flop and they become very important when we are considering sign connoisseur. Or n connoisseur digital circuitry which are operating in mixed signal environment also for digital circuitry when we go for digital design of digital architectures where you are having large number of these flip flop implementing state machines or incrementing pipelining etcetera, there also these definitions become very important. And it is important to be able to trace down these definitions to the transistor level implementations, how they are or originating from the circuit at consideration. So, let us is stop here before we started next module.