Analog Circuits and Systems through SPICE Simulation
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Lecture - 50

Welcome back. Let us resume our discussion on the latch circle that we are looking at transferable implementation of the latch and the clock. So, we started with the simplest latch circuit which is just having a switch along with the capacitor.

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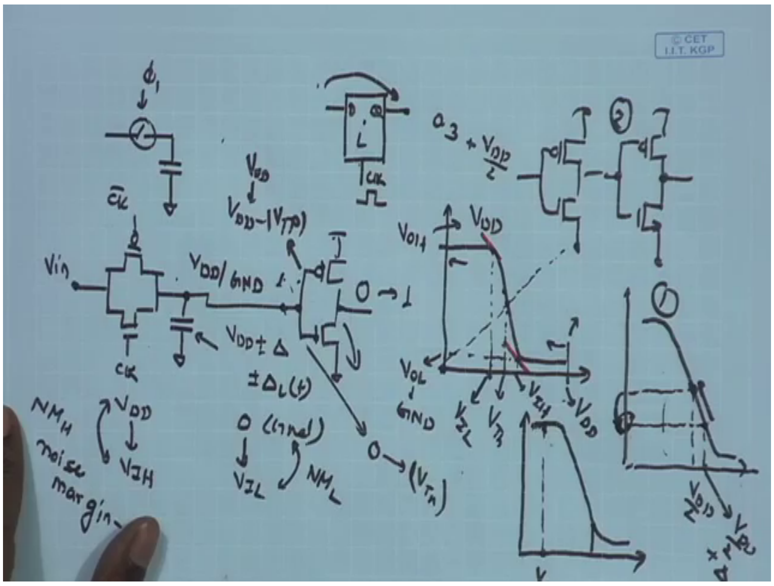

And this can fairly well act like a simple latch, when the phi 1 is on the switch is on the input level V DD or ground will be sampled onto the capacitor. So, this is a single latch, which is double sensitive latch. Out of this we want to construct a flip flop, I can cascade 2 this latches. So, I can go ahead and put 2 such latches in series just like we did for the block level implementation. So, I can put 2 transmission gates.

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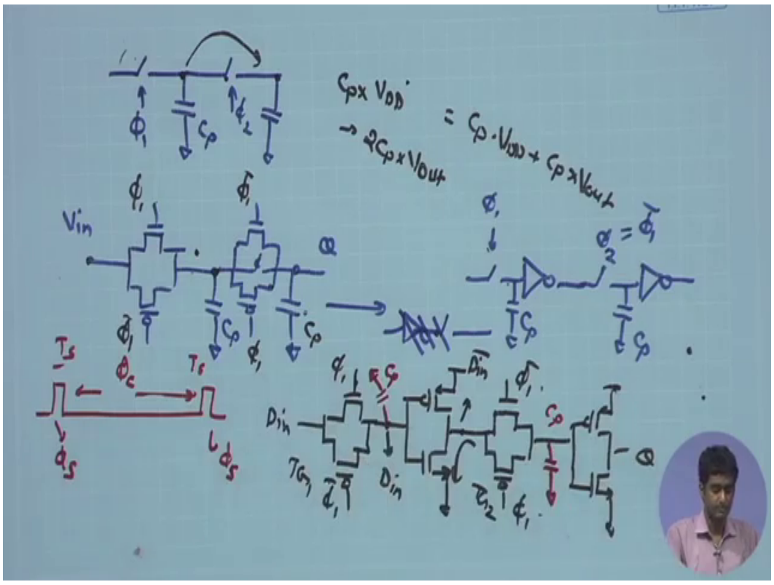

You can have as I said you may not even need a dedicated capturing this may be just a parasitic capturers coming because of the MOSFETs. And you can have another second latch which is driven by phi 2 and phi 1 phi 2 can be just the opposite phase of the clock.

So, if you want to have positive edge triggered flip flop, I can keep phi 2 as the positive pulse of the flop or the level one of the clock. So, correspondingly I have the transistor level implementation. Sorry, they are supposed to me the transistor of implementation. So, let me. So, this is a simplest possible implementation, where you can just a minute let me. So, this is the simplest possible implementation that we can have you have the input clock sampling the data at C p.

So, during the positive phase of the clock you can have the phi 1 over here, phi 1 bar over here. And then you have phi 1 bar over here and phi 1 over here. So, you can have during input during the high level of phi 1 you can have the Tg one which is transparent and pg 2 which is off as a result the input data is sampled at the C p whereas, when the opposite phase is on that is the phi 1 is low, and phi 1 bar is I this is going to be on, and this gets off immediately as a result the data is going to be the same value that was stored at C p will be transferred to the voltage the capacitor over here.

So, this is this can be as possible simple implementation. But what are the issues over here you can I can this work reliably is there any issue that we see in terms of data transfer. So, from V in to the C p and then from the C p to the final capacitor over here, which can also be C p this is just we are relying on the parasitic capacitances. We are not putting any additional intentional capacitance because in general you can have a large number of registers and flip flops in digital design. And if you start putting capacitances for each of those is going to take a huge amount of area for analog blocks there fewer in numbers in the front end. So, you are needing few big capacitors to implement them that there was just few in count whereas, digital unit is can be large in number. So, you need a huge number of registers and flip flopping of course, we do not we cannot afford to put this C ps or additional dedicated capacitors, we can rely on the mustard capacitor.

So, now what is the problem here if I look at the overall operation ideally if this voltage is in the first phase getting charged to V DD by the input. And next I am putting this latch on, what is the voltage we expect here is it going to go to V DD. So, phi 1 phase I charge this to be ready and in the phi 2 phase this was disconnected and this was turned on and therefore, we expect certain voltage over here what is that voltage is that V DD.

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V DD by 2, because the charge sharing will take place and the total capacitance has been increased. So, whatever was the initial would charge on the capacitor C p times you know V DD was the charge. And once you disconnect this that charge is now preserved that is not telling any paths to go. As a result now if this was initially discharged to 0 depending upon the voltage over here suppose this was 0. This will go all the way to the total charge being constant will be 2 C p times V DD or 2 V C p times V out as a result V out going to be V DD by 2. Of course, you can have some different voltage stored we can in the previous phase you can end up having a different voltage, as a result it will depend upon the previous voltage. So, this has to be in general equal to C p times V DD plus C p times V out and accordingly I can find out what is the V out level.

So, definitely this is not going to serve the purpose we are not going to get the same voltage level as we expect. So, in order to preserve that what can be done? What can be added to this latch circuit? So, that I can always ensure that if this level was sampled to be V DD the final level over here is also coming as V DD. Or with this first sample to be ground tunnel level over here is also coming to be ground. So, in that case I have to decouple these 2 capacitors I cannot directly couple the capacitor over here to the capacitor over here using this switch I need to decouple that. One way to do that is to put an inverter over here, if I put an inverter then I am able to comfortably decouple the latch. Likewise the input of this latch can be coming from some other latch or some other logic gate there also I would not like charge sharing with the input device.

So, once again I would like to put an inverter over there. So, I can put one inverter here another I can put another inverter over here, So that the capacitance is over here are not directly coupled to the capacitance on the other side. So, in order to arrive at the latch circuit. I can put inverters after or before suppose as I putting it before the. And so, if we if you have to go for say later we will see that putting the inverter after the switch can have some advantage because there we can apply some feedback configuration. So, let us go for the switches and go for the inverter over here and another switch another inverter over here. And then I have the parasitic capacitance over here which is given by the parasitic capacitance of those transistor at this point and likewise you have some parasitic capacitance over here C p C p.

And these 2 switches I Once again controlled by phi 1 and phi 2 which is which can be just phi 1 bar. So, by phi 1 bar means if this is the clock phase the high phase of the clock phi becoming the low phase of the clock that is it. And these are the parasitic capacitances constituted by this MOSFET and the inverters and so on. So, now, at least I have been able to decouple the 2 capacitances if I am sampling V DD over here, and after the phi 1 has gone low, the V DD the V DD voltage over will be retained over here. Of course, there will be some leakage and thermal disturbance, but to a significant extent the drop may not be very large and V DD will be retained and as a result output will be driven to low output of the first inverter will be driven to low. And therefore, when you close this switch that low level is coming to the C pu transistor level what is happening of course, we should have the picture in mind that what is happening at the circuit level and which transistor is getting on what is the discharge path what is the charge path and so on.

This is the translatable picture you have the phi 1 phi 1 bar, the phi 1 bar means just the opposite phase of the clock this is phi 1 bar and this is phi 1. And this is your D in and this is your Q. So, of course, we have 2 inverters now in change. So, the polarity of D in and Q is going to be same if the D in is 1, the Q is also supposed to be 1. So, that behaviour is of course maintained. And when the phi 1 phase is on this transmission gate gets on I am call it tg one tg one gets on. And the D in is stored over here. And during that phase this is off the tg 2 is off and as a result the output of this inverter will be D in bar. So, this will be D in bar.

So, this D in bar is the meaning transparent to D in, during the 7th phase if the dean is changing the value over here will also be changing and in the phi 2 phase this gets off as a result the value of D in stored over here becomes clamped. Because this after this is getting off whatever voltage was stored over here and this parasitic capacitance of this node will be remaining stationary. And as a result this will be the sample D in value and hence this will be the sampled D in bar value, if this was V DD this will remain V DD and this will remains 0. And the moment if this remains V DD; that means, this MOSFET will be on and it will be always shorting this point to ground, and the moment this latch goes on because this MOSFET is on it will also discharge this node to ground, as a result this will also bring the same value logic level 0 over here. And as a result the output will be going high. That is the overall operation phi 1 phase. This node the parasitic capacitance at this node C p you can write upwards.

So, this is the parasitic capacitance C p at this node. So, when is the switch is getting off over here this C p is touring the charge V DD times C p if the input level was V DD and that is keeping this transistor the NMOS in on state and as a result this particular node is pulled down all the way to ground. And likewise when the phi 1 phase is low or you can say the phi 1 bar is going high this switch gets disconnected and as a result whatever data was stored over here, on the C p that is retained it with this was 0 this is retained at 0. So, these are the 2 nodes or the parasitic capacitance and these 2 nodes are referentially doing the role of storage they are basically storing the charge in this particular configuration of the latch, is it clear?

Now, of course as we saw that we are not going to afford we are may not be able to afford dedicated capacitances over here and the leakage can become dominant. It can end up having a significant droop if you are having a lower clock frequency in the system and you want to keep the data stationary for a long duration, it can be a problem. If you are having a faster circuit or a faster logic then this configuration can work and people do use this flip flop configuration wherever fast preparation is required and you do not need to retain the data for a long duration. But in cases where the data has to be retain for long duration it can be a problem. For example, if you look at the counter that we are trying to build and the last logic level that you have there you can see that the counter level or the output level is maintained for long duration.

So, the entire sampling duration we have these Ts the sampling pulses Ts or we can we can have called them phi 1 in our case. And then you have this the clocks coming in between which is basically let me distinguish this from the phi 1 here I have used phi 1 just for the clock. And here let me call this phi s per sampling phase. And this is the phi I can say phi conversion phase where the ramp is happening and you are converting the data.

So, for this entire duration the MSB of the counter, it stays one for half the duration one 0 for half the duration therefore, the data is retained for a long duration for the MSB counter. And likewise of course, in this particular example in general we are having lower clock frequency as a result there is a significant deviations if we can have deviation in this voltage the bus can be expected. Especially if you look at the last flip flop as I mean will be flip flop with the conquer definitely that is having the longest duration of the data retaining retention it is touring the data for almost half the duration of this entire phi c, and as a result it can have maximum amount of deviation on the MSB level la that can end up discharging significantly for the same dimensions of this parasitic capacitances. Therefore, specially in low frequency operations we may not really rely on this particular configuration of the flip flop. Where we are using these parasitic capacitances to store the charge and retain the logic level. Rather we have to go for a system where we can have storage mechanism inbuilt and we can have some mechanism through which we can ensure the retention of this logic state independent of this parasitic capacitance value. And there we utilize the concept of positive feedback in this circuit.

Let us see what is the pos concept of positive feedback and how it can help us in implementing a stable storage element which is not only used in latches and flip flop, but it is also used in designing memories semiconductor memories, which are basically SRAM integrated on to your chip. Any question before we proceed? So, if we consider this inverter as an amplifier we know that in the sorry another just to be in ground.

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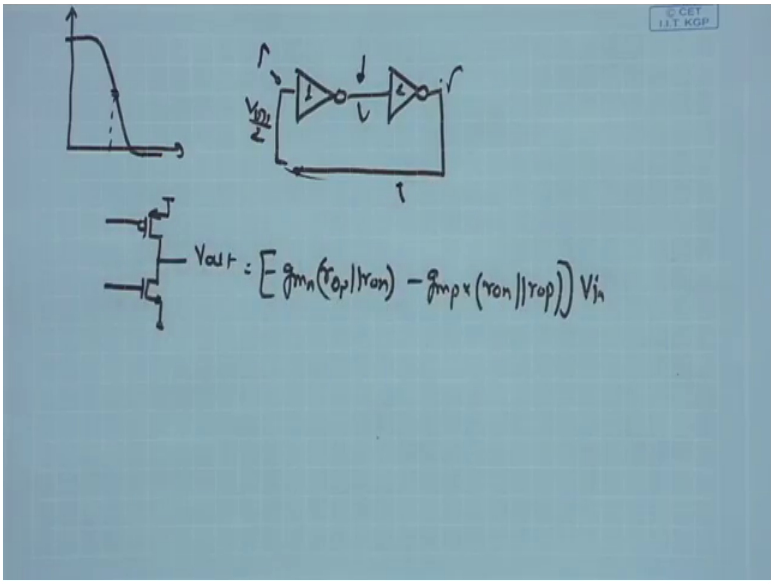

So, suppose by some mechanism I am biasing this inverter in this mid region. So, that it is in high gain region right this is what we do while operating a common source amplifiers or So, they are being sure that the input is such input is biased such that the biasing point is in this high gain region.

Suppose we do the same for this inverter because of because through some mechanism, we are able to bias 2 inverters. Which are connected back to back output of the second inverter they connected to the input of this first one. And the output of the first one connect to the input of the first one. Suppose we are able to buy us both of these inverters in this high gain region. And then we have we apply some sinusoid signal and we suppose bring this loop and apply some sinusoid signal at this point. What is the gain of that circuit? If we look at the overall behaviour we can just takes over position you have the same signal being applied to the NMOS and PMOS for the first device as well as second device also having same signal.

So, it is nothing else, but PMOS and an NMOS problems was amplified tight together I can take superposition and find out the V out as minus gm n times the ro over here which is ro p parallel ro n of the output times V in. Likewise you have the gm p minus gm p times ro n parallel ro p times V in. I can just takes over position. So, you have because of the first signal over here, I can assume that this is ac ground and then find out the expression for the output voltage. So, if I assume the signal is over here and put this to ac ground and I have minus gm p times ro n parallel ro p times V in signal coming over here.

Likewise second If I assume that the signal is at the gate of the NMOS and this is ac ground then gm n times ro n parallel ro p is the signal over here and I just add it together and for both of them of course, we are getting inversion. So, both of them have same effect of on the output for a given input and therefore, this is the small signal expression that I get. So, I can see this as an amplifier provided these transistors are biased in this region I am not saying how they are biased suppose imagine you have some mechanism through which you have biased. And then I can ask the question that if you if you have this connection can we see a positive feedback coming in; that means, if you because of some reason suppose this node voltage is going up.

If this voltage finally, also goes up tends to go up further; that means, it is going to support this transition from the initial point suppose the initial point was V DD by 2, it was the high gain region for both of the transistor suppose you initialize all these both these nodes the V DD by 2. And after that because of some reason because some noise this node voltage went up little bit by delta. So, what is the effect on the final node is it supporting the same direction of change or is it suppressing that. So, here if you see if this goes a little bit higher than V DD by 2 this is going to go down by a larger amount because we are in the high gain region. And as a result this is going to go up by a further larger amount therefore, supporting the same change. Therefore, we have a positive feedback established. Likewise if it is going down it will be going up and it will be going down even strongly therefore, to the supporting the same change or the same direction of change. Therefore, if you initialize this loop in the simulation suppose you initialize this loop to V DD by 2 here and V DD by 2 here by some appropriate setting, you have some noise injected at some point depending upon the initial condition of the noise or the noise level here positive or negative, the inverter can end up latching in one of the 2 levels high or low.

So, because of this positive feedback action. And once that is established the levels over here are stored indefinitely. From the point of view of feedback if I say if I am looking at the common source operation from here to here you have an 80 degree phase shift from here to here you have another 180 degree phase shift because of the inversion. Therefore, from this point at this point of course, we have 360 degree phase shift and we know we have considered we have discussed the stability criteria and in the amplifiers we always try to avoid this condition here 360 degree phase shift and high gain. And therefore, we know that in this condition for the omega or the frequency at which this 360 degree phase shift occurs the circuit will oscillate. So, that is the omega oscillation of the oscillator the frequency at which overall 360 degree phase shift across the loop is obtained. And if at that frequency gain is higher than 1 the circuit will oscillate here we have 2 stages we are in high gain region both of them.

Therefore the overall gain across the loop is definitely higher than 1, but what is the frequency at which omega 360 degree is being reached? That is omega equal to 0, because we know that you have the parasitic capacitances of this MOSFET which are going to further degrade the phase at higher frequency. So, omega equal to 0 we have exactly 180 degree phase shift across this one another one is exactly one, a degree phase shift across this one, but as we go towards higher frequency we know that the first pole we have another 90 degree phase shift second polar we have another 90 degree phase shift for both these inverter. Therefore, exactly 360 degree phase shift is achieved at omega equal to 0. As a result what we are seeing is that the inverter is latching up to one or 0 or 0 or one at omega equal to 0; that means, DC it is not changing

So, that is consistent with our discussion on oscillation and stability 360 degree phase shift being reached at omega equal to 0 and the inverter latching up at DC. One of them getting stuck to 0 another one getting stuck to one and therefore, storing this data indefinitely. So, this is the basic mechanism which is allowing us to store the data or save the data at these 2 nodes to either low or high or high or low indefinitely as long as the power supply is given to these inverters, is it clear? The basic storage mechanism in the latch. In order to construct the flip flop out of this latch; however, we need to write into it we need to deterministically write into the logic levels here and here.

So, that we need to access these nodes and intentionally write logic high or logic low into them.

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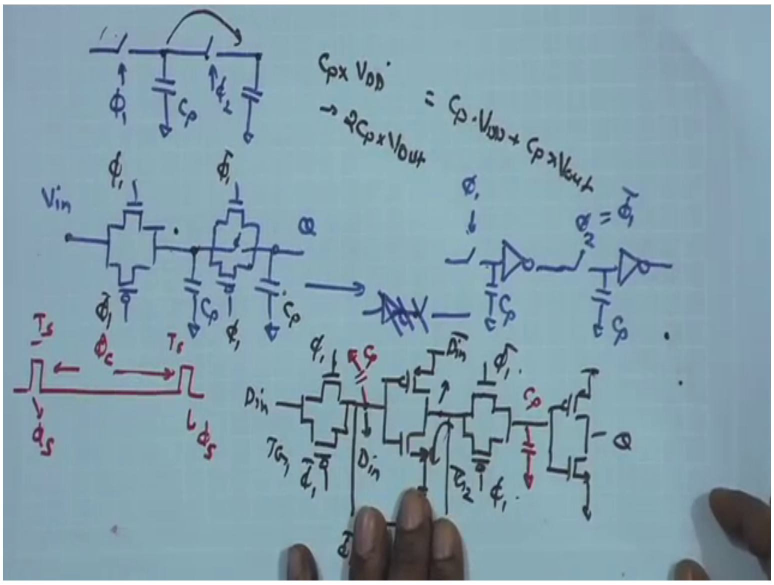

For that I can I can go back to my latch Circuitry that I built which was not having any feedback, and try to modify it try to insert a feedback over here. Here you already have a driving mechanism here, if I insert a feedback for both these inverter and try to make sure that these are going to store the data then the data storage is not dependent upon these parasitic capacitances, we can make sure that the overall circuit operation it stable means if the values are going to be latched and stored for a sufficiently long time. So, one way of doing that while ensuring the right ability, is to insert a inverter in feedback path over here, and keep the feedback path off when the writing is going on at this node, when do we need the feedback when do we need the feedback only when this is disconnected.

So, that is the stored data over here is retained for long duration. So, when it is getting retain or when this latch is on we do not need feedback, because at that point I need this node value to be determined by the input value. But when this is getting off then I need the feedback to retain this data, I need the feedback to be woken up and retain this data. So, a logical conclusion would be to add an inverter over here, add an inverter over here and then put another switch and connected over here, this switch should be given by phi 1 bar.

So, that when phi 1 is on this latch this gate is transparent transmission gate is transparent this node is connected to D in that value over here is dictated by D in this is not playing any role in determining the data over here; however, as soon this goes off I want to retain this data I do not want this to be leaked because of the different leakage paths that we have in the MOSFET. As a result I am turning on this feedback path So that you are having a positive feedback in this loop. And you are ensuring that this node voltage and this node voltage is fixed or clamped to the value to which it was written. If I if I do not do this, if I do not have the switch if I just have this inverter if I do not have this additional switch, then you cannot determine that when this node is then this switch is getting on this node can be driven by this inverter as well as the previous stage.

So, I cannot determine whether what is the logic state of this node. It can be the previous stage you have an inverter which is trying to drive this node to V DD, and at the same time you can have and some other intermediate logic state which is you know being driven by this particular inverter, more severe condition occurs when you have the clock overlap and you can have the logic stored over here trying to propagate through this inverter into this particular node. So, I would like this node to be dictated by the D in when the phi 1 phase is on and not by this path this is activated only when required when this data stored over here is supposed to be retained. So, my final implementation of the flip flop considering this topology would be including just another inverter over here along with the switch and hence creating 2 latches which are having the positive feedback path activated at the complementary phase of the clocks.

So, I can complete the overall latch the flip flop circuitry.

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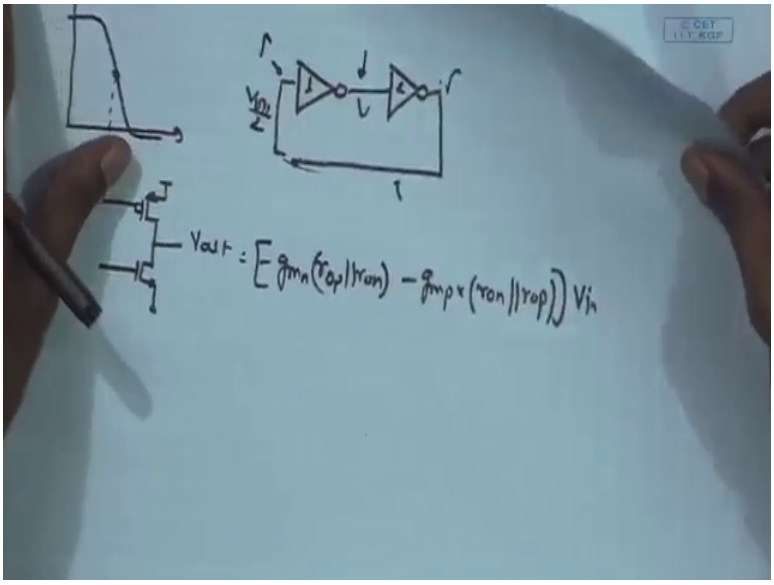
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$\frac{V_{DD}}{2}$
1
2
$V_{out} = \left[g_{mn}(r_{op} \| r_{on}) - g_{mp} \times (r_{on} \| r_{op}) \right] V_{in}$

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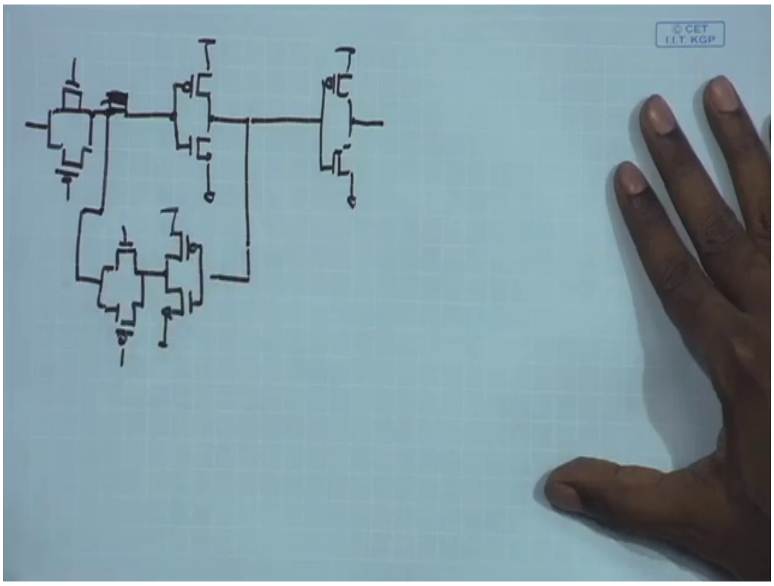

Or let me note down an input state, we have the rules sorry, I have to let me revise make it up.

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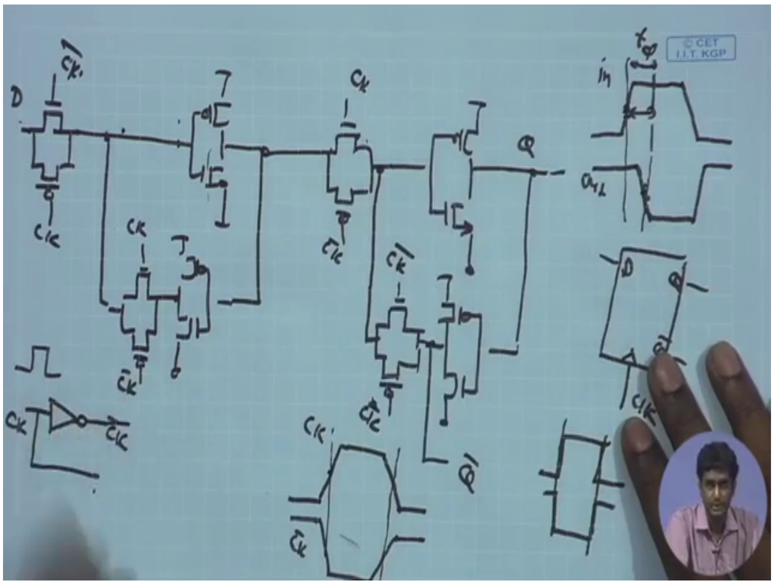

So, you have the so, this is our overall implementation, where the data can be retained for a long duration. So, here I can start if it is a positive edged got to flip flop then I know that this second level supposed to be triggered by the clock, again it is a clock and clock bar and then your clock bar sorry, clock bar and clock. Likewise you have the clock bar over here the opposite fridge and clock here and you have the clock and clock bar here.

So, this is overall circuitry for the flip flop that we can have which is robust enough and it is able to retain the data for long time and is not we are not depending upon the opacity capacitance for sampling the data. So, you can call this as D and this can be Q. And also we can see that the Q bar is also automatically available. So, I can also use the Q bar over here. So, this inverter is also giving us Q bar. We will see that it may not be a very good option to use this s Q bar rather than I can use other inverter to use Q bar we will see that y. So, this is the overall edge triggered positive edge triggered D flip flop that we are having D Q Q bar, and you have the clock edge and this is positive edge triggered.

So, I do not put a bubble over here and you have the input and output terminals. So, this is the basic building block of our of our flip flop of our counter any question before we go further and try to characterise some of the delays and transition diarized and related definitions for this flip flop which can be useful. For our the design remember while designing the counter we discussed the clock to Q delay which is going to determine how much is the ripple duration from the input to the output. So, we need to see what is that ripple duration. And likewise you also need to see to other very important definitions the set up time and the whole time which also plays very important role in operation on the flip flop.

So, we are all going to look into 3 important definitions set up time whole time and clock to Q delay. Before we go there any question regarding the basic operation and how we finally, arrived that this flip flop circuitry starting from the very basic definitions. And assumptions of course, as compared to the dynamic as compared to the flip flops where we did not have the feedback as compared to the simpler flip flop they did not have this feedback. We are having 2 additional inverters and also we are having 2 inverter at original transmission gate. So, for the point of view of clock of course, it is having twice the capacitor suppose there is a clock signal coming in ultimately clock signal is also driven by some inverter or some you know buffers. So, ultimately a clock is the digital signals going 0 and one it will be driven by some inverters and the clock over here will be going to all the different NMOS and PMOS, likewise you will have the clock bar.

So, if this is clock I can have the clock and clock bar being generated and being fed to all the different modules. In general we you like the clock and clock bar to be exactly phase opposite right. So, we would like them to be exactly 160 degree out of phase, but in general they have finite rise and fall time. So, the clock and clock bar if I look at the actual picture they will have finite rise and fall time. So, if this is clock you can have clock bar over here. And in general for logic operation the delay is defined with respect to the midpoint of the transition. So, for example, if I want to see the delay of the inverter, and I draw the 2 waveforms input and output. That is defined with respect to the midpoint. And so, if I want to cut rise the inverter output suppose this is the input waveform to the inverter, having some finite rise time is solid time. So, the inverter will have some finite delay because as we know when the input over here goes up, it will take some finite time for the NMOS to discharge it.

So, it will be discharged completely after some finite duration approximately, once again it will be leading to a down going voltage over here gradually only it will be discharged. So, it will have a slope and with respect to the midpoint of transition on the input it will have some additional delay. So, the input transitions point the midpoint of that out in output transition can be slightly away. So, this is the input of the inverter this is the output of the inverter. Of course, it is 180 degree out of phase is inverted, but because of the finite delay of the inverter, you can have some propagation delay of the inverter I can call it t delay of the inverter. So, generally we characterize the delay of the logic gates in terms of the distance between the midpoint transition.

If this is the input rising edge of the or rising it is the input of the inverter. It will the output would definitely fall as the input is going up, but it will take some finite delay because of the discharge path provided by the NMOS you have a rc time constraint and large signal operation you are having ultimately this voltage getting discharged through this inverter to this NMOS which is having some own resistance. And therefore, it is going to take some time to discharge it. And therefore, there is going to be some delay, and in order to look at the delay we have to look the look at the difference between the midpoints. And that is the way we define the delay of that inverter. So, in general when we are looking at the characterization of these flip flops they are also, likewise we have to look at the transition points and the midpoints of these transition zones to let characterize the delay.

So, before we go further let us take a short 2 minutes break, and then resume our discussion. So, before I go further and deal with the delays of these logic gates and finally, characterise the flip flop in terms of these definitions the set of time whole time and the CTPU delay let us take a 2 minute break and then resume our discussion on the characterization on the flip flop.