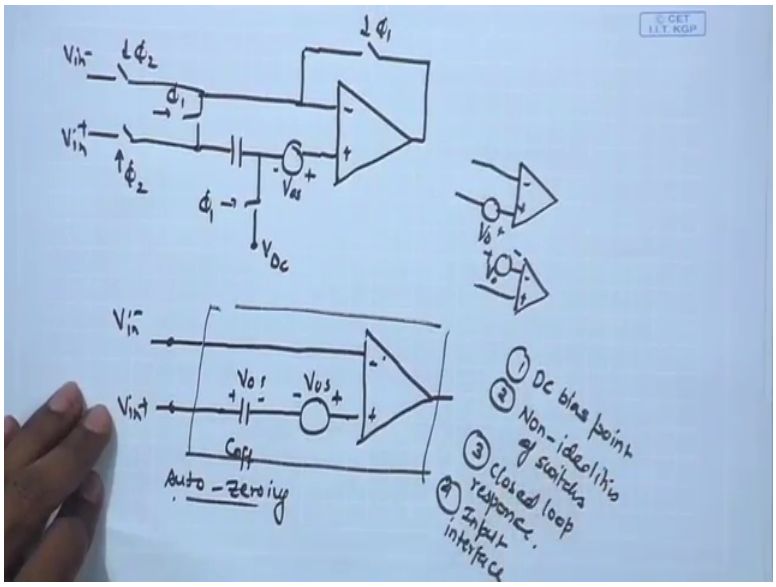
**Analog Circuits and Systems through SPICE Simulation**
**Prof. Mrigank Sharad**
**Department of Electronics and Electrical Communication Engineering**
**Indian Institute of Technology, Kharagpur**

**Lecture - 45**
**Input Interfacing With Autozeroing**

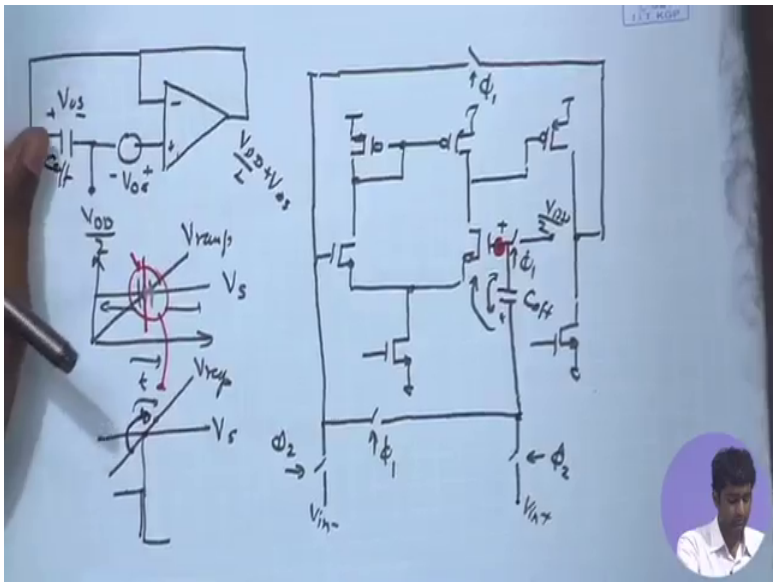
Welcome back. Let us resume our discussion on the issues with the offset cancellation circuitry.

(Refer Slide Time: 00:25)




We have discussed the DC bias point non idealities related to the switches DC. Now the other important issue is the closed loop response and the input interfacing let us look at the closed loop response which is going to be critical as we are having the closed loop operation unity gain feedback, we would like to make sure that when the loop is being closed the overall operation is stable because doing that operation if the phase margin is not sufficient, it may lead to ringing, if it is falling negative it may lead to oscillation during that period and our purpose will be lost. So, we met make sure that you have sufficient phase margin for the closed loop operation whenever the unity gain feedback is connected and then we have to see that what are the pros and cons of applying stability consideration in the closed loop.

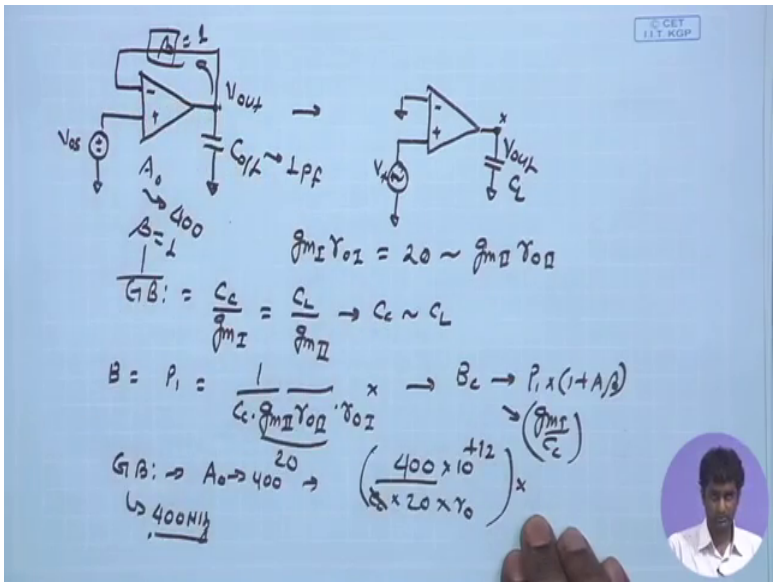
(Refer Slide Time: 01:18)




So, first need we need to identify the overall closed loop circuitries that we are having for the phi 1 phase and for that we have already this particular configuration drawn over here this is connected to V DD by 2, we have a offset voltage over here and the unity gain configuration this is C offset. So, this is the DC point this is the DC point with the point of view of AC analysis this can be seen as the AC ground. So, this is an AC ground and then you have on the top of this DC this V offset effectively applied at the positive terminal and then you have the output voltage being fed back to the negative terminal and also you have AC offset connected to the output which is appearing between the output and the V DD by 2 which is an AC ground right.

So, I can take this C offset out and I will place it here between this point and AC ground has the same effect. So, on the point of view of the phi 1 phase the C offset is effectively appearing as a load capacitance for the closed loop operation between the output and AC ground. So, because this is just a DC potential which have applied to the switch and this is just an AC ground though the C offset appear between the output of the unity gain amplifier and AC ground.

(Refer Slide Time: 02:31)




So, this is my load capacitance for the close loop operation that is the first thing. So, I can connect my C offset for the AC coolant circuit I am putting this to AC ground although it is connected to V DD by 2 absolutely and you have the C offset over here and this point you have the V offset and of course, in order to analyze the stability this is again affect to signal if I assume that it is time invariant to fix signal once again in order to apply this check the stability we will have to use the open loop operation and figure out what is the overall gain and make sure that the phase margin is sufficient.

Now, in this case of course, once again we have the output voltage being fed back to the input terminal in series therefore, at the input we have series configuration output voltage V out is being sampled and fed back to the input. So, of course, at the output we have shunt and feedback factor unity because we are just sampling the V out and the feedback signal to the negative terminal of the op-amp is just the V out as it is beta is one. So, the overall gain a of the circuit is the open loop gain of this comparator. So, a is known we have the A o which we have already set around 400 that is what we discussed last day. So, A o is known and we have the overall beta is one we are estimating that the C offset will be at least say around Pico farad it can be higher if you want better position. So, based on our discussion earlier on the sampling capacitor and its analogy with the offset sampling capacitor we are arising arriving at the estimation of the c offset.

Again in the Pico farad range to preserve millivolt accuracy for the sampled offset. So, this is the open loop gain the beta and the C offset if we if we do not change any of this parameter of course, in the circuit it may be possible to change the a node by tricking the bias current when you are going to this phase suppose we are not going for those complications we are not changing the core circuitry of this amplifier the transistors the biasing dimension none of this are changed. And therefore, this remains a not the open loop gain of this amplifier remains A naught and the C offset comes as a load capacitance what was the off role of C offset in the comparison operation during the comparison phase.

However, C offset is not coming as a load it is just in sees with the input is not any role in determining the output bandwidth of the comparator the bandwidth of the comparator will be determined by the r c time constant at the output this is just in series this is just adding of voltage it is not really coming into the higher frequency is not determining the higher frequency role of.

However in the closed loop operation we are seeing that the C offset is appearing as an effective load and this is the equivalent circuit now remember for the overall if I have to do the open loop analysis again I have to open this feedback we can apply the test signal over here and check the output over here right. So, the open loop analysis point of view we can apply the test signal V t over here and we can just put an AC ground over here because remember this is a you know series connection. So, when we open this looking into the output of the feedback network beta which is one we are having shunt connection at the output we will just put a ground over here and likewise on the other side looking into the input code of the feedback network the other is series connection will put a open circuit over there.

So, V out we put an open circuit and on the other side V in we put a ground and in order to get the loop gain is all we have to do is apply the V t and look at the V out that is the loop gain basically and now if I look at the loop gain and the corresponding bandwidth that we can get for a stable operation we know that this is sufficiently large capacitance as compared to the parasitic capacitance. So, while discussing the comparator we discuss that the overall pole it is going to be determine many by the parasitic capacitance c g d and its miller multiplication and we did not consider as significant load capacitance present, but now we have this large load capacitance present for the close loop scenario

and then we have to see what is the resulting gain bandwidth product. So, in our earlier example when we look that the open loop amplifier open loop comparator design we assume that the g m 1 r o 1 is the gain of the first stage approximately this is going to be equal to around say 20. So, that second stage is also similar and overall we are getting around 400.

So, suppose there was a starting point this is equal to g m 2 r o 2 suppose we have this configuration where g m 1 r o 1 first stage of the amplifier gain equal to second stage of amplifier gain equal to 20. So, that overall open loop gain was around 400 and also we have in the closed loop case we know that in order to have sufficient stability we have derived what is going to be the criteria for stabilizing the close loop operation the gain bandwidth product for the close loop condition depends upon the compensation capacitor and the g m the first stage. So, this is equal to c c upon g m or in other word c c upon g m 1; g m 1 of the first stage.

And also in order to have 45 degree phase margin the condition that we have discussed is should be equal to p 2 the second pole or non dominant pole which is given by the load capacitance C L divided by the g m 2 that is the g m of the starting stage and once again if I assume that all the channel lengths were similar and the bias current were similar in both the stages. So, the g m 1 r o 1; g m 2 r o 2 are going to be similar and here therefore, I am going to have g m 1 approximately equal to g m 2. And therefore, C c the compensation capacitor approximately equal to C L let us assume that C c approximately equal to C L for a 45 degree phase margin. So, we have the compensation capacitor given by the value around 1 Pico farad and we have the gain which is also known to us.

We also need to see; what is the overall bandwidth over here which we are going to get. So, the overall bandwidth in this case for the open loop condition over here which has the C L and the C c within this within the output of the first stage and second stage we know that the gain the bandwidth is given by the first pole p 1 the bandwidth is given by the first pole p 1 which is going to be equal to C c times the g m 2 r o 2 because its gets multiply by the gain of the second stage times the r o 1. So, this is the bandwidth of the amplifier for this open loop case and then I also have the overall gain which is impact intact and which is given by the g m 1 r o 1 times g m 2 r o 2 resulting in the corresponding gain bandwidth product.

Now, if we look at these numbers we have this g m 2 r o 2 which is already determine which is having around the value of 20. So, this is close to 20 and also we have the overall p 1 given by therefore, the r o times 20 times C c now we have see that given this constraint given the value of g m 1 because here we are not determining g m 1 from the stability constraint the g m 1 r o 1 came from the required gain for the open loop consideration and for that g m r o we have this quantity anyway previously determine gain bandwidth product is again getting constraint because of the required c c and for this given for this given g m r o and the required value of C c. Therefore, we need to see what is the bandwidth we are able to get in the overall open loop and hence the close look condition.

So, here we have the p 1 given by this product and the overall bandwidth which is overall gain which is given by the g m r o 1 gm 2 r o 2 to product which is just going to be g m upon C c. Now based on this we have to estimate that what is the overall gain bandwidth we are able to obtain remember the overall product we are saying is anyway 400. So, we have the gain bandwidth product already given by the open loop gain which is remaining same we are not altering it. So, we are saying the open loop gain is remaining same which is product of these 2 which is 400 and we have the overall bandwidth over here which is given by this quantity to the for the overall gain bandwidth product that we are going to get is 400 divided by the C c which is also known and the g m r o times r o 20 times r o.

And the C c value is also known to us we are saying it around 1 Pico farad. So, we have around 10 upon of minus 12 over here.

Student: (Refer Time: 12:18).

Sorry.

Student: Plus (Refer Time: 12:19).

Yes sorry. So, this is the overall gain bandwidth product that you have available from here also we have the overall value of r o which is also known because we have g m 1 r o equal to 20 from both these cases now here if we look at the overall gain bandwidth product and the corresponding say close loop gain. So, what is going to be a corresponding close loop gain if we have this gain bandwidth product and the certain

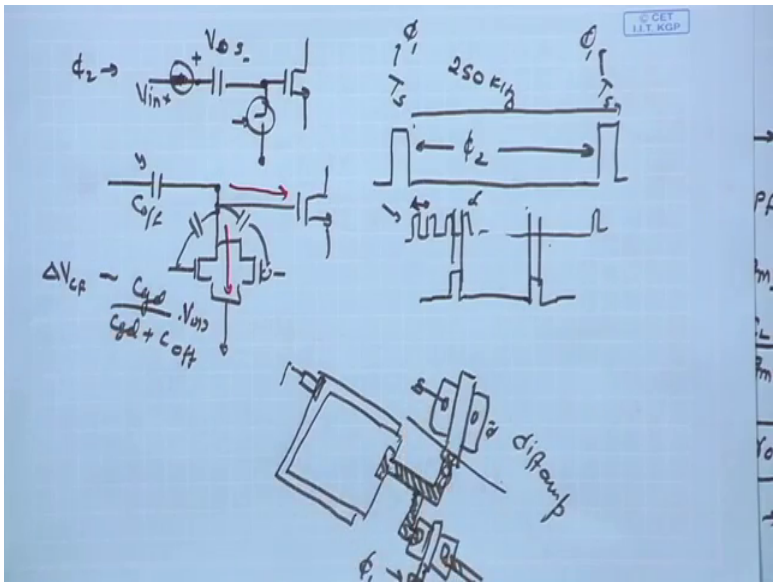
open loop gain over here? So, for the close loop gain I need to multiply this p 1 which is the open loop bandwidth with the corresponding say open loop gain 1 plus A beta; beta is 1 therefore, in order to get say the bandwidths closed; closed loop bandwidth I will multiply p 1 times 1 plus a beta; beta is anyway one therefore, just a times p 1 and therefore, this is going to be a this p 1 multiplied by the overall a which is going to be just g m 1 r o 1 g m 2 r o 2 therefore, the closed loop bandwidth that we are going to obtain from here.

It is once again going to be just g m 1 upon C c right. So, you have the p 1 times the this is the open loop bandwidth times one plus a beta where this is just a and then a time this quantity just going to once again give me g m 1 upon C c which is nothing else, but I am sorry I have you know just. So, this is one upon g b g m 1 upon C c; this is nothing else, but my g m gain bandwidth product. So, the close loop bandwidth in fact, in this case equal to the gain bandwidth product provided by the open loop amplifier and I have to make I have to see whether this close loop bandwidth if we are getting which is equal to the gain bandwidth product is sufficient.

So, that we can operate this close loop operation fast enough by our clocking scheme now since our gain bandwidth product we have chosen is around 400 mega hertz if you remember the discussion this is around 400 mega hertz our overall close loop bandwidth that we are getting this p 1 times the one plus a beta. So, almost equal to this and therefore, may not really be very significant or you know may not have a serious constraint with respect to the offset cancellation loop.

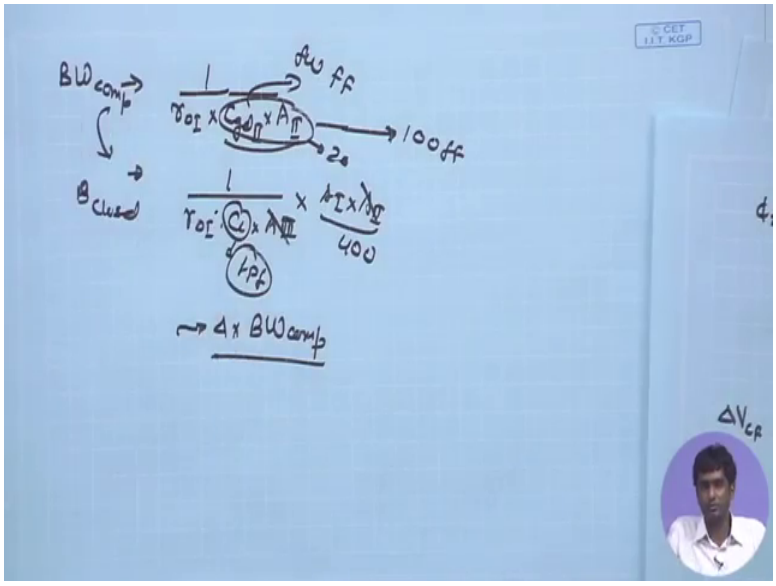
Now, that would imply that for the overall closed loop operation I do not have to worry about the speed of the closed loop operation and remember the clock frequency that we have chosen for the overall the counter operation this was around 250 kilo hertz.

(Refer Slide Time: 15:30)




And or other this sampling period was 250 kilo hertz and we chose the a clock frequency three four time larger is around one mega hertz and here the gain bandwidth product is you know sufficiently large very large as a result the overall closed loop operation is not going to have serious bandwidth limitation if you; however, if you if you look at if you look at the C c value; however, of course, as compared to our original bandwidth that we have.

(Refer Slide Time: 16:18)



If you look at the original bandwidth in the comparator what was that equal to the comparator bandwidth if I do it on a separate sheet the comparator bandwidth I call it bandwidth comparator which is going to be equal to the open loop case where the overall pole was determined by the miller multiplied parasitic capacitance.

And that I can write it as r o 1 which is r o the first stage times the C g d of the second stage C g d 2 times the gain of the second stage which is A 2 which is around 20. So, this was the bandwidth of the open loop comparator in the in the closed loop we are having the same r o 1 almost we are not changed any parameter. So, you have this same r o 1 coming over here rather than the c g d 2 times A 2 we have the capacitor value given as C c times A 2 right. So, right now we have the miller multiplication of C c which is much larger. So, from this point of view also we can see if you look at the open loop bandwidth we have r o times C c times A 2 here this value C g d what is a value of C g 2 approximately this can be add the max say few femto farad few tons of femto farad because this is the parasitic capacitance of the p mos input devices in next stage remember how does it come into picture.

So, miller multiplication is happening because of C g d of the input p mos device of the second stage and that me again few femto farads and this is 20 and this is few femto farad few I would say femto farad and as a result this is this capacitance is approximately this total capacitance approximately going to be hundred femto farad here this value we have chosen 1 Pico farad right. So, of course, the capacitance has gone up by ten as a result if I am looking at the open loop bandwidth as compared to that the open loop bandwidth of this voltage follower definitely is lower by this factor of say hundred, but apart from that we also have the overall gain right. So, this is the open loop bandwidth given by the first pole and the a miller multiplied C c the composition capacitor this multiplied by the one plus a beta factor once again if I look at it you are having a beta approximately equal to a which is A 1 times A 2 a 2. So, you are having A 1 times A 2 where A 2 gets cancelled and therefore, the bandwidth closed loop I will say bandwidth closed loop is going to be A 1 times this number. So, you are going to have A 1 A 2 times this number.

Therefore this is having A 1 upon hundred factor as compared to this and A 1 A 2 we remember around 400. So, 4-5 times larger than the original bandwidth you had for the comparator therefore, in this particular case for the chosen value of C c, we are saying

that the closed loop bandwidth may be this is this number is around 400 and as compared with this we are getting four times the bandwidth of the comparator. So, this is the bandwidth of the let me call it bandwidth of the comparator. So, at least as per these numbers we see that the closed loop bandwidth if we are getting for the voltage for our operation it is higher than the original bandwidth of the comparator that we started with and therefore, in this closed loop operation we may not really be concerned with the settling time or the speed response of this loop.

However if suppose we go for larger c off where you know we are having larger precision requirement and for be affords to use larger c off there of course, once we can see that the C c and hence the c off becomes larger and larger as compared to the C g d then this ration will be detoriating and it can go down also as compared to the present value. So, as we go on increasing the C offset requirement for larger and larger precision it would imply that we need a larger C c because remember the constraint g m which is A 1 g m equal to C L upon g m 2 and that would mandate a larger value of the compensation capacitor and hence it will reduce the closed loop bandwidth you are getting from the compensation. So, of course, that trade off is always going to be there.

Also another thing is the gain. So, if you are having a higher precision requirement in the comparator remember how do we determine the gain that was coming from the precision requirement in this case we have 400, but in case you are having larger gain requirement rather than 400 you are having 2000 then of course, again you will have the overall bandwidth for the closed loop operation getting limited so; however, in this case if we are looking for 7 bit precision corresponding to that we are arriving at the C offset around 1 Pico farad and original gain was say 400 based on these numbers what we are seeing is that for our design examples this is constraint is you know we are very much within the limit for the closed loop operation of the unity gain feedback.

But this is not the generalized case this is only for our specification if you have other specification o the gain of the comparator being high rather than 400 being much larger or the offset C offset being high that would have different ratio and that can make the overall closed loop bandwidth for the unity gain feedback lower than the comparator bandwidth. So, if that happens what will be the constraint? So, if as of now it seems like you know we can go to our original way form and our comparator can operate faster that this clock that is how we have designed.

So, within 1 clock period we can settle nicely the closed loop bandwidth for the unity gain feedback if we also even for the larger. Therefore, within 1 clock duration it can do the offset calibration it can store the offset value across the C offset that is we are concluding. So, just one clock pulse is good enough for storing the C offset and then rest of the time can be given for the normal comparison operation ramping and so on.

As of now that is the conclusion, because the closed loop operation the phi 1 phase can operate even faster that the open loop comparator that we have and within one phi it can within one clock period it can complete the sampling of the offset voltage if it. So, happened that the closed loop bandwidth over here felt significantly lower than the open loop then the solution would be to either increase the bandwidth over here or you could just apply relatively larger number of pulse rather than doing the offset calibration only pulse and rather than applying phi 1 equal to just one clock period you go for larger number of clock pulses for phi 1 that also of course, matches some pulses from your normal comparator operation, but rather than going and increasing a bandwidth of this comparator and burning more current it would be more prudent probably to still some pulses from the overall operation and apply more number of pulses over here for the phi 1 phase.

So, you can see that how the circuit operation or the circuit level results can impact our control scheme when to apply the phi 1 pulse how many phi 1 pulses to apply and then accordingly what is the digital control scheme. So, all these things get link together very tightly. So, if you are messing at some certain application sir circuit implications or mattresses by making this amplifier faster for the closed loop feedback we may be dissipating more power over there or may be making the design more complicated. So, rather than that is your option will be let us use more number of clock pulses for the phi 1 phase so that I can even deal with the case where the closed loop bandwidth is following lower than the actual amplifier the amply the actual comparator bandwidth.

Another interesting point over here that we can also discuss this is an additional point that would just like to mention. So, far in the comparator operation also if you remember the normal comparator operation we have assume that within one clock pulse it should complete the operation and it should be sufficiently fast for that the comparator output settles within one clock pulse if the V ref is or if the V in ramping V ref was I am really

go back to this float is the ramping V ref is crossing the V s just at the next positive edge of the clock the comparator should be giving the right result.

But our original comparator also has a larger delay it is slower than the original clock what will be the result for that is it going to have drastic impact or the impact is less serious can be tackle in some other way. So, can we afford a slower comparator in our design example the comparator speed is not. So, critical because still we are dealing with 7 bit resolution, but if you go for larger and larger resolution where you have a eight bit ten bit twelve bit coming in then you can imagine what is going to be the requirement of the speed for the comparator and in that case can we afford to keep our comparator slower than the clock pulse we can think about it we can discuss this point later what will happen if the comparator is four time slower than this clock what is the result of that is it going to have a significant effect on the overall response specially in our architecture when we are using 2 comparators to cater to the required input swing what is the result if the comparator happens to be slower than this clock.

What is its impact on the overall a DC characteristics there is a nice question you can think about it and we can discuss its implication for the that that just an assign. So, let us not digress from our discussion on the offset cancellation do since we discuss about the delay of the closed loop operation of this op-amp and try to see whether it is able to you know perform well with the given design mattresses that we have for the open loop comparator we also briefly discuss, but happens if your original comparator open loop comparator is slower than the clock frequency. So, we probably we discuss this issue also later for the time being let us focus on the closed loop operation and we have just seen that for the 7 bit precision and expect that we started with for our comparator we are in a safe position the closed loop bandwidth is very much within single clock or is significantly higher in fact, than the clock frequency that we are using in the system.

So, a just single clock pulses good enough for our offset sampling. So, summarizing we have the closed loop operation where the C offset is appearing as a load capacitance for the closed loop operation there once again we need to look at the open loop and find out the open loop gain from the input to output and there once again we have the g m r o product determine already from the open loop amply comparator design where assuming each of them 20. And therefore, the gain bandwidth product that comes as g m 1 upon C c and g m 2 upon C c there we have the g m 1 g m 2 r o 1 r o 2 determine from the

previous constraint C c and C L are getting determined by the constraint on the sampling capacitor we want to be sufficiently higher. So, that leakage and other non idealities do not affect it that is determining a large magnitude for the C L and hence C c for 45 degree phase margin once the C c is known we know the bandwidth is going to be determine by the C c and g m r o of the first stage.

But we also have that when the closed loop ultimately we are having this one plus a beta factor coming in and then we put the right number that we already have a not value which is not changing for the overall amplifier is remaining unchanged. So, that number we already have and based on that we are trying to estimate that based on that we are trying to estimate what is the resulting bandwidth.

So, where we also looked into the bandwidth of the comparator open loop case which was equal to determine by the first stage primarily because there was no load capacitance load capacitance is very small and we assume that the bandwidth of the open loop comparator was being determined by the first stage differential amplifier output r o 1 sorry output resistance r o 1 and the overall capacitance given by the C g d of second stage in the a and that gives us an estimate that you having a total capacitance hundred femto farad corresponding to that I can see what is the overall pole coming.

Likewise in the closed loop case we are having the overall capacitance coming at the first stage only which is equal to C c times A 2 and once again the same r o 1 and we just compare these 2 and we are concluding that this ration this is sufficiently larger 4-5 times larger as compared to the open loop bandwidth of our original comparator and concluding that yes this is good enough and it is fast enough as compared to the open loop operation and it can do the offset sampling within a single clock pulse of our a DC. And then we discuss the case whether it does go down goes down become smaller than this then what is the implication and how to handle that by modifying the control in the offset cancellation loop and by applying relatively rather than just one rather than having using more number of this clock pulses for the offset cancellation.

I hope this point how do we determine the bandwidth in the comparator case that was clear because there what we had assumed was that there is no additional load capacitance there is no significant load capacitance coming here it may be just driving AC mos inverter therefore, C L is small just parasitic capacitance of the gate whereas, in the

second stage you are having C g d which miller multiplies and provides a larger load capacitance over here the and that I assume that to be the dominant pole and hence estimated the bandwidth based on that node and then I compared it with the closed loop. So, this is just the cross check on our assumption.

So, we can take a short break and then resume our discussion on the remaining point that is input interfacing with the offset cancellation circuitry how are we going to apply the 2 input the ramping circuit and rand ramping input and the sampled input voltage to our comparator along with this offset cancellation unit what is going to be the best way, and how are we going to place the sampling capacitor which is sampling the input data we are going to look into that next.