**Analog Circuits and Systems through SPICE Simulation**
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**Lecture - 44**
**Compensation During Offset Sampling**

Welcome back. Let us resume our discussion on the offset cancellation circuit that we started with before we go for that any other questions in the discussion that we have.

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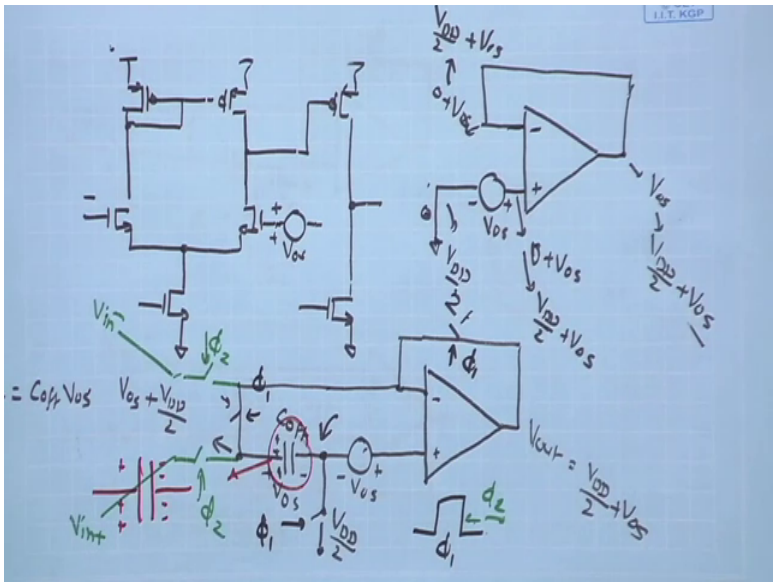


So, we looked into once again the negative feedback operation how the amplifier it is able to follow the signal at the positive terminal.

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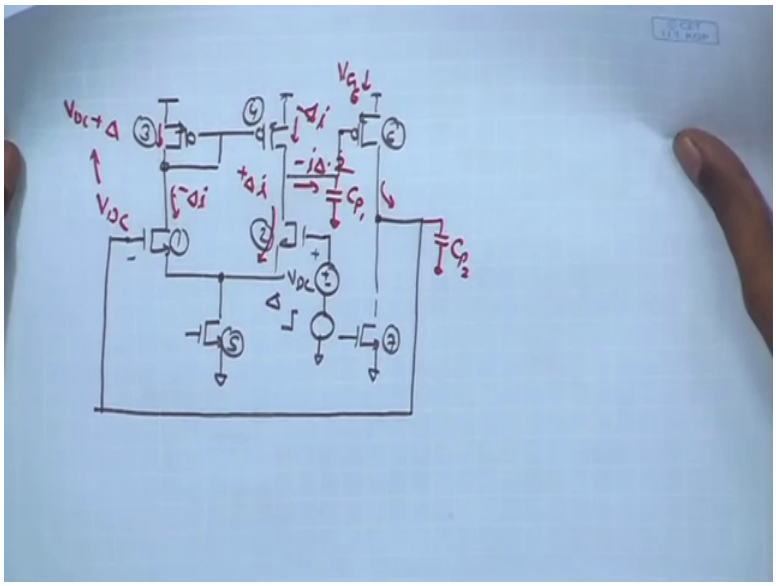

And then we looked into the basic mechanism for the offset cancellation that we can apply to our comparator circuit.

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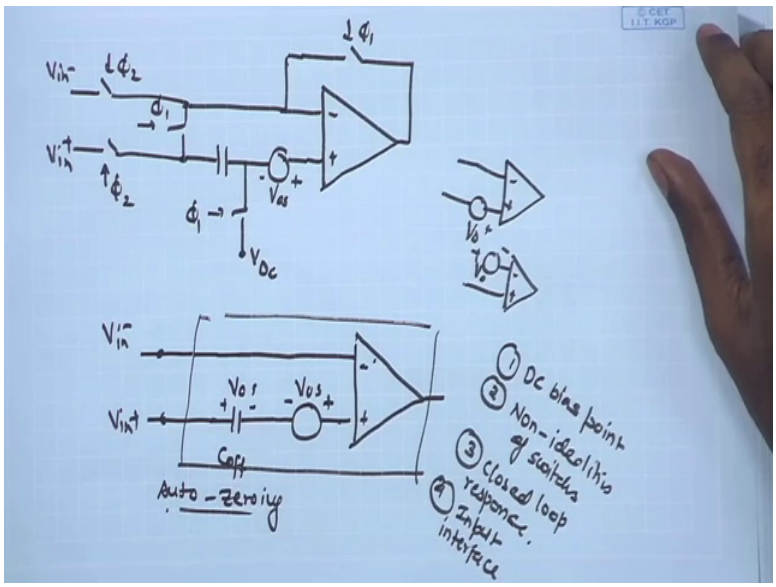


Now, let us going to the circuit issues that must be addressed to implement this operation in other if the comparator that we have designed for our a DC operation. For that there are several issue that we need to look at.

First of all for the overall operation we need to make sure that the DC bias point is intact. So, we need to see the DC bias point we need to see the non-idealities of the switches,

we have already discuss the non idealities of switches in significant detail. So, once again their implications have to be considered here and we also need to look at the closed loop response and finally, if I ultimately you have to apply this operation on my circuit, I need to look at the input interfacing. What manner I am going to apply my input which is coming either from the ram circuit or the sampled analog voltage to this offset cancelled amplifier or comparator. These are the four things we can discuss step by step and look into the circuit issues related to these.

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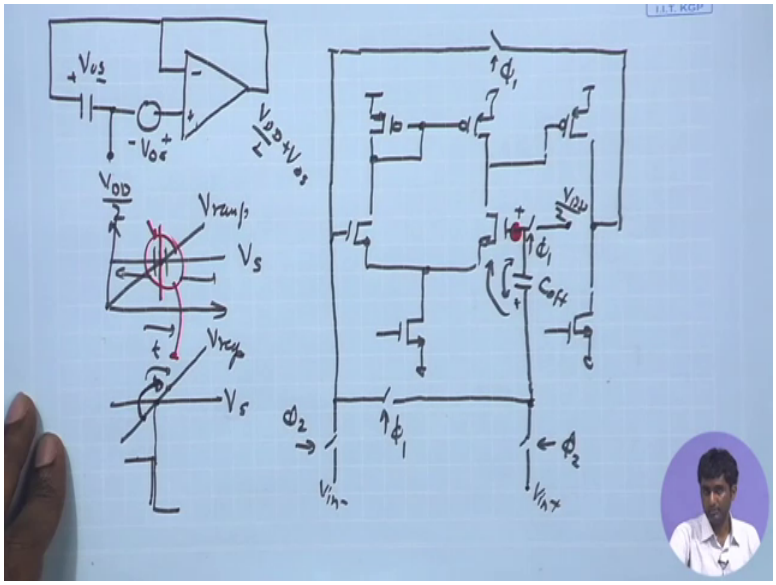


So, first question we would like to now discuss is the DC bias point what is happening to the DC bias point of this amplifier when we are disconnecting the closed loop then we are disconnecting this phi 1 switches. Remember for the phi 1 phase we have the overall operation which can be given as voltage follow a you have the V o s and at this terminal you have the you have a Vc which may be V d d by 2 nominal value say V d d by 2 and as a result you are storing the V o s over here. So, if I look at the corresponding circuit implementation what are we trying to do. So, let us try to implement this using transistor level circuit and try to see where are we going to place these switches. So, if I draw that on my transistor level circuit for the comparator. So, this is our positive input and we are connecting the first switch at the positive input which is suppose to connect this V d d by 2 say.

So, we can have one transmission gate base switch that we have discussed in our previous classes, and this point can be V d d by 2 you can obtain it through some reference generation circuit or simply by dividers if we ignore the issues related to that right now. Now here we have of course, a phase phi 1 coming in and also you know just to keep the track we can enter that V offset over here. So, let this red dot be the V offset the offset voltage that we have and we also have the capacitor which is supposed to be connected between the terminal over here. So, this is our c offset which is once again suppose to be connected to the inverting terminal, while the inverting terminal is in the negative feedback configuration this is also driven by phi 1 phase and finally, the output once again should be connected to this point. So, you have another switch coming over here which is also driven by phi 1 phase.

So, this is these are the three switches driven by the phi 1 pulse and then we also have the other 2 switches driven by the phi 2 pulse. So, this is what we have. So, we have the V iv in plus and V in minus. And once again if I recall my overall operation that we discussed for the offset cancellation what is have when we have phi 1 phase of on in this is the equivalent circuit and we have a V d d by 2 point over here. So, this point is bias at V d d by 2 and as a result this point is going to V d d by 2 plus V offset. So, if I assume that V offset is bad around 50 millivolt of V offset is happening, then we have V d d by 2 sorry say 0.9 plus 50 millivolt coming over here. So, still both are demand pretty close together in terms of DC 900 millivolt and 950 millivolt.

But in the next phase when phi 1 is getting off and phi 2 is getting on we said that this node is become floating and it does not have any indirect connection with any of the DC sources; and that is basically helping us in preserving the offset voltage across this capacitor the c offset that is preserving the charge trapped across the c offset. Now of course, if we look at the input side we are connecting the input to V in plus and therefore, in the phi 2 phase as I said we are going to have the V in plus appearing at this particular input connected to the say positive terminal of this capacitor and as a result since we have trapped the charge across this c offset the potential over here will be jumping to V in plus minus V offset right. So, whenever we connect the phi 2 switches this potential is V in plus, the phi 1 switches turning off as a result the potential over here must be equal to the V in plus the potential drop across the capacitor in this direction and in this

direction what is the potential of across the capacitor we have seen minus V offset because plus minus in this direction.

So, V in plus minus V offset appears over here and therefore, as long as this is connected to V in this will be V in minus that V offset and if V in plus is having a sufficient DC level therefore, this automatically is carrying that DC level plus the V offset minus V offset quantity. So, DC of course, cannot pass to the capacitor, but because of the charge stored across the capacitor it can always provide the step in the voltage. So, when we are connecting this positive terminal of the capacitor 2 V in plus, because of the charge locked in this capacitor you are going to have this V in plus plus that V c coming in series, and then you are going to automatically have the V in plus minus V offset coming as the DC potential here. Likewise on the other gate we anyway have V in minus which is also having its own DC depending upon what is a signal level whether it is V ramp or whether it is sampled signal, it will have certain DC this will have certain DC and therefore, we are not going for any dedicated biasing circuitry for the input for the comparison phase.

When the phi 2 is on the amplifier is operating in the comparison mode this is open there is no feedback in this normal comparator, 2 input being applied to the gates of the comparator and ultimately we have to just compare the absolute values. And we have to just make sure that the values are within the input common mode range of the comparator as we have discussed. So, as long as the input voltage V in is within the input common mode range of this comparator, we just we are just concerned with the trip point when the V ref approaches this sampled V in another that condition anyway the DC bias point will be proper provided by the sampled V in over here, and the ramping voltage over here; this is clear any question.

So, this relates to the DC bias we are not biasing the input for any DC of course, we have discussed that in a comparator operation we did not be concerned about biasing the output also, because ultimately we are concerned with only high or low levels. So, for the differential amplifier operation in the front end we have discuss the common mode feedback and we have discussed couple of strategies stabilization techniques, but here we are not even considering the output DC point, and because the output will not be stable at one DC bias point it is going to be non-linear operation there is V d d either the output is supposed to be close to V d d or ground. So, wherever input signal is sampled and this is

at certain value V sample in the ramping voltage is rising this your V ramp on the capacitor. We must make sure that in the vicinity of this time where you have the V ramp approaching V s the gain is sufficient and it is able to amplify the signal sufficiently.

And under that condition of course, if I assume that the transistors over here are remaining in saturation whether still get good gain; however, if we are not ensuring an appropriate DC bias point we will discuss that little later when you come back to the role of the DC bias point at the output of the comparator, that not only relates to the offset compensation and also relates to in general the biasing of the single ended comparator and the resolution of the single ended comparator.

So, we will get back to this point of biasing the output; what we are right now saying is that for the comparator output we are mainly concerned with the output level going high or low. So, in this entire region the output will be high or low V d d or ground therefore, we did not consider the saturation region operation and a credit DC bias point for this one. All we want is as soon as V ramp approaches V s all the transistors should be in saturation so, that the decision regarding the transition should be taken at the right time step.

It should go up the transition should happen at the right time instance that is going to give me the correct digital value. For that I should make sure that the gain in this region is sufficient so, that whenever the difference if I magnify this you know little bit. So, whenever the difference between the sample voltage and V ramp is changing the polarity is coming from negative to positive the comparator should be able to change the polarity within a very short time, and that would imply that at this particular junction the gain of the amplifier should be sufficient. So, that whenever there is a delta V a small change in the polarity of V s minus V ref the amplifier should be able to detect it, and flip the polarity that is the only purpose. If you are far away from this region here or here definitely the output is close to V d d or ground, these are going to been triode region either this is going to be in triode region when the output is V d d or this is going to be in triode region when the output is ground. So, for those regions we doing it worry.

However let us see the case where even in this region when the input is approaching the V ramp is approaching the V s and 2 are almost similar, even in the that condition of course, we cannot guarantee that this will be close to V d d by 2 and this to be in

saturation. If they are not in saturation suppose the output is very close to V d d or you know it is remaining close to V d d even when these 2 signals are very close together. So, in that case of course, it will. So, when the signal approaches over here it will take longer time and unless V ref becomes sufficiently larger than V f it will not be able to pull the output down, because to begin with the output was very close to V d d and even when these 2 became almost similar the output remain close to V d d.

So, unless the V ref progresses sufficiently beyond V s it will not be able to pull it down. So, that effect is also captured in the form of offset voltage; that what is the minimum difference in the V s V ref and V s required so, that the output you know flips. So, that effect is also indirectly getting captured in the offset voltage if you consider. This because what is the offset voltage offset voltage is point where if you are having the 2 inputs if you are having the voltage for a configuration your seeing that 2 inputs are almost in the similar point or you are trying to see what is the you know minimum 2 voltage that you can apply at the positive terminal. So, that the output is you know close to say V d d by 2. That is what we are looking at and therefore, that difference or that voltage has been anyway stored across the c offset. So, that is also having the effect of the uncertainty in the output stages captured in V offset.

So, need did not worry about this at this point, what we are saying is this offset voltage is going to take care this offset voltage stored across c offset is going to take care of the not only the mismatch of the first stage, but also the deviation of the DC bias point over here, when both the inputs are close together. Because when the both the inputs are close together we need in this V in plus plus this voltage drop, to make sure that the output is V d d by 2. So, that is already stored that is in fact, capturing the effect of uncertainty in the output point. So, that is in a way ensuring that the amplifier will being high gain condition when the V ref approaches other the V ramp approaches V s that is another certain point that you can you can think of.

So, output DC point we did not worry about it in this case is it clear. Input DC point definitely we can based on the capacitors stored charged in the V in we can say that this is just, going to have a jump this is V in this is going to be V in minus V offset. The movement you apply V in over here this voltage is clammed across the capacitor V in minus V offset plus V offset therefore, that is well settled also what I am where I am claiming is that the output DC point is also going to be well defined as V ramp equals to

V s a exactly equal to V s at that point we whatever mismatch effect was there it is already been captured in this c offset. This is clear; regarding the DC bias of the input point and the output point of the comparator. Of course, the other important issue that we need to take care of is the non-idealities of these switches. So, we are concerned with tracking the offset voltage and sampling it across c offset, and the magnitudes can be may be few millivolt all the way to few tons of millivolts.

And we would like to preserve that accuracy, and the offset voltages stored across this c offset not get corrupted because of the leakage to the switches. So, for example, when the phi 2 mode is active we have the switch over here which is off right.

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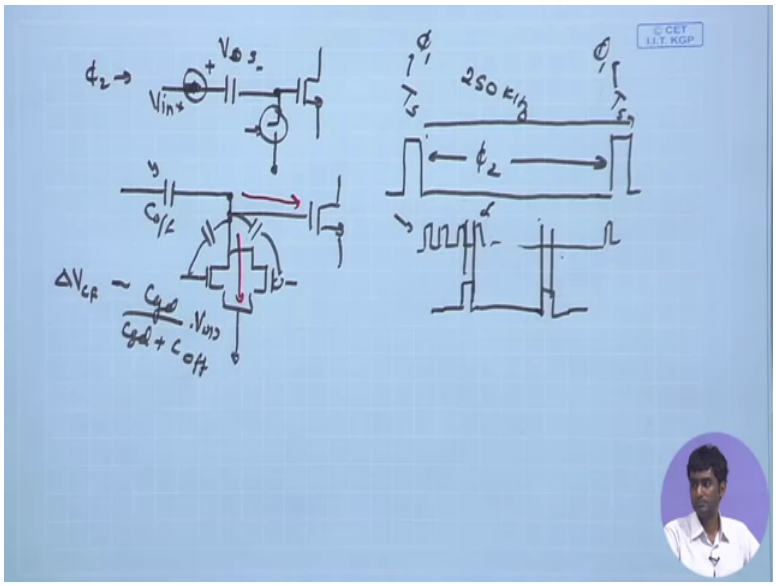


And you have the input signal applied to the c offset. In the phi 2 phase what is the condition of this switch this capacitor? You have the V offset stored over here and you have the switch which is connecting this to input. So, V in plus is connected to the capacitor and at the other side you have this switch driven by the phi 1 phase which is closed. So, here this can be shorted they can say this is the phi 1 or the phi 2 phase where this input is connected to the positive of the capacitor.

However the phi 1 switch is off and then you also have the gate of the mosfet where it is connected. So, of course, we are going to implement these switches is using transmission gates both these switches are going to be implemented during transmission gates, and we have seen that transmission gates do end up dumping unwanted charges at the sampling

points. So, at this point since is the trapped load we do not have any path for this charge to go at this particular point when this switches getting on anyway it is sampling the or passing the input voltage and its connecting this particular terminal to the input voltage therefore, even if it is injecting some charge over here this is ultimately shorted to V in plus it, it is connected from a effective source switches applying that V in plus which is immediately coming from previous stage or stored voltage in the capacitor.

So, this is connected from a source stable source therefore, this switch after getting close if it is injecting some charge it does not matter because ultimately this is going to be sung by the source effectively; however, this switch getting off of course, that is going to inject charges on this point and then once again we have the effect of clock feed through and charged injection coming into picture and we must make sure that if I look at if I remember the bigger picture. You have these 2 transistors n mos and p mos implementing this switch, and I must make sure that the overall capacitances the parasitic capacitance contributed by these transistors they are much smaller as compare to the c offset. So, that the floating node over here does not experience in accuracy does not increase or decrease this voltage, because of the dumped charges arising from clock feed through and charge injection from these switches.

So, once again that will that would require certain sizing. So, remember the sizing consideration where we have the delta V pro because of clock feed through coming as c g b upon c g d plus c offset in this case times the delta V clock we can call it say V d d; and we remember that we must make sure that the c g d is sufficiently small as compare to c offset. So, this is few femto farad, in order to preserve millivolt of accuracy I would like this to be few pico farad. So, if we use minimum size transistors c mos technology one tiano meter, this can be close to 1 femto farad and that case at least this tell me that I should have at least say 100 femto farad to few pico farad of capacitance for the offset capacitor. So, this is first concern and of course, the second concern is stability of the offset voltage in presence of leakage. So, of course, we know that this is not a ideal switch we have the leakage paths through this switch and also you may have gate leakage this mosfet which is going to disturb the total charge stored over here. Ideally if the total star charge store at this point; that means, clammed then only we are having a fit full storage of offset voltage across this, but if that charge dissipates it has path to

dissipate then of course, that stored voltage will diminish or change with time, and it will not give us you know correct subtraction from the applied input.

So, once again this capacitor should be sufficiently large. So, that the effect of leakage is small and over that time when this phi 1 phase phi 2 phase is opened the voltage the charged stored across here is not getting dissipated because of the off resistance of these switches and the gate leakage etcetera. So, once again we have done this analysis we tried to see that for a given off resistance in the c mos technology, how to estimate the c offset and then again we had at least few pico farad c offset coming into picture.

So, once again assume that you have going to require around a pico farad of capacitor just to make sure that leakage is not disturbing this stored voltage, and we are able to preserve this for the entire duration of the processing. Now of course, the duration of a processing or the duration of the refresh is going to be another important question before we determine what is the size of the capacitor. So, remember the operation that we have overall for the comparator. So, we have this sampling pulses T sample which are approximately getting on periodically with the required sampling rate, we discuss the sampling frequency was around to 250 kilo hertz for 7 bit digitization.

So, the clock that we are having it is going to have at least one twenty seven pulses between the 2 rising agent that is going to give us 127 levels or 7 bit contestation that was the design decision that we made in the beginning. Now where can we apply this offset storage where we can apply this phi 1 phase and the phi 2 phase that even important design decision, one possibility is that we apply the phi 1 phase align with T s. So, we can use T s or the phi 1 phase.

So, during this T s phase when the comparator is not operating, I can use the phi 1 switches to store the offset voltage across the c offset and in between we have the phi 2 phase this is basically the phi 2 phase. So, in that case the r c time constant once again is going to be similar to, but we had for the sampling capacitor. So, for the sampling whatever considerations we made considering the off resistance of the of the switch and the overall leakage current to those switches it is going to apply as it is here. This was the overall leakage resistance or the leakage current is going to similar in magnitude if I am using minimum size devices over here and based on that we will again estimate that this c offset should be closed to that sampling capacitor that we had is few picofarad.

And of course, if we add all other effects are charged injection in accuracy the clock feed through in accuracy and then add of these on idealities and estimate what is the value it may be at least around pico farad value required for this c offset this close to the sampling capacitor and the other option is of course, that we can do it intermittently we can use smaller capacitor may be 100 femto farad and you can do the refresh the phi 1 operation intermittently.

But that would require more complicated control on the digital part and also in the analog part will have to make sure that there is a there are certain regions say within the clocking duration where the comparator cannot be used. So, possibly when this clock for the counter is going down even of these phases, we can use the offset sampling operation, and turn the phi 2 switches turn the phi 1 switches on and again from the next sizing edge of the clock we can again turn it off and then we will have to make sure the comparator output is only being used say either in this positive phase of the clock or the down going edge of the clock.

So, the timing control becomes more complicated if we are going for intermediator refreshing of the offset voltage across the c offset. You have to make sure that in between you break the normal comparison operation, we break the normal comparison operation and reserve to offset sampling and immediately after that once the offset voltage has been sampled again, again reconnect to the input to the 2 point. So, that would definitely we can see that we are going to have some more timing signals coming in; other than simple clock you need to rep have another timing signal which is going to tell you when to disconnect the offset loop, and when to you know connected back for the normal comparator operation.

So, 1 pico farad as I say means here it is not a very serious limit because we have seen the major capacitance is coming from the ramping circuitry, because for that for that circuitry for robustness purposes we have kept the current magnitude at least around 100 nano ampere or point one microampere, and that gave us a maximum amount of capacitance around 10 2 pico farad.

So, as compared to that the overhead here will be relatively small therefore, if I look at the overall design whatever we have as of now, this not contributing the huge amount of areas compared to the bigger capacitor that we have, but if it is becoming very area

critical and saving every micrometer square as important, then definitely we can go for options where you can minimize the areas because of these capacitors and in those cases only thing you need to do is you need to have a little bit more sophisticated digital control which is going to help you implementing the appropriate timing pulses any oth any question related to this this kind this is simple than a we are just looking at the non availabilities of the switches and trying to recall our discussion that we have for the sampling switch any issues.

Student: Sir.

Yes.

Student: What about the effect of charging in charge injection effect of the other switch?

As I said the other switch over here when it gets say opened for the sampling the input voltage, there anyway it is you know connecting when it is getting open it will absorbing charge and as a result of course, it will extract some charge from this point, but under that condition it is ultimately going to this deploy the V in it is a V in is getting connected to this particular node and therefore, during the turning on phase even though it is extracting some charge to form it channel both n mos and p mos of this gate, but we have a source over here which is supplying V in. So, ultimately this node will be charging to V in when; however, it is turning off when this turn switch turns off there also this node is not floating node; because in that phase if we see you have this node connected to the feedback loop and going here. So, output over here is controlled by the output voltage of the amplifier.

Only if it is of floating node then that stored charge injected by the switches will be playing role, whenever it is having connection to the other circuitry which are controlling that voltage then of course, the additional charge will be taking care it will be getting absorbed in the amplifier. So, both when it is getting on and off it will not be causing trouble.

Student: Sir, what is the prominal equate there to not there switch of the V d d by 2.

Then what is the signal over here signal is V d d by 2 you do not have anything it is DC potential there is no signal.

Student: DC potential then we have to be only signal, then it will.

No then the charge across the capacitor is not constant you have dissipated the charge those if V ref is floating then only the charge is locked over here and then you have the you know overall charge trapped. And the voltage is drop if you connected to V d d by 2 then there is charge is gone. Let us lake a short break and then resume our discussion on the details of the circuit design.