Analog Circuits and Systems through SPICE Simulation
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Lecture - 43
Offset Cancellation Scheme

Welcome back. Let us resume our discussion on offset of the comparator and the certain techniques for mitigating the offset. Yesterday we started with the discussion on the offset in a differential amplifier.

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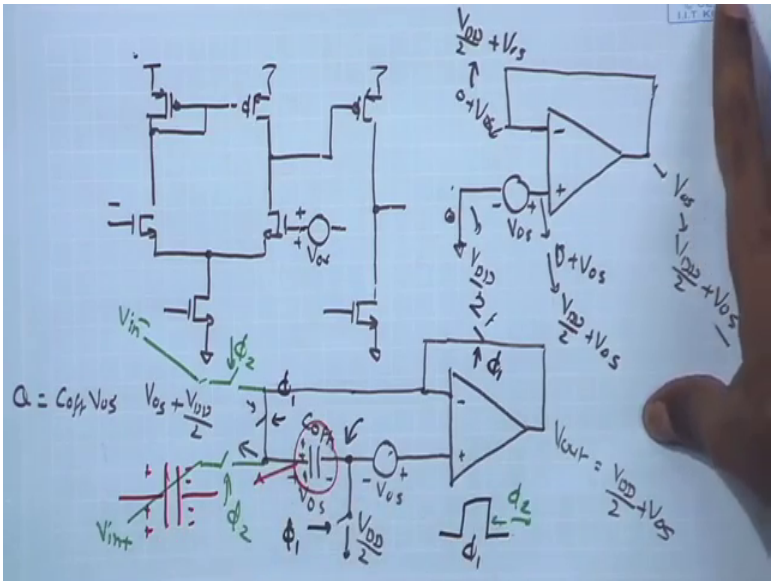

And discuss the origin of offset and how to model it. We discuss the concept of input referred offset. In our case we are looking at deferential input and single unit output comparator. So, we have a output which is single ended, and we have the positive and negative terminals. We discuss the sources of mismatch in the transistors, how process variation can lead to mismatch in the transistor pairs, load pairs as well as input pairs, and how we can figure out the overall effect of that mismatch. Now here if we look at the overall scheme and try to see: what can be the process through which we can mitigate the effect of offset in the comparator. And hence on the overall ADC transfer characteristics.

If you remember yesterday we discussed how the offset of the 2 comparator that we are using, the NMOS input device and the PMOS input device is going to impact the overall ADC transfer characteristics. And we notice that, if the resolution requirement of the

ADC is even higher may be rather than 7 bit you are going for 8 bit or 9 bit higher number of bits. The resolution dictates or mandates that the offset must be addressed. If you have few tons of millivolts offset coming over here, it would it would corrupt lot of LSBs or you know, you know what is the corruption in the data or error in the data will correspond to large number of LSBs.

So, we would like to mitigate this offset using appropriate circuit techniques. And look at the overall details of the circuit implementation. So, first we can look at the block level concept that is going to be useful for mitigating offset. And then we will go deeper into the circuit level implementation, the associated issues and try to see whether the overall requirement for the offset cancellation scheme is being met within our circuit constraints.

So, as we have done earlier we can start with say assigning an offset voltage over here. So, suppose we extract the offset voltage from the comparator, whatever is the effect of mismatch in the input pair slow devices be extracted, in the form of an effective offset voltage applied at the gate the MOSFET and then we are left with the ideal amplifier, then we have completely matched NMOS pair and fully matched PMOS pairs. And then based on this we need to look at the overall circuit scheme which can help us mitigating this offset.

So, let us now look at the block level implementation of the offset cancellation scheme, where I have the in non inverting terminal I have applied in offset voltage V offset in cop keep the polarity as such definition of V offset is the direction I have taken in plus minus in this direction. And I have the other terminal the negative terminal as it is. So, this is the ideal amplifier constituent of the transistors on define that we have over here, it is having single ended output. Now the mean concept involved in the offset is to first of all extract the effective offset voltage of the amplifier.

So, if we for example, close this loop and construct the unity gain feedback amplifier, what is the voltage we expect over here? If I said these 2 say ground or AC ground basically, suppose I set it to an AC ground in that case we have 0 over here and this point is 0 plus V offset. And of course, if this is having sufficiently high gain the amplifier will make sure that this point is also coming as 0 plus V offset. Therefore, the output point is V offset, output is having the signal V offset. And of course, the definition you know another definition of offset voltage is the required voltage at the input, which is going to

make sure that the offset the output turns to 0 or you know, the mid value. For example, if I apply a minus V offset input over here then the minus V offset plus V offset will be coming 0 and then the effective potential over here will be 0, and then I can expect that the output will also be 0 equal to the input so that is another definition the amount of input that you need to apply so that the output level is equal to 0 in this case.

Of course 0 here means AC 0 it is when AC ground. So, in effect you can have ADC voltage or DC bias point over here something like a common mode voltage level. How does the, what is the basic mechanism, which let us the amplifier follow the applied signal or in this case say V offset. Suppose V offset is an applied signal so, you have the AC ground on top of that you have an applied V offset signal. So, what is the basic mechanism involved in the loop which allow the amplifier to follow? So of course, we have a negative feedback loop.

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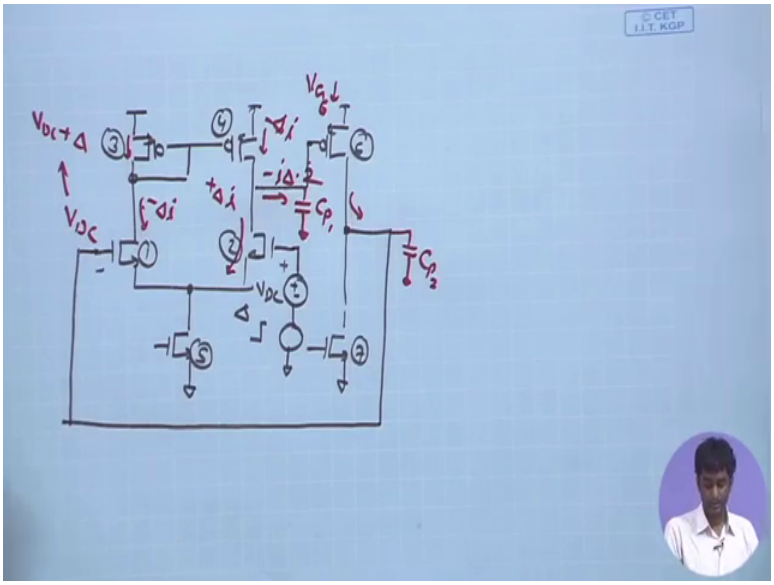

And if we look at the operation at the transistor level and construct the negative feedback look we can see; what is the role of the 2 stages, and each of the transistors in these stages in order to determine the close loop operation. So, we are going to have a negative feedback loop. Remember this terminal is going to be my positive terminal negative terminal, because from here to here you have a inverting gain and again from here to here inverting gain.

So, if you increase this potential is going down and this goes up finally. This is goes up therefore, this is the non inverting terminal, and suppose you have some DC bias point both of them are having certain DC bias point. And I am trying to connect I am trying to establish negative feedback. So, the output has to be connected to the inverting terminal, and then I am having suppose that DC voltage which is sufficient to keep all the transistors in saturation. So, of course, this DC potential should be such that the input devices as well as the bottom transistor are in saturation. So, I have some V DC and on the of that I am applying some signal at some instance, I am applying some say a step signal and let me call these let it number these transistors 1 2 3 4 5 and 6.

So, this is a step signal that I am applying at t equal to 0. So, before that this potential was at 0 plus V DC whatever, V DC you have applied V DD by 2, and let us assume that the output potential was also same V DD by 2 at that instance. And under that condition if I use the direct connected consideration under that condition when the 2 input DC points are same we know that for the differential pair both these DC points are going to be same. Because if these 2 gate voltages are same equal to the applied DC potential V DC, I have the same current almost flowing through both the transistors and upper transistors also have the same gate voltage therefore, there V s g will be same and hence, the other variable this is V s d also must be same. So, we know that under common mode operation if these 2 potentials are same, this potential this potential is going to be same.

Now, if we apply a step potential that t equal to 0 and this becomes V DC plus delta, what is going to be the response of these stages? An we of course, know that if it is a high gain amplifier finally, the output should settle to V DC (Refer Time: 09:09) delta, so that both these potentials are very close together, that is the expected behavior. But what is ensuring that behavior? What is making the amplifier start towards that operation? And finally, stop when the output voltage over here becomes equal to V DC plus delta. So, at least at this node of course, we have some parasitic capacitances, which is coming from the next the common source stage, as well as the parasitic capacitance is contributed by the transistors in this stage. So, I have some effective C P over here.

And when we apply a delta voltage over here at equal to 0, we are creating an effective difference between the gate potentials of m 2 and m 1, we are increasing the gate potential of m 2 with respect to m 1. Therefore, of course, we know the differential amplifier operation will increase the current in say m 2 by delta i, and since the total

current is constant where it by this m 5 there will be a reduction in the current going in m 1. So, here you will have minus delta i same amount, so that plus minus the total current remain same.

So, if I have increasing at equal to 0 and I am increasing the gate potential of m 2 by delta i expect that instantaneously there should be a increase in the current in m 2. Initially t equal to 0 both of them were same, but after t equal to 0 plus this should be having delta i plus as is minus delta i. And if I talk about the small signal operation this is ultimately that you are going to have a reduction in the current direction whatever current was flowing from drain to source in this MOSFET that is reducing. So, the change or the small signal can be represented as minus delta i flowing in this direction.

And therefore, you have the same minus delta i flowing in the PMOS and since this is forming a current mirror. So, if this is having minus delta i we are ultimately having minus delta i in this direction also in this PMOS also because m 4 forms a mirror with m three. So, if this is minus delta i the m 4 should also have ultimately minus delta i mirroring the minus delta i in m 3. And as a result if I apply KCL at this node, what is the total current I can expect coming out of this node? Here you have plus delta i in the down word direction here you have minus delta i in the again down word direction from V DD to this node, or in other word say I can say delta i from this node to V DD right. As a result I have effectively minus 2 delta i going in this direction. Or another words I can say if I represent this as minus 2 delta i current going into the C P.

Or another word I can say that there is a 2 delta i coming from the C P into the circuit node. And if you have 2 delta i current flowing from the capacitor into the circuit; that means, of course, that the charge stored on the capacitor is reducing and therefore, the voltage on the capacitor is reducing right. That is the basic mechanism or differential amplifier whenever you apply a delta V over here, you are creating a difference in the currents, if I assume this is plus delta i minus delta i the delta i in the m 3 gets mirrored into the delta i of m 4. And then at this node if you apply the KCL you are having overall small signal current minus 2 delta i showing outside. And if I, if I assume, if I assume that if I assume that you have the small signal resistances also of course, they will be also contributing to some of that current. So, here I am not talking about the r o of the PMOS and the NMOS in the usual analysis you also have the small signal current paths the R os of the NMOS and PMOS.

So, they will also be contributing to the KCL equation, but if I just look at the capacitor and see what is it is behavior. So, ultimately when it suppose to this node is supposed to charge this parasitic capacitance, is going to increase or decrease depending upon the direction in current flow on the net current flow. And therefore, here at least if I look at these current directions whenever the voltage over here is going up and this total current is positive in this direction that is 2 delta I; that means, the charge ford on the capacitor is getting dissipated and you are having the voltage over here reducing. And if the voltage over here reduces; that means, the gate voltage of this m 6 is reducing, V g 6 is going down and; that means, the current in m 6 is going to go up and; that means, that this particular potential once again you are having another I can call this C P 1 let me call this C P 2, you are also having some parasitic capacitance over here.

If this overall current is going up once again you will have this node voltage going up and as a result additional charge getting dumbed on C P 2 and it will try to increase this voltage. And as this voltage increase there is an finally, upper vouchers V DC plus delta. So, this voltage also is going to shift from V DC to V DC plus delta, and as gradually this voltage approaches the V DC plus delta what is going to happen once again, both of these become almost similar as a result the delta i plus minus diminutions approaches 0. And hence the charging of the capacitors tops there is, because other that condition whatever the small signal current delta i plus minus is flowing this stop. Because these 2 are now matched and beyond that point you do not have any difference in the small signal currents at this node you do not get an overall small signal current going into the C P.

Therefore this stops and finally, since this voltage stops rising this voltage also stops rising and it to the value which is V DC plus delta. So, this is the basic you know mechanism which is present in the negative feedback loop, which is helping us in making the gate voltage of m 1 closely follow the gate voltage of m 2. So, we are going to use this same mechanism for extracting the information for the offset voltage that we have in the amplifier. Let us see how we can do that, any question in this operation how the gate voltage of m 1 is following the gate voltage of m 2 whenever you change the gate voltage of m 2 by small amount how it is able to follow. So, circuit transistor level operation point of view also it should be clear.

So of course, from the block level we know that amplifier with sufficiently large gain it will also always make sure that these 2 potentials are going to be almost close or very similar. But at transistor level this is the overall operation involve. Now how can we use this to extract the information regarding the offset? So, as I as I said here if you have an amplifier with an offset rather than, rather than having a perfectly matched pair you have any offset. And then rather than putting ADC voltage over rather than putting an absolute 0 I can suppose I have the DC bias point which is say V DD by 2 So, I put a V DD by 2 over here. And as a result this becomes V DD by 2 plus V offset, and once again the amplifier should make sure that this point also is V DD by 2 plus V offset.

And hence this is also V DD by 2 plus V offset I am just taking V DD by 2 as a comfortable number because that is midway between the V DD and ground. So, if I have some DC bias point in the top of that there is a offset present and in the close loop operation or in the unity gain configuration, the amplifier gain will make sure that this output also settles to V DD by 2 plus V offset. So, I am interested in extracting this quantity, and to do that the circuitry that can be used, it involves a capacitor across which we would like to sample the offset voltage.

So, we have say the negative feedback in action, and at this point we apply V DD by 2, a common mode voltage which basically. And then we also apply the same potential over here. So, V out which is equal to V DD by 2 plus V offset is going to appear over here right. So, if the con (Refer Time: 18:30) connected in this fashion where you are applying V DD by 2 at the positive terminal. Remember to the circuit diagonal this is the terminal available, this is internal to the amplifier. We have just extracted it in modeled it as a source, but ultimately it is coming from the properties of the amplifier mismatch in the transistors. So, this is this is not accessible to the user, to the user to designer this the point accessible.

So, I can apply a desired voltage over here DC AC whatever you want. So, this is part of the amplifier we are just modelling it as a convenient delta V in series with the input device. So now, I have the V OS plus V DD by 2 coming over here at this point. And therefore, what is the effective voltage across this capacitor V DD and V DD by 2 plus V offset. So, we have V offset stored across the capacitor in this direction. So, through this loop through this configuration close loop configuration, I can extract the offset voltage of the amplifier and store it across the capacitor. I can call it say C offset. Now the next

thing is we have extracted the V offset we also like to apply it to the signal in a such a fashion, so that the effect of this extracted voltage cancels or nulls the effects of the offset of the amplifier.

So, in this loop itself, if I see if I immediately open this after you know shorting the output of the amplifier to this terminal the capacitor, if I open this and I also remove the connection from V DD by 2. Suppose through some switch I had connected this point to V DD by 2. Now also through some switch I had connected the output of the amplifier with the inverting terminal, and through another switch I had connected the inverting terminal of the amplifier to this capacitor. So, suppose in this operation that I just described these 3 switches are closed and therefore, this was having a negative feedback unity gain operation negative terminal connected to the this terminal of the C off and also this point was connected to V DD by 2.

After that if immediately open these 2 switches and also this switch, what is going to happen to the capacitor over here? And what is going to happen to the charge that was stored at this node? So, if I assume that these 2 switches are opened simultaneously, after that this node becomes a floating node, because it does not have any current paths through any other transistor. This is the input device MOSFET gate, ideally it is having very large impedance, there may be some gate leakage current small amount of gate leakage current which can assume that is very small, and this is a capacitor. So, whatever charge was stored over here, at this node or the negative plate of this capacitor, it has no other path to go, it will remain trapped on that plate of the capacitor.

And therefore, whenever you have some negative charge on this plate of the capacitor stored, it will keep the positive charge on the other plate also in stuck. Because it has electric feed and you have in that negative charged over here which is not able to skip. So, it will also keep pulling that negative charge and into that positive charge also keep tackat that point. So, because this becomes a floating node after I disconnect these 2 and that negative charge that stored over here, is not having any path to leave it will be stuck at this point, and the electric field if I just zoom out this you are having the suppose negative charges stored over here, positive charge over here, so that the delta the total charge magnitude is going to be Q equal to C v So, C offset times the V offset. This is the sorry, V offset yes, so you have, this is the total you know charge which is stored on the positive and the negative plate of the capacitor.

And the movement you disconnect this from V DD by 2 the charge at this node is remaining clammed it has no way to go. And therefore, it is also going to make sure that the positive charge over here also remains clammed. What does that mean? That means, that the charge stored on the plate of this capacitor is going to remain fixed. And if the charge remains fixed that also implies that the voltage drops across the capacitor also remain fixed, it is not going to change.

So, just because this node is becoming a floating node, and you do not have any path this charge to go, you are able to trap the negative charges over here, and hence the positive charge on the other plate of the capacitor. And hence you are basically storing the offset voltage across this capacitor. And once you have this offset voltage stored I can go ahead I have open these 2 switches also. So now, it has become a open loop amplifier. And then I can basically apply my inputs to the I can apply my inputs to the 2 terminals of the comparator through another switch.

So, if I had these 3 switches operating in or getting on in phi 1 mode. If I call this say phi 1 phi 1 which is one clock face this is phi 1. So, these 3 switches were opened were closed in phi 1. So, when the phi 1 phase came of the clock this is phi 1 case, these 3 switches were close and as a result you had the negative feedback intimated over here, negative terminal shorted to the positive it was the capacitor over here and also this terminal connected to V DD by 2. But know I am opening the phi 1 switches and then connecting the phi 2 switches, phi 2, phi 2 to the 2 inputs that I want to compare. So, here now I can have my 2 inputs. Say you know, V in minus and V in plus, which can be the circuit is that we the signal that we have the ram signal and the input sampled signal, suppose any 2 signal 2 analog signals.

So, in the phi 2 says I close the 2 switches over here other switches are getting opened. And therefore, what is the equivalent circuit that I will have in the phi 2 phase? So, this can be give us phi 2 phase. So, when phi 1 is off phi 2 is getting on immediately, if I assume that then what is the equivalent circuit resulting circuit. If I keep this as it is, if I keep this as it is and try to draw the corresponding circuit in the phi 2 phase.

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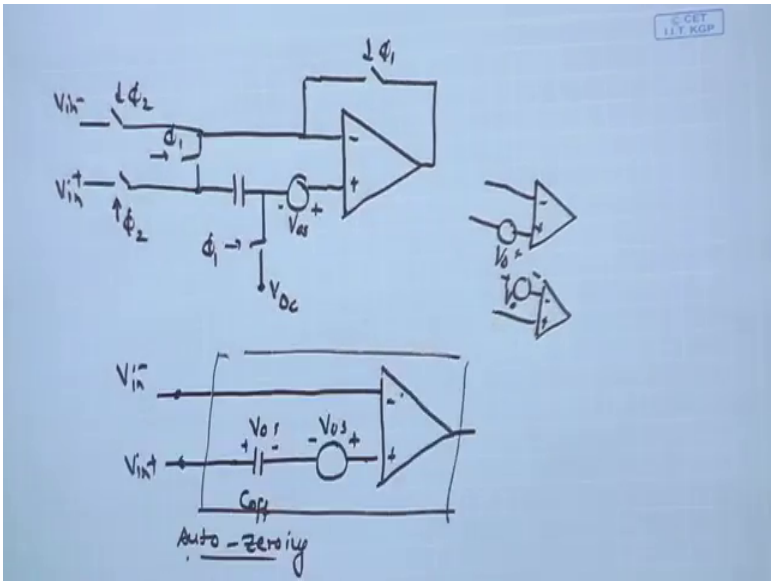

So, you have the inputs getting applied to the negative and positive terminal of the amplifier. But in the positive terminal I have this C offset coming, this C offset coming we has which has V offset voltage stored across, this is V offset voltage stored across this. And then you have the actual offset voltage of the amplifier with polarity given by plus minus V offset over here. And then you have the positive terminal negative terminal negative terminal is directly connected to say V in minus, and you have V in plus and this is the output.

So, this is our normal comparator only thing is we have the offset voltage stored across the C offset coming in series with the offset voltage original offset voltage that was modeled at the positive terminal of the amplifier. And as a result these 2 coming opposite polarity in series they get cancelled, as a result the effective potential over here is just V in plus and here you have V in minus the internal terminal. Therefore, what I can say is that the stored offset or the stored voltage across the capacitor has been able to cancel out and mitigate the effect of mismatch. Whatever offset was present in the amplifier it captured it across it is terminals and that came in series with the applied signal or in series with the amplifier offset and therefore, nullified the effect.

And then I have close to an ideal amplifier with 0 offset. So, if I look at how the signal is seen the comparator, it is having 2 terminals over here, and the C offset is storing the V offset with opposite polarity and it is getting cancelled with the V offset. So, this is the

overall functionality or overall principle for the offset cancellation. It also terms that auto 0 in which can be use for canceling offset in comparator as well as amplifiers even the front end amplifiers may be having offsets. And in certain cases cancellation of those offset can also become important right now. So, far we have not discussed the issues that would offset of the front end amplifier, will see they are the concerns are significantly different. And we will see what can what technique can be used over there to mitigate the offsets.

And whether it is equally important concern over there; here we have discussed with respect to comparator what is the effect of offset, what is the effect of overall comparator performance and also the ADC characteristics. So, ultimately we have the overall offset cancellation circuit given by this scheme where, we have we can call it say any particular V DC it can V CM and then you have switches over here connecting the negative feedback and then also you have switches over here. So, these 3 switches operate or get on in the phi 1 phase, and then you have the other switches, other 2 switches which are getting on in phi 2 phase. So, this is the overall scheme that can help us in cancelling the offset in the amplifier using out of the range scheme.

Student: Sir, do we have the concentrator or compensation for the bias current?

We look into that of course, when we are going for closes loop operation we have to be concerned about the stability between the operations. So, we will look into that that we will try to build upon all the non idealities in this circuit and try to see, whether we are meeting the concinnities, or whatever specks we have chosen for this amplifier whether with the same specks we are able to comfortably need our close loop operation.

Student: Sir, we have (Refer Time: 29:50) something clock or simulation (Refer time: 29:52).

That is good question, and we will look into that so that of course, relates to the size of the capacitor the capacitors sizes larges you can keep the stored charge over here for long time without getting it destroyed by leakage. In that case you can refresh it very less option for example, for the entire conversion cycle you can do it just once, before the ramping starts you can do it once. If the capacitor size chosen is small then you will need to refresh it frequently. So, of course, there is a trade of if you want to save area and make these capacitors small, you will have to go for very frequent update.

Student: We have to model the offset voltage when we have the positive terminal?

We can model as both the terminal. So, we can also derive V offset by 2 plus minus over here, but this is convenient for explanation.

Student: If we need to offset this presentise relative, how do we apply the (Refer Time: 30:53)?

The same thing so, whether it is whether the offset is present here, you have a plus minus you have a V offset over here. So, it is equivalent to applying a minus plus V offset over here so early the same thing. Let us take short break and then resume our discussion on the details of the circuit design.