Analog Circuits and Systems through SPICE Simulation
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Lecture - 42
Offset

Welcome back. Let us resume our discussion on the variation in mismatch and related issues. We just now discuss the implications of threshold voltage variations on the inverter transfer characteristics.

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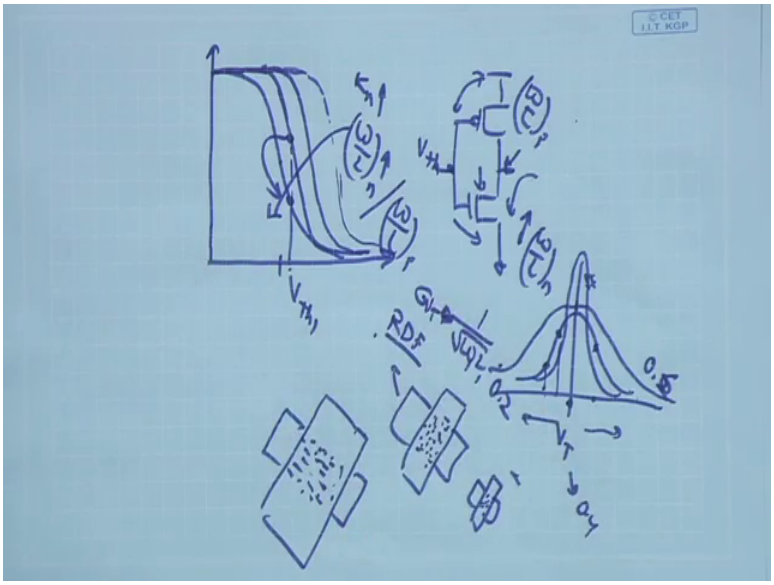

And we saw how is it going to impact the interfacing between the digital inverter and the preceding analog stage. And we try to justify the use of the second stage in meeting the full swing requirement and having better robustness and also making sure that the static power dissipation in the interface inverter is limited. Just like the threshold voltage distribution has it is impact on the characteristics of digital CMOS circuitry; it has even more severe more critical impact on the performance of analog circuitry. The threshold voltage mismatches can play a very important role in the differential amplifier operation where we are expecting that that pair the transistor pairs constituting the differential amplifier they are very well matched.

So, or our differential amplifier analysis assume that the transistor pairs are well matched there V T all the device parameters lambda everything is well matched. And that gives us

good differential amplifier it ensures that the CMRR ratio is large the differential gain is large in the common mode gain is lesser. However, we have seen in the beginning that if you are having significant mismatch between the transistors you can have a poor CMRR as well as PSRR. You can end up have converting a common mode disturbance in your differential signal because of the mismatch in the input pairs or the load pairs.

So, whenever there are pear transistor and you having mismatch between them it can lead significant amplification on the common mode signal. Even when we are operating the amplifier as comparators or as feedback amplifier once again those mismatches can play important role. For example, here in our in a particular example we just studied, we came up with an architecture where we are using 2 comparator C p and C n.

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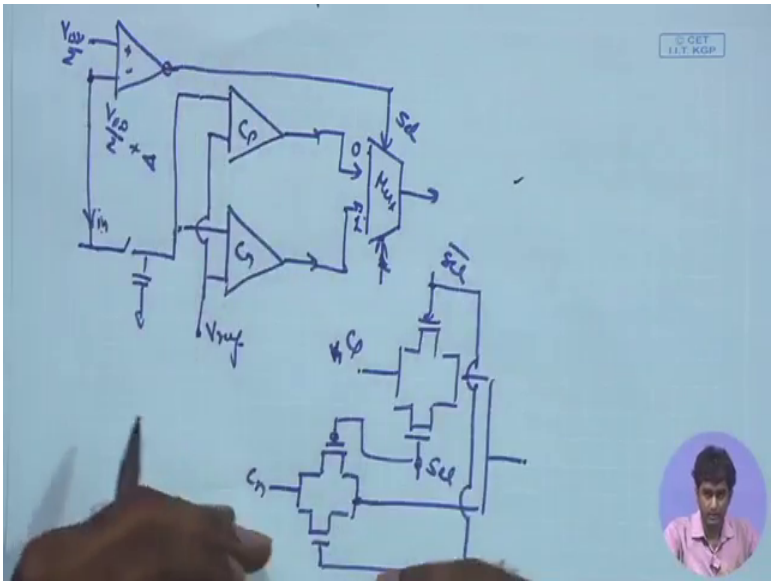

And we know that the individual pair C n and C p individual pair of the MOSFETs in C p and C n they can have threshold voltage mismatches.

So, let us see first of all what is effect of the threshold voltage mismatch in the transistor pair and finally, how does that affect our overall operation this architecture that we have chosen.

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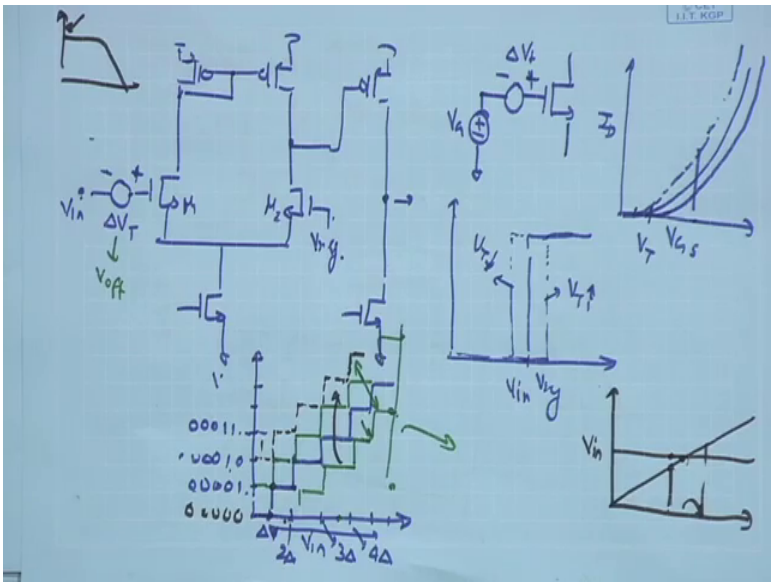

Let us consider the first differential stage itself, ideally if I am looking at the differential input with single unit output. And suppose we also include the second stage over here. So, of course, ideally we understand that considering the process idearation we not have a very well defined control on the output DC potential. But suppose we have sized it such that if the DC potential over here is V DD by 2. Suppose we have some mechanism through which we have fix this potential to V DD by 2 or assume that when the input signals are close together the output expected is V DD by 2.

So, when both the signals are exactly same the output expected is V DD by 2. Now when the we know that we have derived the specification for the gain of this amplifier when we are operating it as a comparator based on the a DC application specifications of resolution so on. So, there we saw that if the there is a significant difference between these 2 signals delta V say in our case 15 millivolt the output should be completely going up or down to V DD or ground respectively.

However, if there is a significant mismatch between these 2 transistors, how are the overall transfer characteristics going to change? So, V T mismatch in the transistors can be represented as a voltage in series with the gate of the MOSFET. So, I can add a delta V T in the gate of the MOSFET and how does it captured the V T mismatch if you are having the ideal MOSFET where you do the I D V gs characteristics.

For example and you will get a certain curve for the ideal MOSFET without and mismatch. And then in the second case this is the nominal V T or the MOSFET that we expected. But in the case you are having the device which is having a slightly larger delta V T. So, what will happen the entire curve will shift slightly toward the right? On the other hand is a delta V T is negative the entire curve will shift towards the left. So, I can capture this shift in the characteristic by modelling the mismatch of the change in V T by a small voltage in seize with the gate of the MOSFET that putting a delta V T over here.

There are many other parameters in the MOSFET that can vary V T is of course, particular parameter coming in the model. In the actual physical device there are so many different parameter because of which other characteristics can also vary, but in order to capture the parameter variations generally delta V T or V T mismatch is the good way, and generally in order to capture the effect of all other you know physical parameter variations and mismatch. We model all of them; we can model all of them in form of V T mismatch. You can also have many different physical parameters contributing the V DD mismatch.

But for the time being assume that ultimately, the some process mismatch or some process variation is leading to this delta V T change. And we want to see the effect of that on the comparator operation of the amplifier operation. As long as the open loop operation is concerned and if we say that say this is m 1 and this m 2 and this is having a V T which is slightly larger as compared to the other device into, if we have V ref over here. And now we assume that the V T of this device is larger. In case of, in case of perfectly matching case I would expect that that when this input approaches V ref and process V ref the output should be going output should be going high.

So, if I look at the ideal transfer characteristics when the V T are very well matched and looking at V in whenever V in is crossing the V ref I should have the comparator output transiting from low to high. This is ideal characteristics, but now if I have a delta V T coming over here; that means, the effective V T of this, so the way. So, I have drawn is you know the positive voltage over here; that means, the effective threshold voltage is m 1 has been reduced. If it tick the polarity plus minus then it is increased, why? Because if the polarity is plus minus over here; that means, you know a smaller gate voltage over here will be able to able to you know turn it almost strongly because your having a delta V T Positive over here.

So, here also if I am having this delta V T Positive from here to here; that means, if you are having another gate voltage V g that you are sweeping this V g plus a positive delta V T added over here will mean the effective gate voltage here is larger as a result the current will be shifting towards the right. For a given V gs the current will be a larger and these are shifting toward left. So, we should just take you are the polarity.

Now, likewise here if you are having a delta V T sign over here plus minus; that means, if the for a given V in the effective V g experience by this MOSFET is larger as compared to the m 2. As a result, what do we expect? It will be tripping at lower value of V in. So, the (Refer Time: 08:11) will be shifting this way. On the other hand it was negative that would mean it will require larger V in to mismatch the same V ref. As a result this is V T lower and if you have the other opposites scenario the V T will be shifting or the characteristics will be shifting towards the right side this is for V T big higher.

And definitely if your delta V T become comes comparable or larger than the resolution that you are targeting, say 15 millivolt in our case. That would mean that you can have error in the overall digital value that you are getting. For example, if I expect that the overall a DC transfer characteristics is something like this you have the analogue values along the x axis. So, this is your analog sample V in. And correspondence to the y x s your plotting the digital word. So, if my these are the intervals. So, this is your delta V and let us let me call delta. So, this is delta, this is 2 delta, this is 3 delta, 4 delta and so on.

So and corresponding to that I have the digital words. So, if my signal is greater than delta then I am having the word something like 0 0 1 if I am my signal level is higher than delta. So, if I say my signal level is higher than delta for this entire range single line between delta into delta the output is 0 0 0 0 1. This is a binary output that I am depicting; if my signal level is between delta and 3 delta my digital word is over here. So, I can write it 0 1 0 0 0 and so on. Likewise if the signal is between 3 delta and 4 delta my signal the digital word in codded is 3 0 0 1 1 and so on. So, this is the digital word corresponding to the corresponding analog value. If the analog value is lying between delta into delta it is going to encode it as 0 0 1 if it is between delta to delta 1 0 1 1 and so on. This is the expected value and we can go on. So, this is the stare cade case you know approximation we of course, have some error we have a contestation error of

course, because for this entire range of the input signal the output is same 0 0 1 whether the signal lies here or here it is always going to be encoded as 0 0 1. So, that leads to an important a DC you know parameter which is contestation error, we may did with that little later.

But now assume this is the characteristics we expect ideally. But now the comparator is having some delta V T shift and suppose, the V T is negative form one input signal is coming over here. And V T of m 1 is lower than the V T of m 2; that means; the comparator will be tripping from high to low in our case for lower values of V in write; that means values even lower than delta will end up having the high level over here. So, you can have the entire characteristics getting shifted. Suppose the delta V T is just around 15 millivolt higher than 15 millivolt or 20 millivolt.

So, in that case the shifted characteristics will be something like this is. So, if the assuming that delta V T is say 20 millivolt. So, it is higher than delta and lower than 2 delta in that case the overall characteristics that shifted towards left and we have this as a new characteristics right. Because now the signal V in is getting effectively added with this delta V T and as a result it will be crossing these ref delta references for lower values of V in right. So, effective potential over here becomes V in plus delta V T in that case.

And as a result the whole curve for the a DC characteristics get shifted towards left. Likewise if you have larger mismatches whether 15 millivolts if it is 30 millivolt or 35 millivolt there will be you know 2 step shifts. So, the entire characteristics will be getting shifted by 2 steps.

So, in that case the characteristics may look like this right. So, first of all we are having a shift in the overall characteristics having error in the exact value and also we are losing some of the consternation, because here the values we cannot have values lower than or we cannot encode the values lower than a certain magnitude say 3 delta. So, if this is the condition your having a twice 2 step shift then we cannot include the values which are within the range 0 to 2 delta, that will give you that you have basically losing that, because 0 to delta is lying out of range of this characteristics.

So, we are losing that information of around 2 delta voltage all the signal levels lower than 2 delta are not getting encoded correctly. That is one disadvantage and another disadvantage is that the characteristics are digital word in recorded are higher than the

expected the exact values. So, if I am say having only say, one comparator then this is occurring as an offset in the overall amplifier overall ADC characteristics.

So, we can test the ADC and we find out what is the overall shift and digital domain we can subtract that shift. And we can still retrieve the required value at least for the range which is getting captured. The lower 2 delta which is getting missed, that we cannot capture, but the remaining can be obtained by just subtracting the 2 delta digitally. You have the digital word you can subtract it always if you know that is offset, this is clear?

Now, the problem is that is in general this delta may not be even constant sorry; the shift may not be even constant. The delta V T that we are adding over here that may not be constant this can vary over time. So, there are some device effect because of this offset can vary over there can be time dependent shift in these offset. If a static offset which is constant in time then we can basically read out the digital data and we can collaborate it and we can find out by texting that this is the offset this amplifier is having or this comparator is having, this is the delta V T this MOSFET is having.

And based on that I can go up back in the digital domain and subtract those lower 2 bets values or add those 2 bets value to get the correct digital value. That is possible, but in general that can keep shifting over time the digital domain does not have the information about it is not really tracking the time dependent shift in V T. So, that can lead to out of problems it can lead to inaccuracy on the fligh it can lead to inaccuracy in the recorded data.

In our architecture we have another issue that is also coming up we are using 2 comparator. The PMOS input device and another with NMOS input device. And their characteristics can get shifted by you know may be similar amount in opposite directions. If that happens suppose NMOS characteristics get shifted up by 2 delta and the PMOS characteristics get shifted down. You can have the delta V T becoming you know negative plus minus as a result the characteristics can shift down.

So, suppose this is the characteristics that the comparator with PMOS input devices having. So, it is you know very different from or significantly shifted with respect to the characteristic that the NMOS comparator is having. Therefore, for a given input signal we can see that the output of the NMOS and the PMOS comparator will be different and as a result you know you are going to have different digital words coming out of those 2.

If they are operating in different region for the lower voltages as we said the PMOS will be used for higher voltages the NMOS input device will be used.

And at the juncture we can have that miss, this is the point beyond which the NMOS will be used is the input voltage is higher than certain value will be going to the NMOS comparator and if the input voltage lower than this boundary will be using the PMOS. But boundary once again we can see that the NMOS will be the PMOS input device will be giving a different result and NMOS input device will be giving a different result.

And therefore, you have a mismatch between their results if you are using at some point your using the NMOS comparators output your using other time you are using PMOS comparator output there mismatch can result in different effective digital words for similar magnitude of the input. And therefore, we are combining the results obtained with the help of NMOS comparator and the PMOS comparator once again it can lead to errors, relative errors.

And once again, if those 2 errors are changing over time shifting over time that becomes even difficult to track; so in general if you are for example, going for the sizing of the transistor you are trying to reduce it to few micrometers. In that case the mismatches can further aggravate, you can have mismatched between the 2 PMOS transistors over here the NMOS over here and as a result, the overall the overall effective mismatch between these 2 transistors in the pair it can lead to a larger effective offset voltage. And good value will be at least it can range it can go all the way up to few tons of millivolt if the fabrication layout is not done properly the mismatch can be pretty bad it can go to few tons of millivolt.

And in that case our transfer characteristics for the NMOS and PMOS comparator can be different and vary over time. And therefore, there will be a time dependent error in the signal that you are recording. So, this is very undesirable and definitely we would like to have some mechanism through which it can be compensated. So, before we go there we would you like to you know talk little bit more about the overall offset of the amplifier. Any question before we proceed further? And discuss the offset and some more detail.

So, first I am trying to x trying to show the effect of the offset. If you are having such a delta V T mismatch at least in this input device what is the effect of that on the overall a DC transfer characteristics. And then let us have a little bit more discussion on the offset

for a single ended output or differential output what is the difference how does it come into picture. Any question to this point? Amplifier over here it is single ended output and of course, here we do not have a mechanism of defining the DC potential, we have assume that the 2 outputs are very close or close to V DD by 2.

And one of them are going high by delta V which is 15 millivolt I expect that this is having sufficient gain at will be able to drive the output completely V DD or completely to ground. That is what we have assumed. Now if I look at the delta V T basically it is shifting the con characteristics in certain passion depending upon the polarity of delta V T. And this delta V T I can place it by V offset, which basically is going to captured the effect of delta V T of the upper 2 devices also. How do we do that? Just like we have the concept of input referred noise we can refer the noise contribution of all the devices that the input. Likewise we can refer delta V T contribution of all the devices at the input.

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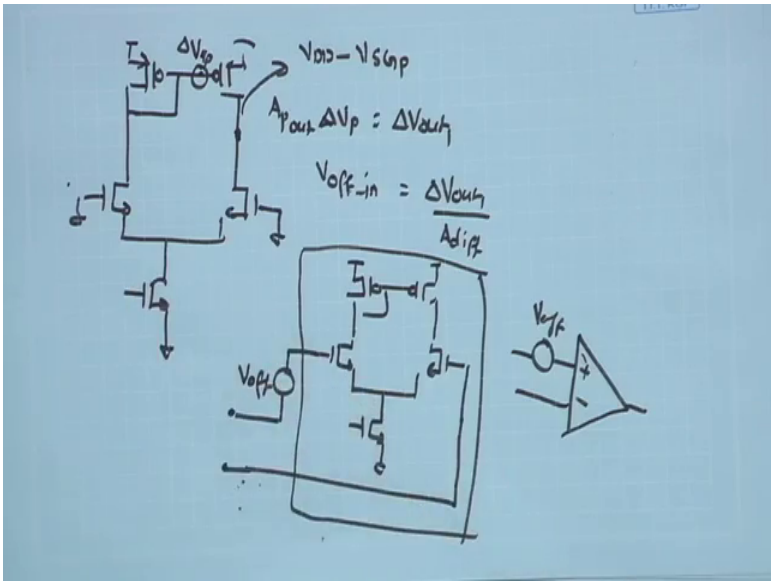

For example if you are having say, if you are having say certain delta V T over here. So, you are having delta V TP and also you are having certain delta V T. And So I can take the superposition of this individual delta V T and find out what is the effect on the output voltage because of this delta V T coming in. For example, if I assume for example, let us take the super effect of this delta V TP first on the output assuming small signal assuming that this delta V T small as compared supply and small signal is valid. I can

find out the gain from this point to the output. So, let me call this A P to out. A P to out times delta V p is the delta V out 1.

So, as compared to the nominal value nom, what are the nominal value? Nominal value was equal to this value expected to be V DD minus V SG of p and depending upon the threshold voltage we can determine what is the V SG you have a certain bias current and it was going to generate certain V SG. And therefore, this under perfectly match condition these 2 being match, these 2 being match we have seen that these 2 drain potential should be similar therefore, they will be equal to V DD minus V SGP this is the DC potential expected. But now if I assume that there is a small delta V T coming over here.

Because of that whatever is the gain from this point to the output it is just going to at like a common source amplifier over here we have a input device and then if the common mode analysis also we have done this kind of you know analysis. This is acting like a common source device source grounded here applying some delta V T is going to lead to voltage gain over here. And I can call it delta V out, A P out means from the p gate to the output we have gain A P out which is a gain of this common source amplifier, from this input of the gate to the drain. Assuming that others inputs are set to 0.

So, for this site is just like common source amplifier PMOS input device this is the output point. And for that I have certain gain A P out times delta V equal to delta V out 1. Now if I want to refer it to the input at, what is the equivalent delta V at the input? We should produce the same delta V out 1.

So, in that case that can I can divide this V offset input that is the input referred offset, input referred offset equal to this delta V out 1 divided by a differential which is the differential gain of this circuit, what is the difference between these 2 inputs which would produce the same shift or same change in the output as compared to the DC bias point. That becomes my input referred offset. So, just like the noise case we have seen that the input referred noise is mostly depends upon the first stage right. Because it is getting for the second stage the overall mismatch effect is getting divided or over the noise is getting divided by the gain of first and second stage.

Likewise for the 2 stage amplifier or comparator that we are using the overall offset or the input referred offset will be dominated by the offset of the first stage. Second stage

offset which want to refer it to the input it will be divided by the gain of 2 stages. So, as compared to the first stage it will be sufficiently suppressed. So, the mismatch in the first stages the PMOS pair and NMOS pair they are going to play important role or dominant role determining the input referred offset of the amplifier. Not So much for the second stage similar to the noise effect.

And therefore, I can for the external user if I have designed this transistor and I have characterized this that this is the input referred offset. So, I can model this input referred offset as an ideal perfectly matched you know, differential pair where all the transistors are very well matched. I have taken the contribution for of mismatch in these 2 pairs these 2 pairs and then added them together over here. So, effectively I am having some V offset which is present in the device.

So, this V offset is having the effect of delta V T or the mismatch in these 2 devices they are anyway directly coming at the input because there is any way the input device. Whatever is the delta V T mismatch over here x it appears as it is over here. For the output the low device is we are first calculating the output change because of a particular delta V over here and then referring it to the input by dividing that delta V out by the gain of the first stage.

So, this is the essential concept of the offset or the input referred offset. And to the external user that I have this as the ideal amplifier which is perfectly matched and I am missed the effect of mismatch in the differential pair transistors are being hmm model with the help of this we offset inserted in the in one of the terminal; so in this case the positive terminal.

So, in general I can model this has an offset voltage V offset inserted in series with one of the terminals. So, I can either inserted over here or here that depends upon the overall polarity. So, I can model the overall amplifier by an ideal amplifier extract it is offset out. Just like me do it the noise then we extract all the noise as the input referred noise and the rest of the amplifier is noiseless. So, we are doing the same thing with the offset. And then we can it is convenient to analyze the effect of such an offset of delta V on the amplifier characteristics on the output DC point or the signal swing and so many other thing that we are going to get.

So, this also plays an important role in the front end we have not here discussed this implication the front end design. That is also going to be there for the time being we have started this with the comparator design. Will revert back to the front end design also try to see; what is the effect of offset front end design especially for the fully differentially case.

And what can be the solution to those. Likewise in the comparator the solutions may be slightly different we can see; what are the poor than cons of this offset. So, overall characteristics point of view, this is what is going to happen this is the overall implication on the architecture that we have chosen. And next we need to look into the we need to look into the solutions at circuit level or architecture level which can help us in medicating the effect of offset and get back to our original a DC characteristics. Any question before this point?

Student: Previously why we have shifting of that curve I D verses delta V?

This?

Student: Yes.

So, here as I said you are having the ramp voltage right. So, what is the mechanism of the a DC that we are having? It is charging the capacitor using a ram voltage and at some whenever this ram voltages reaches the V in sampled it should trip. But now suppose I am having this delta V T added to the m 1 it is representing the offset. So, in that case the V in plus delta V T represent the larger voltage at the gate of m 1, so rather than tripping here it will trip here.

So, as a result if it is going to trip here; that means, the digital count is lower than what I expected or the ideal expected value. If that likewise the delta V T was negative it would trio here and the digital could have been higher than the ideal value. So, this is the digital you know for a given analog input I have drawn the digital value. This is the characteristics between the analog input and the bandwidth digital output of the a DC. If the input is between in 0 and delta the output is all 0 0 0 0 if the input is between delta into delta output is 1 0 0 0 or in other words 0 0 0 1 if it is between delta in 3 delta 2 delta and 3 delta it is you know 0 0 0 1 0 and so on.

This is the characteristics transfer characteristics or input of the characteristics of the a DC. If now if I have this scenario then the entire curve either get shifted up or down. This is clear? Any other question? And more severe thing is your using 2 different comparator for NMOS and PMOS the shifts can be opposite. And in that case the mismatch effect is even worst. It can other point is can shift over time.

There can be time dependent shifting in V T. They are some mechanism through which we can have time dependent shift in V T like temperature. Temperature changes V T can change and as a result the PMOS and NMOS have different temperature coefficient for V T and that can lead to different shift in the V T.

Likewise there some other mechanism related to such known effects for example, which because of smaller oxide thickness etcetera, we can have some mechanism which can lead to time dependence shift in the devices. And they may be reversible, but temporarily they can have you know time dependent shifts and which can lead to time dependent shift in the overall DC characteristics over here.

So, if you want to be accurate in a if you want to preserve the accuracy, not to you know miss the lower values of the signal and have correct values coming out of the 2 comparators consistent values coming out, we would like to go for cancellation of the offset. The example that we have taken constrain relatively relax. We are assuming full swing 0 to V DD and the delta V or the resolution in voltage domain that we are going to seize or on 15 millivolt the offset values can be of that range 15, 30 millivolt you can go to that.

If the perdition requirement are higher may be 8 bit or 9 bit there you can see that much more many more bit is will be corrupted. So, here we have taken the resolution of 7 bit and as a result the delta V analog resolution of the comparator is you know 15 millivolt and offset that you can get one tonometer can be of that order means few tons of millivolt. And in cases when we are so still here we are talking about you know few bit is getting error or few bit is having problem.

But, if you are having higher resolution you can imagine suppose, you can having 10 bit resolution or 10 bit resolution would require you know V 1 millivolt of precision and there you have 15 bit or 15 millivolt mismatch the 30 millivolt mismatch 30 levels of error. There is even more drastic therefore, the offset cancellation will become even more

crucial. So, here probably it is less crucial, but still your having 30 millivolt of mismatch your having you know 4, 5 LSBs of error which is not good so and likewise 2 comparator being used that is also aggravating our case. So, therefore, it is important to consider this concept of offset and the technique to cancel that offset. That is in general applied whenever we are having whenever we are targeting significant precision our data processing.

And along with the single unit virginal will also looking to the differential version fully differential and try to see how it can benefit us, that let us going another reason why differential fully differential operation is advantages. For the comparator we will see that if your using fully differential version offset cancellation can be more effective or more convenient to implement. Any question?

Student: Sir, here delta V T and V offset both are some DC some DC where to use.

Yes.

Student: So, what do you mean by the amplification of a DC value some gain?

D C amplification, you have DC gain right what is you have a amplifier characteristics low frequency up to DC you have some gain right? That means, if you are if you apply a DC voltage and just keep it or apply DC voltage of course, the output voltage will change, that is DC. So, the gain of the amplifier is this right. So, DC you have gain. If you change the DC bias input one of them is V DD by 2 and another is V DD by 2 plus 20 millivolt of course, the output will change.

Student: And when finding the gain we assume that the DC the DC point is constant. So, we take if find the gm. So, in this case sir DC point is.

D C bias what you have is a small change in DC between these 2 or small difference in DC can be seen as DC bias plus the delta V, the delta V small signal. What I am saying is small signal is applicable and we are looking at small signal gain. So, signal gain is the high frequency, small signal can be DC. Any other question?

So, as we have seen in the chopper, what we are trying to do? We are trying to shift the frequency towards or signal towards higher frequency the 1 f minus towards DC close

DC. We do not want it to interfere signal. So, there also we are trying to model that noise with the at the very low frequency source close to DC. So, any other questions?

So, it is all these things are important to understand and these are design issues which are very crucial, in our simulations also try to we will try to access some of these and look at the associated solution, resume our discussion.