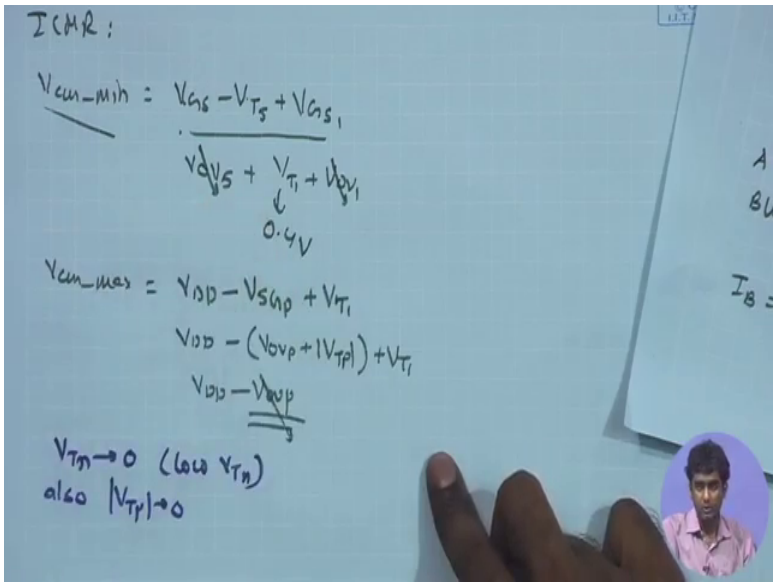
Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

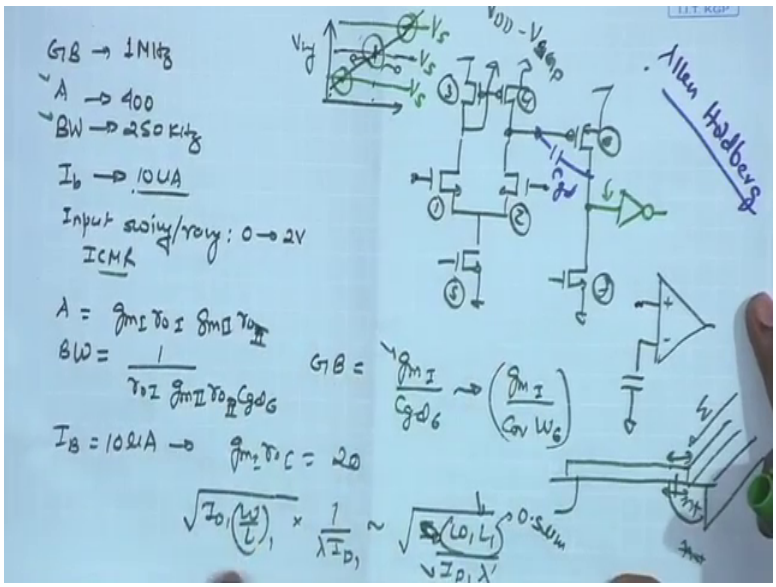
Lecture - 41
Inverter Interfacing

Welcome back. Let us resume our discussion on the ICMR and looking to the solutions which can be taking to get a full rail to realize ICMR.

(Refer Slide Time: 00:23)



(Refer Slide Time: 00:35)



One of the ways of course, that may seem obvious is that if we have the option of choosing a 0 vary transistor for the NMOS we can increase ICMR if I have the option of very low V D transistors I can select those specific devices to reduce the V C m min and in some technologies u n power meter TSNC or UMC models you may have transistors which are having lower V T and I can choose those transistors in some cases to have to increase the signal swing not all models that not all foundry providers those models in some cases where you have the models available if you have access those the particular device model you can use in improving some other device performance.

In this case we can probably go for a 0 V D D transistor for the NMOS for improving the ICMR on the lower side. So, in that case of course, as we see the for the ICMR min another V t 1 will be reduced few tons of millivolts and as a result you have V C m min going towards lower value if we do that we also if we if we look at this equation here the V C m max also depends upon V D D minus the V s g of the PMOS and we say that this is the gate voltage V D D minus V s g this is going to be gate voltage of the PMOS thus plus V t 1 is the maximum input voltage that you can have this is the mix maximum input common mode now V t 1 is 0. Then of course, I have the maximum input common mode given by V D D minus this quantity you do not have any longer the V overdrive come coming, but you have V D D minus this entire V s g term coming and therefore, once again if I really want to take the advantage of 0 V t NMOS I would like to get rid of this V t also.

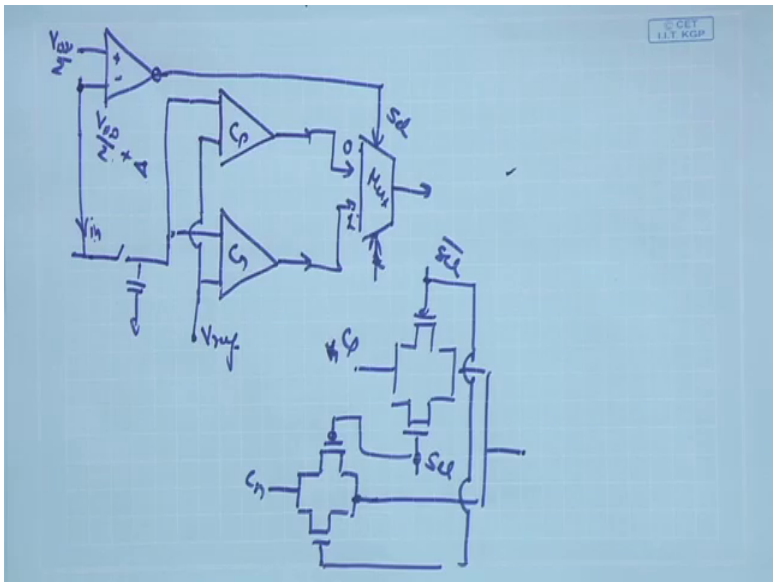
So, we can go for V t n tending to 0 or low V t NMOS also V t mod V t P tending to 0 if you have low V t PMOS option then only you will be get you will be getting the same advantage on the upper side if you take the nominal V t PMOS and the upper side you will be having limitation on the ICMR. So, make sure that if you are choosing low V t NMOS which also choose a low V t PMOS that is one way and of course, in case you do not have that option available we can go for some other techniques to improve the overall ICMR. We can go for architectural level choices we can combine say 2 different kinds of comparators to arrive at overall scheme where you have full range ICMR.

So, let us have a look into that and let us try to address the issues related to that scheme. So, here I can if I take note of the fact that an NMOS comparator is going to have ICMR which is limited on the lower side because for NMOS I have the V C m min getting

limited by the V t of the NMOS transistor on the upper side; however, we can go all the very close to be V D D.

If I am choosing bit transistor for PMOS input device the condition is just reverse. So, for the PMOS input device the input can go all the way to ground the ICMR can go all the way to ground, but on the upper side it is limited you cannot go very close to V D D. So, the input common mode range limited on the upper side in that case another lower.

(Refer Slide Time: 04:11)



So, if we have a scheme where we are just combining the comparator with PMOS input device and the comparator with NMOS input device and then trying to combine their output in correct fashion using a multiplexer we can have a analog multiplexer which is having a select line over here this is a analog multiplexer. So, we have to choose between the inputs of the C P and C n. So, we have the same V in sampled V in going to both of them and you have the same V ref also going to both of them. So, this is your ramping V ref, which is coming from the ramping circuitry and this is the sampled V in. So, this is common to both all I need to do is choose one of them depending upon the input magnitude remember if the input magnitude is larger the n C n will perform properly; however, if it is going lower it will fail; however, the C P will perform properly.

So, I can be basically compared this V in using another comparator with the mid value of the I C mid supply value which is V D D by 2 and if the input signal is higher than V D D by 2 we know that the C n can work well. So, this can become our select signal let us

ignore this and I can put the option one over here and 0 over here one over here means when the select signal over here if I call it select signal if the select signal is high the one input will be selected; that means, the C n will be selected.

So, if the input signal is sorry the input signal is higher that V D D by 2 then I would like to select the; I would like to select the C n. So, I will just put a bubble over here; that means, is I mean inversion. That means, just to follow the sign if the input signal is higher than V D D by 2; that means, is will be going low because I have put a bubble over here and that would mean that this will be one when the input is going higher than V D D by 2 and that will be selecting the C n and likewise in the other direction will be selecting C P and such an analog mugs can be implemented using a simple transmission gate that we have discussed in the last class you can have the t g where you have the V the 2 inputs of the t g coming from the C n 1 the C n and the C P and outputs being combine over here.

And here you can of course, have the select lines you can have the select and select bar over here. So, when the select is high I can select the C n and vice versa I can have the select the bar over here and this is my output. So, and this is an analog marks and we have discussed that the on distance of switches can be relatively very low and as a result whenever one of these mugses are on the corresponding output C P or C n will be connected to the output it is expected that C P in C n are digital values, because they are comparator outputs and therefore, these are going to be full swing signals close to either to V D D or ground and we know that the t g will be able to pass both of these. So, this is one scheme where we can apply a t g based mugs to select one of these comparators based on the input signal level.

Now, one of the question is that the we pointed out that C P works for input signal level which is say higher than V D D by 2 going all the way to sorry is going to work all the signal level going all the way to ground and C n works for all the signal levels going all the way to ground V D D, but it does not work for the signal levels going all the way to ground. So, what should choose over here the choice of this comparator important choice of input devices going to use n or P is it is it important for this one here of course, the we saw that it is critical we are choosing these 2 for different ranges of input operation. However, here we are assuming that this is working for the entire range. So, this is this is this an issue. So, this was. In fact, one of the questions this was raised in our discussion

of line discussions and the reason why we are not concerned about the type of input device over here is that the different voltage is fixed it is just V D D by 2.

And therefore, the comparison operation over here or high gain operation of this amplifier will be of concerned only in the vicinity of V D D by 2 if the input is much higher than V D D by 2 definitely the output will be deterministic if it is much lower than V D D by 2 also again it will be deterministic. So, the critical point for this comparator is only when the input signal is close to be V D D by 2 and for that whether it is NMOS or PMOS input device does not matter both of them are going to work well if the input device if the reference is signal V D D by 2 whereas, for the other 2 what is happening reference is being swept and the critical point of concerned is when the input signal is close to the reference therefore, for the entire range of reference 0 2 V D D and hence corresponding to that inspire entire range of the input signal should be able to work. So, for that the operation is the high gain operation is happening in the common mode fashion because they are the input signal and the V ref are very close at the flip point where the comparator is changing the result changing the output.

And hence for these 2 we have to be concerned about input common mode range; however, for this we do not have to be and therefore, the choice of input device not critical another thing is what about the gain specifications for these comparator then you may be have the specification of the gain for here once again is gain critical the answer would be no, because if the gain is poor than the resolution of its comparator will be poor that would mean that for the V in close to V D D by 2 say V D D by 2 plus say delta for a sufficiently large delta.

The result is not well defined it can be either high or low and this delta can be few tons of millivolt it can be also 100 millivolts in this case we try to keep this delta small whether governed by there is illusion requirement there we try to set the delta within 15 millivolts which is coming ultimately from our requirement of the condition and the accuracy of the a d the precision of A D C and so on. But here that delta is not concerned why because even if the gain is poor and as a result the decision in a relatively wider range is nondeterministic even there is a 100 millivolt you know range where the gain other responses and domestic.

There the choice of C n C P in the vicinity of V D D by 2 will not be. So, critical because if your V in is you know V D D by 2 plus hundred millivolt the V D D by 2 minus 100 millivolts still these comparators both of these comparators can work. So, in that range it is not very critical to choose one of them only when the input signal is far away from V D D by 2 going towards ground or to going towards V D D which is basically 0 plus V t and on the upper side V D D minus mod V t. So, those are the if the input signal is beyond these 2 range these upper limit of V D D minus mod V t. And let us other side mod V t n on the lower side. So, if the input signal is going above and below this side then only the selection of these 2 become critical we have to make the right selection; however, within plus minus 100 millivolts if one of them is getting selected and another one is not selected that does not matter because both of them are out going to operate well. So, therefore, the gain requirement for this comparator is not. So, critical I can have a poor gain whether that you just may be 10 or 20 gain that is also going to be good enough for this particular comparator.

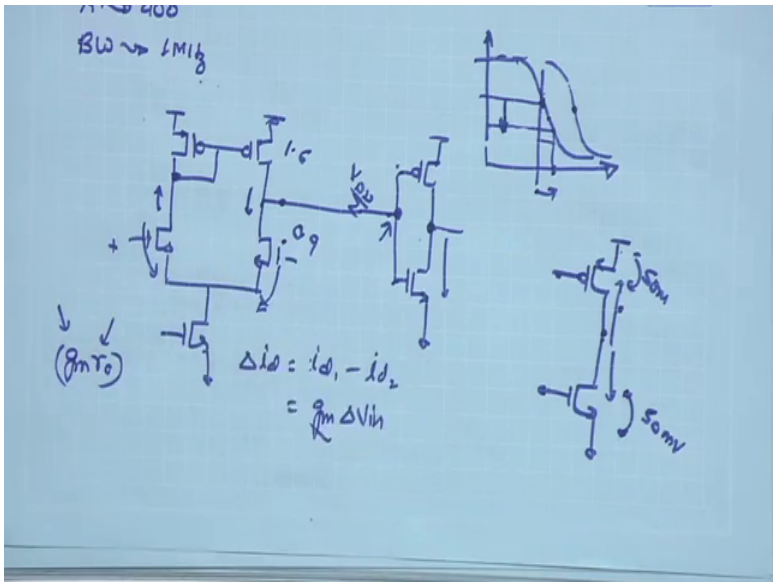
So, if you have a 20 gain difference of 100 millivolts will be amplified to full V D D swing therefore, this is going to relatively going to be a cheap comparator do not need to worry about the gain high gain requirements for this one of course, bandwidth should be fast enough we should be able to response fast. So, that the comparators are getting selected at the right time. So, speed should be enough gain requirements relatively poor still to be safe if it is not hurting our requirement we can still go for gain which is at least say around hundred unless it is significantly hurting our power budget.

And if we see if we look at some results coming from simulations the power budget for these transistors this comparators will be within 2 microamperes close 10 microampere within that and if we are having significantly lower gain requirement for this one the power once again can be lower and bias current can be sacrificed it can be fraction of microampere and still it can meet the required nominal gain just make sure that the gain is sufficient worst case it does not drop below the required value. So, this is going to be a relatively cheaper device as compared to the other 2.

So, this is another way in which we can achieve full ICMR without sacrificing the overall performance without having stringent dependency on the input device sizing of the comparator that we just discussed another very important issue that we would like to mention is the choice of single stage inverters verses 2 stage and interfacing of

comparator and the digital the component which are going to follow the comparator. So, these 2 issues are related and going to play a very important role in designs where we are having final interface between an analogue comparator and the subsequent digital unit. So, let us look into this.

(Refer Slide Time: 14:16)



So, we have seen that ultimate target is around four hundred gain from the overall comparator and also bandwidth requirement is around if I look at it one megahertz in your earlier examples while working on front end amplifier we have obtained this amount of gain from a single stage itself, but of course, in that case the bandwidth for the single stage will also get limited if you try to obtain this entire gain from a single stage the bandwidth also gets limited, but despite that if you are supposed to your trying to get this gain from a single stage unit and trying to just apply the first deferential stage for the comparator operation and trying to interface the comparator with and the next stage which can be just a digital inverter.

For example the simplest digital circuitry; so, if I do away with the second stage what are the pros and cons this is a quite done important issue to be addressed and understood. So, here if I look at the interface between this differential amplifier and the inverter assuming that this is able to achieve a sufficient gain and as a result the swing over here is sufficiently large we are expecting that this inverter will be able to convert the swing into full digital swing because this is able to achieve a overall four hundred gain and

therefore, a small difference in voltage here maybe just 2-3 millivolts of difference between these 2 signals is going to give me or close to full swing at this point. So, in that case I may not even required the second stage and may be able to get the entire gain from the stage there we have 2 cases if you are depending upon this GMRO product of this first stage not even to obtain the overall swing there either you can have a larger GMRO you can have relatively large r o to obtain that while meeting the bandwidth constrain.

Case one if you have large g m if you have large g m; that means, the current g m the difference in the overall current that you get assuming small signal operation delta i d that is say i d 1 minus i d 2 overall that is going to be proportional to g m times delta V in and therefore, for a given V in the g m is large you will be able to switch the current completely into one of the devices for a relatively small V in and if your g m is sufficiently large that further required delta that we have estimated say 15 millivolt the signal is completely able to switch or the current is completely able to switch in one direction that was definitely turn off one of the devices. And as a result we can expect full swing at this point.

For example, if this device is getting turned off because a large g m I in getting diverted completely and this is getting turned off what will happen this is anyway going to be V D D, because there is no path for the current to flow if will V D D otherwise in the other case if this is turning off in that case once again there is no current one and this one. So, this is going to be close to V D D this is turned off and as a result this is there is no current from the PMOS at this point where as this is completely on. Therefore, this will be discharged to ground.

So, in either the 2 cases the g m is sufficiently this note will got going to completely V D D or ground for the given delta V in and therefore, we may not be even need the second stage and we can just put another inverter and go to the digital domain. However, if the g m is not sufficiently large the current will not be switching completely although you may be having expected you would be having a expected the large gain and the expecting a large signal swing over here, but if the current is not switching completely ultimately for increasing swing since the current is not completely swayed and one off both none of these devices are completely off one of the devices will be entering in triode diversion.

For example, if the voltage over here larger here it is smaller and ultimately this voltage is dropping down this is increasing this transistor going to remain in saturation no problem, but if this is dropping while this transistor is remaining on this will ultimately entering into triode division and further gain will be drop and once this transistor entered into triode region the gain of the overall amplifier circuit dropped and it will no longer go down further and it will saturate to a value which is higher than gram it can be almost close to V D D by 2 also if the transistor is not is the sizing is not proper.

So, it can hang midway rather than doing all the way to ground it can be close to be V D D by 2 because the gain has dropped while this node is going to going to go down therefore, on the upper side is also similarly if the signal over here it is larger and here it is smaller once again if this transistor trying to go if this will go up while the current is not switch completely this transistor may finally, enter into triode region because the signal going up and as a result once again gain will drop and once again the voltage may not be able to reach V D D.

So, therefore, the swing can get limited because that current is not getting switch completely and the gain is dropping before the signal reaches full swing and hence it can be risky you are not having full swing over here and then you are connecting an inverter the digital inverter over here to this analog signal. So, if we have say single which is hanging midway say close V D D by 2 in that vicinity and we are applying a digital inverter directly over here what can be the condition none of the NMOS or PMOS will be completely off both of them will be remaining on specially if it is close to say V D D by 2 under this condition both NMOS and PMOS are having sufficient V s g you are having sufficient overdrive voltages as a result you can have a huge amount of static current flowing through this inverter for that duration.

So, as a result you will end up burning a good amount of static current for that small period for the comparator we have you know control on the current by using this bias current we can control the cloro static current over here C mos inverter we do not have current control. So, just depend upon the W by L and the V g s the V g s is sufficiently strong as compared to V t you have the vision V overdrive it will burn a good amount of static current within a small period it can give you a huge amount of current dissipation and it can disturb your power balance that you are trying to create. So, that that is one issue another and it can have cascading effect. So, you can have the next stage also if this

is you know not having full swing is somewhere could close to V D D by 2 the output of this inverter will also be not having full swing in substituent stage it can also burn more power.

In general the characteristics of the inverter is of course, if you are having the transition region gain under water which is sufficiently large and your signal is close to say mid midway in this transmission region even if it is not exactly V D D by 2 and the slope is large you can ensure that if my input is say slightly higher than V D D by 2 the output will be relatively sufficiently lower than V D D by 2 if the gain is large this slop is large and my input is little bit at least lower than V D D by 2 this larger slop showed that the output is sufficiently lower. So, definitely that will help in pushing the output of this inverter further away from V D D by 2. So, that is the property of a inverter regenerative property where if you having input which is at least little bit off set from the trip point of the inverter not necessarily V D D by 2 the trip point of the inverter we can make sure that the output of the inverter is sufficiently further away from the trip point.

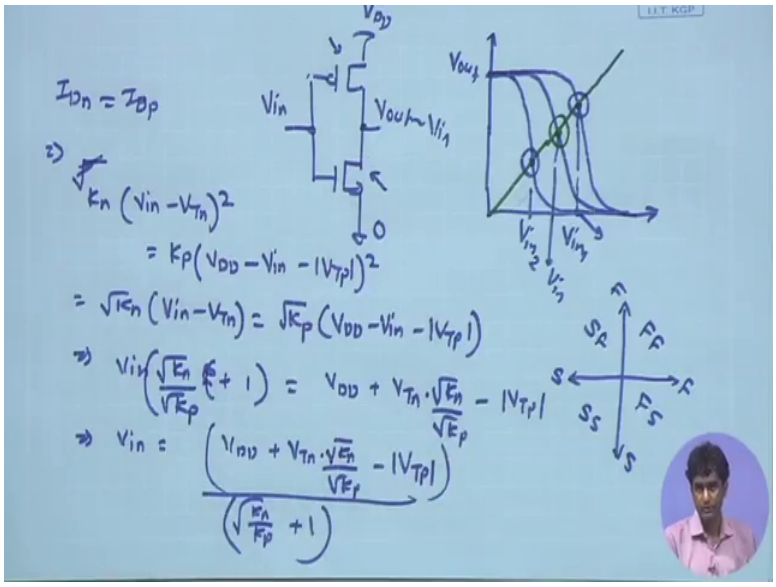
So, but in that case also we can end up burning a good amount of static current that is not a good tactics. So, although you may be able to meet your gain requirement for the first stage would be good to involve or introduce a second stage. So, that it is ensuring almost full swing and it is ensuring that either the output is going all the way close to be V D D up ground. So, that the interface between the comparator and the digital inverter is robust enough it is not leading to static power dissipation in the inverter another critical issue will be the trip point of the inverter that I just mentioned trip point is not necessarily V D D by 2 it is not necessary that midpoint that we are looking at in this transfer characteristic is going to be V D D by 2.

And that is another important issue which plays an important role whenever we are interfacing an analog unit like a comparator output with the digital inverter. So, let us look into the concept of trip point little bit more detail after a short break before we go there we can see if there is any question any question any part we needs a discussion over here.

Yes let us resume our discussion any question regarding the discussion we have so regarding the selection alright. So, let us looking into the conceptive trip point of the inverter which is again going to play an important role for the analog circuits wherever

we are trying to incorporate digital inverters interfaced with analog signals, so trip point is defined as the threshold of the inverter this is the input level for which output is equal to input.

(Refer Slide Time: 24:30)



So if I draw the transfer characteristics of the inverter and look at the V out equal to V in curve which is forty five degree the point where it intersects is going to be a trip point the point at which V in is equal to V out this is V out and this is the V in. So, if you are going for V in higher than this trip point we are expecting that again you are having the output going down and on the upper side once again output going close to the V D D and this trip point can be seen as threshold of the inverter the point at which it is going to the input value at which it is going to switch from high to low.

For example if you have trip point which is higher we expect that this curve will be moving further over here and therefore, this is the value of V in for which it will be switching down likewise if the trip point of the inverter is lower where this expect that this is value this is the value of V in this is the value of V in 2 for which the inverter is going to switch down. So, you can see that the definition of trip point is going to tell us what is the minimum value of V in for which the high to low transition and then inverter will take of corresponding that the low to high transition of inverter will take depending upon the input signal. So, this trip point of course, tells me that the what is effective threshold of the inverter just like the MOSFET as a threshold we can say that the

switching threshold and it depends upon the intersection of V in equal to V out curve and the inverter characteristics over here in order to obtain this trip point and see what are the parameters on which it will depend we can write down the equation for the current in the inverter when that trip point is occurring.

So, when the trip point occurs we are assuming that both this input and output voltages are close and they are somewhere midway they are not close to extremes. So, if I take that assumption for the time being then I can say that this is you know close to say V D D by 2 and I have V in and V out approximately equal to V in this is V D D and this is ground 0 in that condition what is the region of operation for the PMOS and NMOS if I assume that say this is close to V D D by 2 suppose I am taking the middle curve and I assume that this is close to V D D by 2. So, both of them V in equal to V out are going to be close to V D D by 2.

As a result we can definitely see that for the NMOS the gate voltage gain voltage is similar as a result of course, this is going to be in saturation likewise for the PMOS the same thing gate voltage gain voltage is similar therefore, is in saturation therefore, at that trip point both the transistors we can assume they are in saturation and I can write down the current equation for both of them i d n equal to i d P for the trip point and for i d n if I write this as say root let me write down the equation as k n V g s minus V t square. So, this is V in minus V t n square and this is equal to the mos current PMOS current which is equal to V s g minus mod V t square.

So, the V s g is V D D minus s which is minus g which is your V in once again minus mod V t p. So, I can equate these 2 I can take the root k n V in minus V t n is equal to I am ignoring the channel and modulation for simplicity of course, that will also come into picture and this voltages. And from here I can find out the V in if I take the k n upon k P over here I have the k n upon k P and you have sorry this plus one coming over here and this is going to be V D D plus mod plus V t n times k n upon k P minus mod V t p.

And as a result I can write down the particular trip point value as V D D plus V t n k n upon k P minus mod V t P upon root under once again k n upon k P plus one. So, we can see the dependencies over here how they are coming up. So, k n k P is equal to the trans connected parameter of the MOSFET which is equal to mu n C x W by l. So, if I assume mu n C x are constant. So, these 2 quantities are ultimately depending upon W b L ratios

and if I look at older technologies even in 1 meter k n upon k P ration if I talk about the mu n upon mu P ration that is around 2. So, NMOS is faster the mobility the of NMOS is slightly higher as compared to PMOS by factor 2 to 2.5 and as a result if I assume the W by ls are similar this will have that particular factor mu n upon mu P coming in now if I look at the design parameter that is W by L available to us there we can see that if I am increasing the k n upon k P term and if I assume that these terms are getting you know cancelled out almost similar and therefore, the magnitude over here is you know relatively lower if I just increase the k n upon k P the term this denovated term is going to increase and as a result if I see the trip point is going to shift towards lower value.

So, in that case I am having the overall trip point shifting toward the lower value and hence threshold of the inverter or the trip point of the inverter is shifting towards lower value likewise if I am having k n upon k P lower that is I am increasing W by L of P and reducing the W by L of n the trip point will be shifting towards relatively higher values what is the consequence of; that means, the overall trip point is going to determine by the W by L ratios and also the V t n V t n values V t n and V t P values which are not very much in designers control they can vary from device to device significantly.

So, even if the k n k P are set almost equal the V t n V t P value may not be exactly same and likewise you are having in the denominator specially you have an k n upon k P ratio which can vary from unity. So, once again you are having the other parameters also like the lambda which we have ignored coming in the picture and determining the overall trip point. So, that that we have ignored for simplicity nut ultimately lambda also going to play a role therefore, the trip point is dependent upon the sizing of these devices and also the terms like threshold voltages and the lambda and therefore, they are very much process dependent and can vary from inverter to inverter even if you have inverters with the same dimension they can have significantly different trip points.

It can vary by several times of voltage can vary by 100s of millivolts and typically in the C mos process you can have the threshold voltages of NMOS getting higher uniformly that in that case all the PMOS transistors on the dye will be having slightly higher voltage than the nominal case you can also have a condition where the NMOS threshold voltage are going high. So, in that case once again all the NMOS transistors dye will be having slightly lower threshold or higher threshold voltage and the nominal value. So,

both these scenarios can happen NMOS and PMOS can have uniformly relatively higher or lower threshold voltages.

So, we call them process corner. So, basically we have four possible process corners you have the case where you can have the NMOS you can have. So, if I denote one of the access for the PMOS and another one for NMOS you can have a case where both NMOS and PMOS are slow; that means, both the threshold voltages of NMOS and PMOS for all the devices are higher than nominal. That means, the on current will be large smaller and hence the speed will be smaller you can have the condition where both the NMOS and PMOS threshold voltages are lower than the nominal in that case both the devices will be faster than expected, because of threshold voltage will be smaller and current will be faster.

So, it is a fast corner likewise you can have the other 2 corners where you have slow fast one of them having relatively smaller volt threshold voltage and the higher other one and you have the fast slow corner. So, you can have in general these four corners and that would mean that dominantly on an average if you take an NMOS if the device is in slow fast corner or the dye that you are having this slow fast corner; that means, the NMOS will be relatively slower as expected or the threshold voltage of the NMOS is higher than expected and vice versa.

So, in general we can have these four corners and as a result the threshold voltage of the MOSFET or the inverter that you are expecting can significantly vary from, but we have decided for the in the simulation and hence when we are targeting interfacing of analogue signal with the digital inverter we cannot be sure that the threshold voltage of the trip point of this inverter will be V D D by 2 it can vary significantly and in that case the assumption that a given swing say from one point six volt to say point nine volt it will be reliably amplified by this inverter and covert into digital level because the trip point has been set to be you know midway between these 2 that is not going to work in simulation you may be getting some values like this say minimum value over here point nine and micro 0.6 and by sizing the W by I of these 2.

For example, as I said if you increase the W by L of the PMOS the trip point will shift further there will be for the higher over here there is the characteristic will be shifted for that we just saw. So, if you do that then we cannot expect that whatever trip point we

have designed it for say midway between 1.6 and 1.9 after the fabrication the trip point will remain there it can go down also it can go down below one below point nine also. So, therefore, it will fail in that condition.

This is not a very robust case when you are trying to interface the analog output coming from the comparator directly with the digital inverter. So, it will better to convert this swing this signal into full swing using another stage and then applied to the inverter. So, that will lead to a more robust design and it will not be dependent upon process it will not be you know dependent upon the sizing of this W by L of P n n V t of this of P n n.

So, that even you are having changes in the process corner and you are having different corners, because of which the threshold voltages are changing for the NMOS PMOS spare and as a result the trip point of this inverter is changing still you will be ensuring that the output signal is going to all the way to V D D and ground and hence the inverter is going to work reliably. So, this justifies the use of the second stage even if in case you are having a lower gain requirement and you are able to do it with a single stage more reliable design would include a second stage for that you are always ensuring full swing before it goes to the comparator interfaces with the digital inverter.

So, we saw 2 reasons one is the static power dissipation. So, that when the signal is close to V D D by 2 not fully ground or V D D it can be lot of static power dissipation in the interfacing inverter second reason is the robustness of the circuit whether where we are talking about the trip point of the inverter which can vary significantly is not necessarily V D D by 2 as we see it depends upon the device parameters and the W by L ratio of the NMOS and PMOS transistors and that can also significantly vary over process it can be very different from the expected value and hence such an interfacing will not be reliable for this particular stage the gain will not drop unless this output voltage is reaching all the way to V D D minus V overdrive.

So, if the V overdrive is small it can go all the way to V D D till that point also the gain will sufficient likewise on the lower side also the gain will not drop unless the voltage over here as gone down all the way to V overdrive of n and that would mean that you know few tons of millivolt. So, if you are sizing this properly the V overdrive of this NMOS can be within few tons of may be just few tons of millivolt as a result a the gain of the stage will not drop or this or this NMOS PMOS will not enter into triode region in

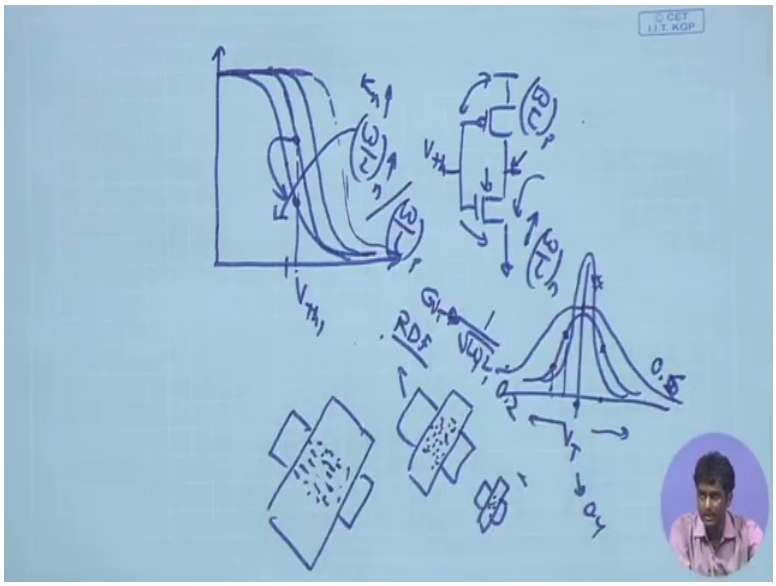
the voltage is over here is going all the way to V D D minus V overdrive which can be very close to V D D or this voltage is going down all the way to just V overdrive of n which is one again very close to ground.

So, you have few tons of millivolts may be 50 millivolt over here and 50 millivolt over here even for this entire range this 2 transistors are still in saturation therefore, the gain will maintained there will no there will not the swing will not reduce the gain of this stage and then you know create problem in the amplification whereas, in this case what is happening if the g m is not sufficient and the swig is increasing the transistors are entering into triode and as a result the gain is dropping and is not able to approach V D D or ground because before it can approach V D D of ground the gain of the circuit has drop

And it stuck to that you know intermediate value and that case interfacing with the digital inverter is going to be a bad idea whereas, the second stage have the opportunity of having full swing because this or this transistor will not enter into triode even this voltage approaches all the way to V D D all the way to ground that is the reason why interfacing with this referential amplifier then applying a digital inverter will be a better option most robust option for the point of view of process variation and also power dissipation .

Any question for the proceeds for the and look into some other design issues associated without comparator. So, we should have safe information regarding the trip point once again if I look at the trip point we can if I am talking both the W by L ratio it is also important to see what is happening if I changing the W by L of n and. So, at this at this point see that we will see if I having the k n k P ration increasing then; that means, that the trip point is going to go lower why it is happening that also we can see. So, if the W by L of NMOS is getting increased; that means, for a let me let me draw it on a separate plot.

(Refer Slide Time: 39:54)



It is more evident having this intuition is important whenever we are looking at the sizing of the inverter which is interface analog circuitry. So, that we are clear about the W by L sizing a requirement. So, in many cases it comes into picture when we are looking at design having mix signal components. So, if I say that I am going to increase the W by L of the NMOS then what we expect to happened with the transfer characteristics this equation trust me the transfer characteristics shift towards the left because the k n upon k P ratio will try to doing this value down trip point down now if I look at what is happening here if I am having the suppose this is my original curve where the trip point is given by say V t h one trip point of the inverter threshold voltage of the inverter and then I decided to increase the W by of this MOSFET.

That means for the same V t h since the V g at W by that has increased I would expect larger current in the NMOS; that means, NMOS has become stronger I have put larger W by L for the NMOS that for the same V t h I expect larger current over here on the other hand they had the same W by L for the PMOS. Therefore, the V s g of PMOS remaining same W by L of the PMOS is remaining same this is remaining same, but I have increased the W by L of n as compared to the original device where the trip point was obtained here.

Now, here if I see that the V f g of the MOSFET is remaining PMOS is remaining same and the W by L is remaining same and for the NMOS. However, the scenario is different

W by L has increased for the same V g therefore, they would expect larger current flow over here and that would maintain that the PMOS also has larger current because they are same device and the only way PMOS can have larger current this voltage should go down right that mean that this voltage must be further down as compared to the previous value that we can see that this curve should shift down from here to here we say that the pull down devices become stronger if the pull down devices becoming stronger it will be able to pull down the inverter from high to low for smaller voltages threshold voltage is come lower. So, the NMOS is the pull down device to pull down the output to ground all the way.

Whatever capacitance over here appearing because of the parasitic it will try to discharge it to the ground; s, if the NMOS is becoming stronger the device over here will becoming larger; that means, it can pull down the device for a smaller input voltage on the other hand if the PMOS is becoming stronger it will take much larger voltage over here to pull down the device is the characteristics shift toward the higher side. So, this is important to you know keeping mind increasing the W by L of the NMOS; that means, making the pull down device longer that will pull down the inverter characteristics earlier lower input voltage whereas, the pull up device of PMOS if I am trying to make that strong it will be it will take a larger input voltage pull it down because the pull up device become stronger.

So, this the direction in which my k n is increasing or another words W by L of n is increasing or you can say that the ration of this 2 quantity W by L of n and W by L of p. So, if I making the W by L n of n stronger as compared to the W by L of P then this is the shift in the characteristics that it can this is very important and whenever we are dealing with interfacing of inverter with analog circuitry this have been constraint one is to be addressed.

In some cases we would like to internationally keep the V t gates on the higher side or on the lower side and remember threshold voltage variation it reduces the if the size of the MOSFETs are larger, so, very shortly discussed the concept of Mofset. So, if the MOSFET devices are larger the sigma V P distribution of the V t becomes sharper. So, sigma of the V t drops with drops with the area of the MOSFET; that means, if I collect say hundred MOSFETs of dimension W by L such a the dimension the product is W and L one the area is W one L one. So, they will have a certain distribution of V t; that

means, I am this is the V t that I am measuring and this is number of samples this is the number of sample. So, I am taking first hundred MOSFETs with having W one L one dimensions the area therefore, the gate area W one L one if I look at their V t distribution some MOSFETs end number of MOSFETs are having V t which is over here another given number of MOSFETs having V t which is over here you know some MOSFETs are having V t which is higher than the nominal this is nominal V t that I expect and along that you have a Gaussian distribution.

If I take another hundred MOSFETs which is having the W by L say four types in that case the distribution the sigma of the distribution also become sharper and distribution become smaller; that means, the spread in the V t become smaller why because one of the important contribute to this sigma V t happens to be the dopant fluctuation when the MOSFET size is smaller in the channel you have under the channel you have some dop dopant which are considering the channel and const they are they are basically determining the threshold voltage and those dopant numbers are ultimately going to vary from device to device.

If we look at say if we look at you know different devices of different dimensions you can have you know the dopant numbers varying very significantly especially if it is scale device another result the threshold voltage which is dependent upon the dopant that can also you know vary is a number of dopant is fluctuating if we have larger devices then the percentage variation of the dopants is also smaller if we have a device area which is you know larger much larger device then the percentage variation the dopant will be smaller because if you are having a very small device for a particular technology minimum size device then the number of dopants countable and the percentage fluctuation that you can get over here will be larger.

As you are going on large increasing the area the percentage fluctuation that you get in the number of dopants over here also reduces with area because here the probability of you know finding electrons per unit area is given and then you have a small area therefore, the probability of fluctuation over here is much larger whereas, the probability of electron per unit area this larger area. So, you having a much larger area over which you are averaging the probabilities and as a result you are having the percentage variation in the absolute number of dopants over here relatively smaller as a result larger number of or larger area of the device larger W L leads to smaller sigma V t this can be

analytically derived also from the MOSFET threshold voltage equation if I assume certain dependence of the threshold voltage on the dopant is random dopant distribution or r d f is one of the major contributor to this threshold voltage mismatch or variation from device to device and if I therefore, if I keep this information in mind for circuit point of view it can be very important because if I increase the W by L of the MOSFET the threshold voltage distribution can be relatively smaller I can I can expect that the threshold voltage of the MOSFET will be close to the nominal value it may not deviate too much.

Whereas, if we use minimum size transistor the variation can be big if you use minimum size transistor that distribution can be much larger and the nominal V t is say point four volt the V t can go all the way to say point 2 volt sorry point six volt can go all the way to say point 2 volt it can be bad if you are using minimum size transistor. So, I i am being aggressive over here, but even in good technologies you can have at least hundred millivolt plus minus variation for a minimum device whereas, if you are having say larger devices the distribution become sharper because the sigma V t reduces. So, larger device W by L larger W and L of the PMOS or NMOS will ensure that the V t of the device is close to the nominal value and then I can have more assurance regarding the threshold voltage of this inverter or the mismatch between the transistors can be relatively lesser.

So, I can be more deterministic that if I am choosing a certain W by L ratio for this my V in or the threshold voltage the trip point of the inverter can be more deterministically obtain from this equation, because these are not varying so much distribution or the variation of these two components is not so much so that is the another important point to be taking care of, and while looking at the analog circuit differential amplifier the operation amplifier mismatch an offset once again this point has to be considered.

Let us take a break and see whether we have any question at this point before we can resume our discussion.