Analog Circuits and Systems through SPICE Simulation
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Lecture - 40
Comparator Design

Welcome back. Let us resume our discussion on the Comparator Design that we are looking at. Remember the starting from the ADC specification arrived at the some of the important specification of the comparator.

Before that we discussed some other constituent of the ADC, the single slope ADC, namely the sampling unit. Where we discuss the transferable details of the sampling unit whether the non idealities that have able to come when we look at transistor level implementation of a simple transmission gate based sampling switch. And we after that we looked into the ram circuit, what are the issues associated with building a ram circuit, we looked into the required value of the capacitors and the charging current magnitude. And also the implementation of the current source which is supposed to be used we should have the vision the wide range as well as a relatively flat slope respect to the output voltage. Or in other words high output impedance, but low output low voltage headroom.

And next we are we also derived the specification of the ADC starting from sorry, specification of the comparator starting from the high level specification of the ADC. We looked at the required clock frequency for the counter and from there we arrived at the required gain and the bandwidth of the ADC.

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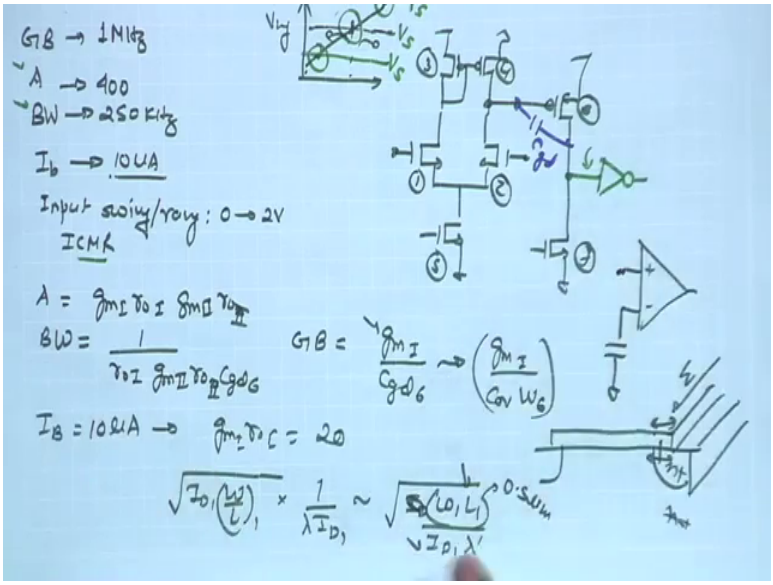

And the required gain value was around say 400 and the gain bandwidth product that we are looking it was around 1 mega hertz. We have the bandwidth of the amplifier around 250 kilo hertz. So, this is these are the values we estimated and based on these we need to look into the design of the comparator and specify the first of all the sizing depending upon the gain and bandwidth values. Also, one of the target should be to minimize the bias current, because ultimately it is a area constraint and power constraint design. Where we are, we are supposed to minimize area of the single channel acquiring above potential along with that you are also supposed to minimize the overall bias current in different analog units.

So, we have seen that the power budget allocated to the front end design, front end amplifiers that was close to say 10 to 20 microampere. Like was in the filtered we had relatively lower bias current because of use of short circuit is for implementation the Gm-C filters and therefore, that that block was relatively low power consumption block. And likewise in the ADC we need to look at the different power components and make sure that the overall power dissipation is relatively low or relatively limited as compared to the front end, we should not go beyond the front end otherwise the ADC will come the dominant power consuming block.

Remember the decision regarding the choice of the ADC topology also depends upon the performance of the ADC that we are able to get. It should able to meet the sampling

spirit requirement, it should also be able to meet the resolution requirement, at the same time it should also be able to satisfy the power constraint. We should be able to get the required resolution and sampling spirit with the given power constraint.

So, looking at the selected topology of course, we have to make sure that the constituent building blocks namely the comparator, the sampling unit the ramping circuit and the digital units taking together it do not consume lot of power. I would we would like to limit the total power budget may be lower than 20 microwatt or may be relatively lower than that so that, it is power budget is relatively smaller fraction of the entire power budget allocated to the signal processing will change. Towards that in we can set up a convenient upper limit on the bias current that we are going to apply for the comparator; if you look at the different blocks that we have discussed so far.

In the analog domain the sampling switch the ramping circuit and the comparator, the block which is consuming static power is basically the comparator. And therefore, we expect that in the analog domain the comparator is going to be the most power Henry unit in the entire ADC. And therefore, it would be important to minimize power dissipation in the comparator.

And therefore, if I set a constraint upper limit of bias current say 10 microampere for the comparator, we can start with that constraint and see whether the most important criteria of the gain band gain and bandwidth is being met. Along with that we also have the constraint of input swing if you remember the input swing or input common mode range that would be dictated by the maximum pick to picking swing provided by the last stage amplification.

And we have assumed we have seen that it is convenient to get almost nearly full swing a signal from the last stage amplification, if you have a common source stage after that if I am forming the last stage of the op amp, then we can expect almost full swing coming out of the stage. And hence the input swing I can say input swing or input range that the comparator should have is going to be almost equal to V DD 0 to V DD in our case 2 volt.

And it not be wrong to equate this required input swing to common mode range of the amplifier that you are building the comparator that you are building. I can write this at input common mode range, I will see why it is, equivalent to input common mode range.

So, if you look at the overall operation of the comparator that is going to be connected to our ramping circuitry and the input signal. Suppose we are having the 2 stage amplifier as our comparator, remember the purpose is to detect the cross point when the V ram or the ramping signal on the capacitor is crossing the reference signal V ref.

This is the point at which the comparator is supposed to make the transition. So, if the polarity is such that you are having the input signal or the input signals coming at the positive terminal, you has a sampled inputs coming as the positive terminal and you have the V ram or the capacitor voltage ramping up on the negative terminal. Then the transition between high to low should happen close to this point. If you have far away from these 2 points and the comparator gain this large enough definitely the comparator output will be deterministic.

If the V ref is sufficiently different from this sampled value of V in definitely the output will be close to be ready or ground. But the moment V ref approaches the sampled voltage that is that here that is the region the or crucial instance at which we should be getting, timely resolution timely switching off the comparator. So, if the response to the comparator is fast enough and the gain is sufficiently large, whenever there is a whenever the ramping signal crosses the reference or the stored sample single by a small amount delta V it will be able to switch provided delta V times a is equal to the full swing as we have designed earlier.

So, we are interested in the comparator transient close to this particular point and therefore, at that point we can see that both these signals are going to be almost close together right. And at that particular point I have to make sure that the comparator is going to work fine for the sampled input level. Because if the input level sampled is too low I would expect that the comparator should work fine while the V ref is very small, the ramping voltage is very small equal to the sample input voltage.

Likewise, on the other hand if the sampled voltage is constant and it is pretty large we would also expect that the comparator should also work fine, it should transients the transition of the comparator should be fast enough even when you are a ramp is approaching the sample voltage which is high. So, irrespective of the sample input voltage at all this points the comparator should be well behave.

And for that it would require that the input common mode range of the comparator is large enough starting from 0 all the way to V DD, because as we see the critical point is when these 2 signals are close together the sample signal V s, V s and V s and the ramping V ref is whenever we are getting close together; that means, the comparator is the both the inputs of the comparator are close together and we are supposed to detect a small differences change in polarity of V in 1 minus V in 2 at that regular point. And for that we much make sure that even for low input voltages as well as very high input voltages of approaching ability it should be working.

And that is the definition of input common mode range it is, if you want to make sure that the gain of comparator is sufficiently high all the transistors in the in the amplifier are maintained in saturation for the entire range of the input common mode level. That is termed as the input that that maximum range for which all the transistors, maximum range of the common mode input for which all the transistors remain in saturation that is termed as the input common mode range.

So, essentially for reliable operation, but we are looking at is that the input common mode range of the amplifier should be rail to rail; that means, it should be able to handle rail to rail input swing. That means, when both the inputs are close together and you are you are having basically effectively common mode applied as the input common mode input applied at the gates, the amplifier should be able to operate with high gain for the entire rail to rail swing of the common mode or another word it should be able to maintain high gain for the entire range of the input common mode.

So that is one of the time requirements and as we will see as per our previous one of the main challengers will be maintaining the input common mode range. You of course, have the requirement for the gain and bandwidth which once again may not be. So, critical in this case because ultimately you are talking about an open loop amplifier where we can have relatively higher bandwidth and open loop gain although we sufficiently large. So, these 2 may not be very critical whereas, having a large input common mode range that will become major bottom neck for the comparator that we are looking at.

So, for looking at the gain and bandwidth once again we can just identify that what are the quantities; what are the transistor parameters which are going to affect my gain and bandwidth. And that is going to give me the direction for sizing what approach should I

take which transistor should I size in what manner. What should be the channel and what should be the bias current and so on. In order to size the transistor in appropriate direction, if you are not meeting aspects you can go back and you know change the sizing. So, if you just look at the application that we are concerned with here, we are expecting that the output of this comparator is going to be given to some digital circuitry because there is a supposed to be a digital level. If it is not having full swing then probably we can keep an inverter digital inverter which can convert this comparator output into full swing.

We will be looking into the details of digital comparator digital inverter and interfacing with the analog circuitry what are the associated concerns. But ultimately we want a full swing digital output out of the comparator that is the function that you can ideal comparator so we would like to have this full swing. So, in general for the digital comparator or sorry digital inverter the parasitic capacitance at the input node may be once again of the order of few from femto farads to at the maximum tense of an femto farad.

And therefore, the overall parasitic capacitance over here may be still dominated by the transistors of the amplifier itself. Therefore, what we can say is in the overall case if you are not having any significant load capacitance over here in that case the all over here can become the dominant one. Of course, it depends upon condition if your comparator output is feeding a lot of other logic gates and you are having a lot of other digital circuitry being driven by this output, then it can become a dominant load you can have a large capacitance over here.

But if I assume that it the load is sampled just a simple inverter which is minimum size, then this point may be giving you the dominant whole. Because you are having at least a miller multiplication for the C gd for this particular MOSFET. And as a result for similar dimensions of the MOSFETs and similar value of I D similar value of r o we expect that the miller multiplication of C gd will provide larger capacitance, larger effective capacitance at this node and hence this can be the dominance whole limiting overall bandwidth.

So, effectively what again right is that the overall gain of my comparator which is going to depend upon say g m 1 r o 1 and g m 2 r o 2. And the bandwidth if I say is going to

depend upon the first node over here, I can write this as 1 upon r equal and C equal and that is node and therefore, we have the r o 1 of the first stage and C equivalent if I assume once again that C gd is dominant components miller multiplies C gd is the dominant component then I will have the gain of second stage g m 2 r o 2 times the C gd coming into picture, C gd of again I can write it down as C gd of 6 coming into picture.

So, again I can preserve the roman letters for depicting the stages and the specific numbers the roman the decimal numbers to depict the transistor number. So, C gd is basically appears as the effective load capacitance and we are call the miller multiplication you are going dominant all over here. If I look at the gain bandwidth product once again I have the g m 2 r o 2 getting canceled and you have r o 1 getting cancel and you are having effectively g m 1 upon C gd 6.

Determining the gain bandwidth product and therefore, we would need a if you want a sufficiently large gain bandwidth product you should make the g m 1 sufficiently large. And what would C gd 6 depend upon approximately if I say it would C gd 6 depend upon? Approximately if I say it is going to depend upon the C overlap where C, overlap is the overlap capacitance per unit width of the MOSFET times the W of m 6. Remember how does the C overlap comes into picture in the saturation reason you have the C overlap coming, because of the C gd coming because of the C overlap because of the gate overlapping with the drain and drain region.

And then the magnitude of this effective capacitance is proportional to the sorry the magnitude of effective capacitance which arises because of this overlap is going to be proportional to the W, So larger is the W larger is the effective area of this overlap. So, it not So much dependent upon L it is dependent upon the L overlap which is technology parameter and W. So, we can say that this is going to be a dependency of the gain bandwidth product and we have also the dependency of the gain and the bandwidth individually.

This can be the equations which are going to govern our design steps based on this we can iterate with a given starting point and try to see in which direction to move. I can start with bias current budget say I B equal to 10 microampere. And for that I have the overall gain to be determined, if I assume once again that I am bias forgetting the game equaling to stage here. Therefore, again of 20 from it is stage. So, g m 1 r o 1 I am

targeting to be 20 like ways g m 2 r o 2 also I am trying to be trying to set 20. That would imply g m 1 r o 1 is equal to around 20 and from here I have the dependencies of both this terms.

Again look at the dependencies root you have the bias current I D 1 in the first stage and W by L of the first stage and likewise r o you have 1 upon lambda I D 1 and again lambda is depending upon lambda dash times upon L. So, this is a quantity which is inversely proportional to L. So, I will get L 1 in the denominator. So, if I assume that the r o of these devices dominants in that case I will get the lam sorry, W 1 L 1 and you have the I D 1 coming the denominator and you have the lambda dash. So, basically the design parameters that we see the dependencies are W 1 L 1 upon I D 1 for the m 1.

And if I assume that we are choosing L 1 which is common to all transistors just to get the sufficient r o we can keep the same length almost the similar length for all the transistors remember here we are not worried about noise constrain. So, we do not have sizing constrain on l So severely. So, let us assume that we are going to determine a certain L for which we can find out the required W 1 so that, we get a certain gain.

So, let us say that for the I D budget that we have chosen 10 micro we can divided into 2 halves. So, I can assume 5 microampere bias current over here another 5 microampere bias current over here. That gives me the I D 1 of the first stage. So, this is something we have started with and likewise I have the L 1 which I can start with, I can start with a nominal value of L 1. We can keep it say 0.5 micro meter and you have a I D 1 in both the stages for that basically I need to determine what is the W 1 so that, you get a sufficient gain of 20 from the first stage.

So, for this L 1 I can determine the value of minimum value of the W 1 so that, again of around 20 is achieved in the first stage. And likewise if I use the same channel length in the output stage and is almost similar bias current output stage I have the corresponding value of r o 2 coming into picture and therefore, that g m requirement is also similar.

And therefore, the W by L and r o r 1 to be related over here; so one I have this W 1 and L 1 in the first stage determined said that for this particular channel length I need a certain W 1 to get 20 gain. It also gives me the W 1 for or the W for the second stage transistor. And also we have assumes that the channel lengths are similar. So, I get the W 1 for the second stage transistors also to get the similar g m 2 r o 2 value.

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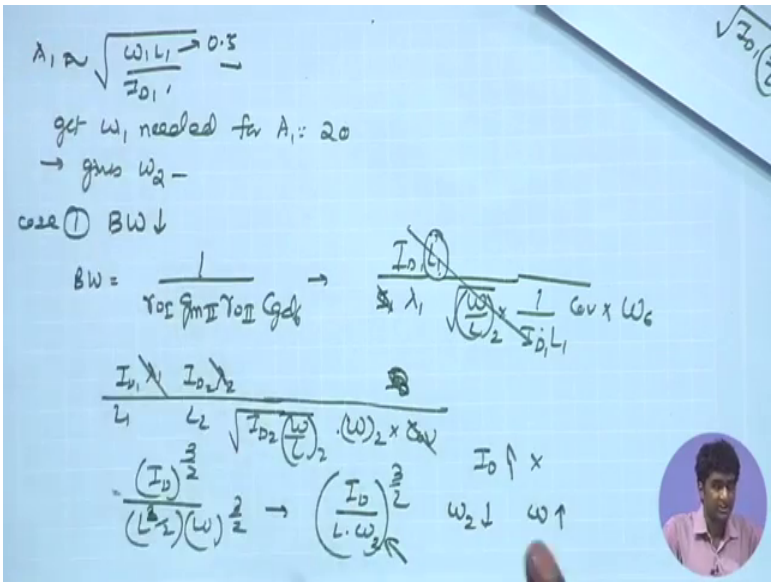

Now the next thing is, once we once for this once for this A 1 which is root under the W 1 L 1 upon I D 1 this is the, this is a proportionality. So, once for this I have determined the W 1 required for a selected 0.5 micro determine get the W 1 needed for a of 20 A 1 of 20. This also gives, also gives the W 2 for the input stage of the, it also gives the W of the m 6, because their g m are taking to be almost similar. So, it is also gives you that W 2 of m 6 and also I have the L of the m 6 taken as same value. So, I have the W 2 determined and corresponding to that I have the bandwidth determined by the equation over here.

So, if I have the overall bandwidth given by r o 1 g m 1 r o 2 C gd 6. So, I know that if I am keeping the same W 1 the bandwidth is mainly going be determined by the quantity over here. So, for the predetermined value of r o 1 g m 1 r o 2 and the C gd 6 which is ultimately coming from the W by L or W of m 6. I can check whether the bandwidth condition is met. If it is not met then once again we have to go back and pick my choices over here so that, I can move in the right direction. So, I can set the game and checking for the bandwidth.

So, if the bandwidth condition is such that the obtain bandwidth is much lower than what I expected. Then I need to go back and twist the parameters over here such that the gain is remaining more or less intact, but the bandwidth is in our hands. So, in order to do that once again we can have several options over here. So, suppose case 1 you have the

bandwidth lower than required. So, in that case I would like to keep the gain as it is while I would like to increase the overall bandwidth. So, if I say that this is the quantity on which my gain dependent and I have to you know increase the overall bandwidth while keeping the gain constants. So, I would like to keep this ratio almost similar while I can try to go back and look at the bandwidth equation and try to increase this quantity.

And here once again if I look at the bandwidth I have the bandwidth given by r o 1 g m 2 r o 2 and C gd 6. And as we have seen this quantity once again I have r o 1 given by I am just writing the design parameters on which I am dependent. So, I have the r o 1 given by 1 upon lambda I D 1. So, I have lambda 1 I D 1 which is again our chosen quantity and this is once again proportional to L, So this is L 1 also virtual than quantity already.

And then I have the g m 2 which is once again going to depend upon root under W by L 2 and you have the r o 2 which is once again depended upon I D which is similar in both the cases I D 1 times L 1, which is also similar in both the cases and then again C overlap times you have the C gd 6 which is depended upon W 6. So, once again this is the bandwidth I have to, I have to increase the bandwidth while keeping the gain constant So, I should make sure that this product W L upon I D is remaining all more or less constant while I am able to twick this quantity over here and the parameters over here so that, the bandwidths get improve.

So, if I look at the I am sorry, if I look at the overall quantities over here. So, I have the bandwidth dependence on I D definitely pretty strong. So, you have the I D sorry, So I will just adjust, I will just messed up let me write it down once again. So, you have r o 1 which is I D 1 times lam lambda I D, so basically this is lambda dash upon L 1 and likewise you have r o 2 which is I D 2 lambda 2 upon L 2.

And you have the g m 2 which is going to proportional to I D 2 W by L 2 and you have the C gd 6 which is proportional 2 W 2 times the C overlap, which is the technology parameter this is not in our hand likewise these 2 also not in our hand. So, I can get rid of these and I am left with this particular quantity. And once again if I assume that the overall if I assume that the overall bias current similar in both the cases. So, these are just going to be the same values of bias current.

And therefore, I have a strong dependence on I D. So, I have I D reward of 3 by 2 coming over here to and then I also have L square coming over here or other L to the

power 3 by 2 coming over here. And likewise I have we can say W 2 times should have a W 2 So, W 2 the power of 3 by 2 over here. So, these are the quantities and swing So, I D upon L times W to the power of 3 by 2. And as a result I can, I can, So, this is W 2 I can the target would be finally, to increase this quantity while keeping the other one same. And to do that one option is that you can, you can increase the I D 1. So, we can look at one particular option let us increase I D and that would increase the power consumption over all and here correspondingly we have to increase the W and L product so that, the overall gain is reduced.

So, power consumption if you want to keep it under control we would like to you know, avoid this option second option maybe that we can increase the L and W 2. Now if I increase the if I, if I reduce sorry, if I reduce the W 2 that is another option. So, for the given L if I am reducing the given W 2 while I am increasing the I D whether same factor that can be an option. So, I can increase I can reduce the W two so that, the bandwidth goes up. And now I have in the second in the first stage of course, the gain will remain almost similar if I am not taking this parameters, but if I reducing the W 2 I will end up reducing the gain of the second stage which is the g m 2 of the second stage. And that can be compensated for example, by say increasing the W 1 of the second first stage.

So, I can go up and increase the W 1 by the same factors so that, the A 1 is going up by the same factor where as a 2 is going down little bit so that, the A 1 into product is being maintained while reducing the overall or increasing the overall bandwidth. So, we can we can see the directions to be taken up. So, this is the overall gain can be you know bifurcated in an uneven fashion I can try to divert more gain toward the first stage in lesser toward the second stage. And tried to push the pole towards higher frequency by choosing a W 2 which is smaller because smaller W 2 would imply a smaller C gd and hence higher bandwidth lower miller multiplication and higher bandwidth

So, this is another concern that we can have. Now if we are able to do that another target would be that we would like to reduce the bias current also as much as possible so that, the green and when they both are maintained while achieving limited power consumption in the amplifier. So, for that we can see once again these 2 operations if we have to lower the power suppose we have achieved is appropriate bifurcation between A 1 and a two so that, the overall gain and bandwidth has been know being met.

Now, if that is being met now other target is to check whether we can reduce I D further. So, again these 2 equations are going to give me some direction regarding that. So, we can see if I reduce the I D over here, the gain in the first stage may go up once again. But however, the bandwidth over here will getting will be getting limited. And however, once again if I want to keep the bandwidth also sufficiently high that would mean that I need to once again reduce the L. So, rather than choosing the same and I can go for an L 2 which is smaller.

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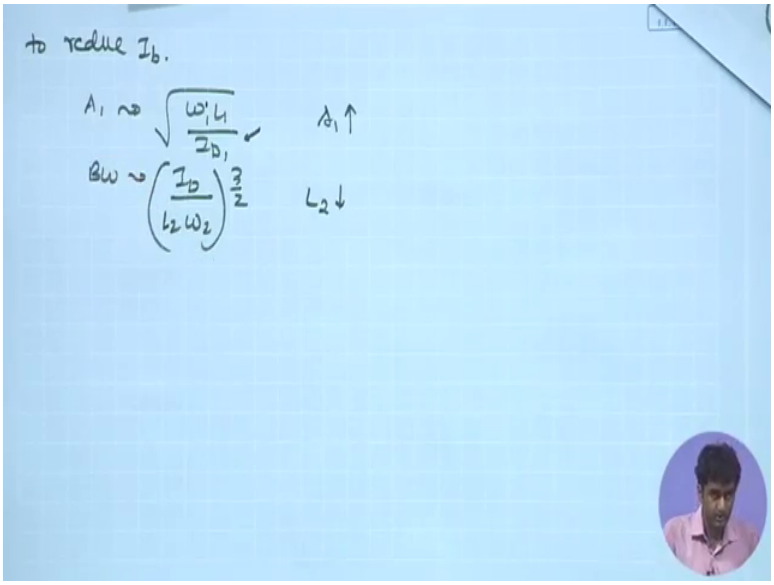

So, in order to reduce to reduce I bias once again I look at the 2 equations the gain of the first page which is W 1 L 1 upon I D 1. And I can look at the overall bandwidth dependency I D upon L 2 W 2 to the power of 3 by 2. And suppose by the previous step we have obtained a proper bifurcation of gain A 1 is sufficient, a 2 is also sufficient we would and we are meeting the bandwidth. Now our target is to say our target is to save some bias current by pushing the I D down.

So, if I push the I D down here once again we are getting reduction in A 1 sorry, increasing A 1 A 1 will go up. At the same time in order to keep the bandwidth same I will have to either lower L 2 or W 2. So, if I do that say I reduce the L 2 by the same magnitude. So, that would once again imply that the overall gain for the second stage which is also proportional to root under W 2 L to open I D to that will be going down and in order avoid that once again I have to make sure that the gain reduction in the second

stage is you know corresponding to the gain increase in the first stage. So, if the magnitude that similar then I do not worry so much.

So, once again I have an option that despite reducing the L 2 and reducing the I D simultaneously to keep the same bandwidth, I can achieve overall similar gain because of gain the first it has been made less exactly higher. So, these are the directions we can take a step by step. And if we are aware of the dependencies that from where the dominance is coming from where the r o the significant r o part is coming which device dimension affects the parasitic thing what manner. So, then we have the right directions we can we within we can make informed decisions about the sizing.

Of course, in the simulations whenever we twist the device dominations we can get the appropriate part based on the intuition based on the information about the dependencies that we have we can get the appropriate part. But if we have clear information about the dependencies even without these derivations at least if we have the higher level information in mind that, how the critical pole is getting originated, how the bias current how the sizing of the input device going to improve or degrade the gain on what critical parameters which devised dimension the bandwidth is going to dominate depend, based on that we can do the sizing the right direction.

So, here we sure that we started with the certain given bias current and certain channel length and assuming equal gain division we looked into the W L required for obtaining a certain gain, because we have the W L of the input device determining the overall gain for a given I D and L. And then we went to the bandwidth component and verify whether the bandwidth is being met if not then once again we have to twist these 2 quantities in a certain way so that, the bandwidth is increase without decreasing the gain. And second thing is we also need to reduce the power consumption for that once again we can try to reduce the bias current while making sure that the gain is maintained and the bandwidth is maintained while you know meeting the power specks.

So, this is the way we can approach a design problem, just having the right direction regarding the dependencies is going to help us in achieving the right specks for the gain bandwidth as well as minimizing the overall bias current. So, there is no unique I will go with them so, there is no unique set of steps. Depending upon the specification depending upon the requirement the load conditions etcetera, you may have to look at

your sizing consideration. If the condition would have been different and have been and you had a large broad capacitance over here, so is that the bandwidth dependency is really over here. Then the sizing constrain would be different.

So, here just try to derive the sizing consideration for this particular condition. So, this is regarding the sizing with respect to the gain and now again and bandwidth while receiving a power consumption. Now the other constrain that we mention very beginning is ICMR where, are input common mode range must be full swing, close to full swing. There if we look at the criteria, the input device size is going determine the ICMR on the lower side.

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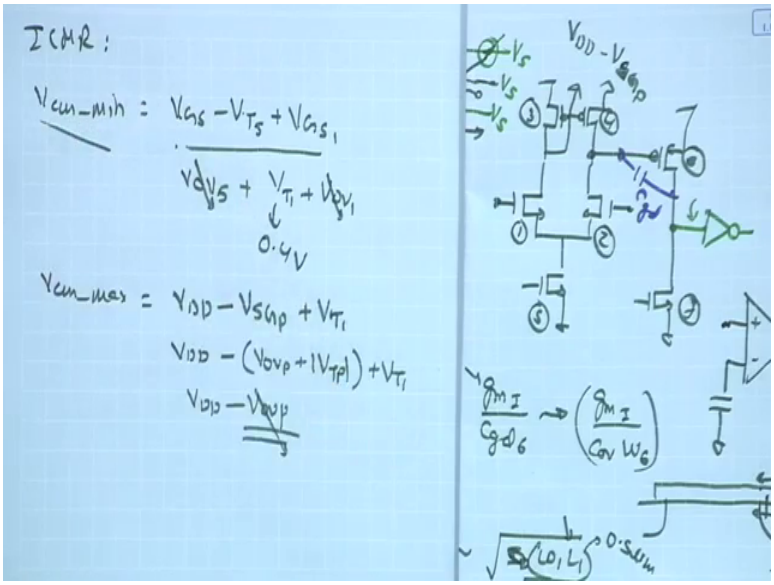

Remember, what is the minimum input common mode voltage that you can apply at the input? If I look at the I see my requirement which I said is going to be more critical than the other constraint of gain bandwidth and power. So, if I look at the ICMR the V cm-min depends upon the V G 5 minus V T. For a given V G 5 bias point over here V G 5 minus V T is the minimum voltage and plus V G s of 1 is the gate voltage of the input device. So, this is the minimum gate voltage that you can have while keeping the m 5 in saturation. If you go below that then the drain voltage of m 5 will be following below V G minus V T and as a result this trio this transistor will be entering to into trio region. And hence if I look at this overall quantity we have this term which is basically represented as a V overdrive of m 5. And I can of course, try to size the m 5 as much as

possible so that, the overdrive voltage was down. Remember the overdrive voltage is depends upon the size inversely.

So, I can I can size them 5 larger for a given bias current so that, V overdrive goes down V G s 1 can also be written as V T 1 plus V over drive 1 because V overdrive is once again V G s minus V t. So, this is V overdrive 1 once again I can depending upon the bias current I can afford to increase the W by L or I can check whether for the given W by L that is coming from our previous step the V overdrive 1 is sufficiently small. If you try to change or reduce the V overdrive here then of course, remember that the gain and the bandwidth gain going to get affected. So, if you try to improve the overdrive voltage of m 1 then of course, you have to back a node raid and check whether you are gain bandwidth requirements some are getting violated.

So, suppose we are having sufficiently low overdrive 1 and overdrive 2 because bias current is sufficiently small. So, a nominal size of W by L for a even you know W by L of around 10 or 20 may give you overdrive voltage which are sufficiently small may be few tons of mill volts. So, in that case I can ignore these two, but this is the component which is remaining which is going to say 0.4 volt or nominal MOSFET. And therefore, in the lower side these are the V T of this transistor ultimately is going to limit my V cm-min.

On other hand the V cm max I want to say, V cm max if you are common mode voltage is increasing remember that the drain potentials over here remain almost clammed to the V DD minus V G p. So, this is V DD minus V G sorry, V G p minus V SGP. So, this is a if I assume that this is the source to gain potential drop V SG of this P mods. So, this potential is V DD minus V SGP. And remember for this definition on this I have with current miller load if you are increasing this input gate potential.

If I assume that both are them are close together the output potential over here will be close to the direct connected voltage over here, this is be following there will be close to the required value V SG V DD minus V SG. And as a result the maximum potential you have at the gate of m 1 and m 2 while keeping these 2 in saturation is going to be, V DD minus V SGP plus mod V T a plus V T n or V T 1 or V T 2.

Because, remember if this is clammed to V DD minus V SG and you are trying to increase these 2 gate voltages ultimately these 2 transistors will entering to trio to when

the gate potential crosses the drain plus V T. So, once again we have, I can represent this V SG as the V overdrive of P plus mod V TP. And I have V T 1 So, if I assume that V T n or V T 1 and V TP are almost similar then I am left with just V DD minus V overdrive P.

And therefore, if I choose the W by L of these 2 transistors sufficiently large over here, I can reduce the V overdrive significantly. So, remember that in the bandwidth and gain also this do not play a very significant role as a the given condition. And therefore, I can afford to increase the W by L of this transistors so that, the V overdrive is almost negligible as compared to b t and I can safely increase the upper V cm-max. Therefore, the limitation is coming from the lower side in this case V cm-min for the difference amplifier with n mods input.

So, let us see couple of ways in which we can mitigate this and we can achieve full swing or rail to rail input common mode range so that, our ADC can work for the entire range of the output provided by the analog amplification chain.

Let us take a break before we can resume our discussion.