Analog Circuits and Systems through SPICE Simulation
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Lecture – 04
Basic Analog Design Part - II
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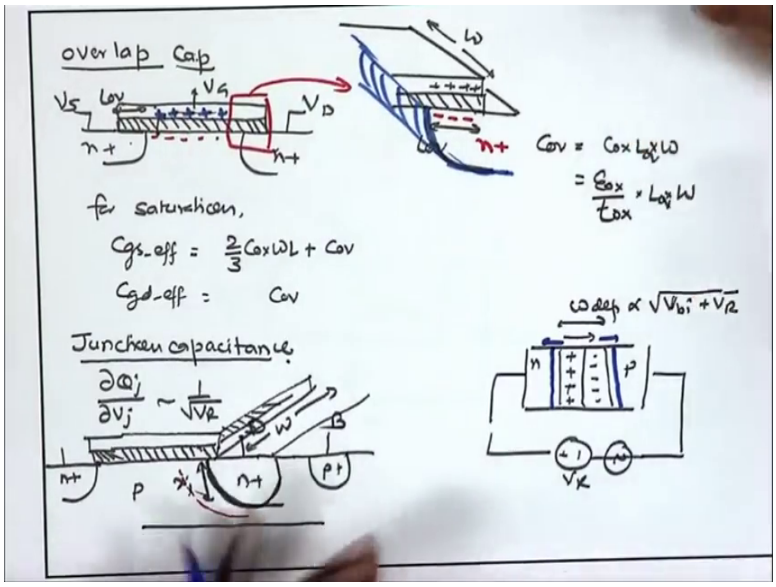

So, in a fabrication process inherently we have an effective overlap length between the gate and the source and drain regions. If this is the metal gate V G and we have the drain and the source. So, there is an effective overlap between the gate terminal and the source and the drain region. And in fact it happens to be important to maintain this overlap, because it facilitates continuous channel, because of process variation suppose in certain cases a channel gets ends here then you will not have the gate or the channel region completely in contact with the source and drain. So, by mistake suppose in process variation the channel ends right here the gate ends right here then the channel be broken. So, it is safe for to have this overlap. So, in intentionally also process technology allow this effective overlap length and that is the technology parameter; Ts and c 180 nanometer will have a characteristics overlap length which is present in their device. So, that depends upon the foundries process.

So, this region the positive charge on the gate which is uniformly distributed all throughout the metal; if I zoom out this region and look at the phenomena that is happening there. So, in this region what is the positive charge you are putting that is not balanced by the channel charge. We said that the positive charge in this region are balanced by the negative charge in the channel; whatever positive charge you put in the middle region just above the channel that is balanced by the negative charge in the channel. But positive charge on the metal which is overlap with the source and drain region that is balanced by a large number of electrons already present in the n plus region.

So, more electron get attracted and accumulated towards this oxide interface and that is how this get balanced. So, it is not dependent upon whether the channel is created or not created it is always present, whether it is saturation, whether it is triode off condition; this charge is always going to be present because the moment you put some positive charge here you are attracting more number of negative charges towards the oxide interface and that leads to an effective capacitive effect capacitive phenomena and that can be also incorporated or clubbed with the cgs or cgd. So, both cgs as well as cgd are going to have this effective component which is once again dependent upon the L overlap the W and the Cox.

So, C overlap can be just written as Cox times L time W that is epsilon ox upon tox times L times W. Because that is L overlap sorry L overlap is the overlap length multiplied by W gives you the area of this effective capacitance coming between gate and source and gate and drain they are always present. So, I can write down for saturation region cgs effective is going to be 2 by 3 Cox W L plus the C overlap. Likewise cgd effective only C overlap, because there is low capacitance coming because of the channel charge only have the overlap capacitance.

Now let us also talk about the junction capacitance. So, we know that in a diode when you are having some reverse biased applied you are having say n type and p type you are having some positive charge in the depletion region on n side and some negative charge in the depletion region on the p side and there is an electric field. And if you are applying say a reverse bias a DC reverse bias say V R and then you are on the top of this you are applying some AC signal trying to change the V R either making it little bit more positive or little bit more negative. So, result of this is expansion and compression of this

depletion region. If you make the V R more positive we know that the depletion region of the diode increases it widens right if the W depletion that is a depletion region of the diode it is proportional to V bi the built in potential plus V R. So, if you are increasing the reverse bias potential the depletion region increases as a result the stored charges increase.

Once again, whenever you are trying to apply a AC signal across this diode there is a charge storage mechanism which is increasing or decreasing the stored charge in this device. And that once again leads to a charge storage mechanism. So, I can define this junction capacitance as dQ junction by dv junction what is the change in the charge across the junction that you obtained by changing the voltage little bit. That is going to be the definition of junction capacitance.

So, in general this can be a non-linear relationship. As we see the W depletion is dependent upon the root under V R, likewise the total channel charge is going to depend upon root under V R. So, dQ by dv is going to depend upon 1 upon root under V R. So, we can say this is going to be something like root under V R relationship.

So, the same phenomena of junction capacitance that is the charge storage mechanism is present in the MOSFET, because MOSFET inherently has this p n junction in built between the n plus source and drain and the substrate for the NMOS and likewise p plus source and drain and the substrate for the PMOS.

Once again, whenever we are changing the overall potential between the source say you know let us call the drain and the substrate; substrate potential we have seen that it needs another contact so you can assume there is a p plus contact for the substrate. So, this is the body terminal as we have seen I have not drawing the source part let me draw that also n plus to the source.

So, here whenever we are increasing the drain potential we are making this diode between the p and the n more reverse bias. So, we are going to increase the effective depletion region formed between the n plus drain and the substrate. And therefore, we are again playing with that stored charge in the depletion region. And that leads to the effective junction capacitance. And we can clearly see that this again is going to depend upon the total area that is the W of the MOSFET. So, here we have to look into the

direction perpendicular to the paper to the sheet and that determines the total W of the MOSFET, and then you have some dimension for the junction you can call it xj.

So, the total effective capacitance is going to depend upon this cross section area of the junction that is contact with the p plus region that is remain the effective junction area. And that is proportional to the W. So, what I can say is the junction capacitance is going to be proportional to W if you have larger W the junction capacitance will increase.

Now this is regarding the definition; this is how we define the capacitance the junction capacitance, the overlap capacitance and the capacitance arising from the channel charge between v gd and v gs. So, what is the significance of these capacitances in real circuit operation? This can be understood from the point of view of say small signal analysis. For example, if I take this diode and as I said I am injecting a current.

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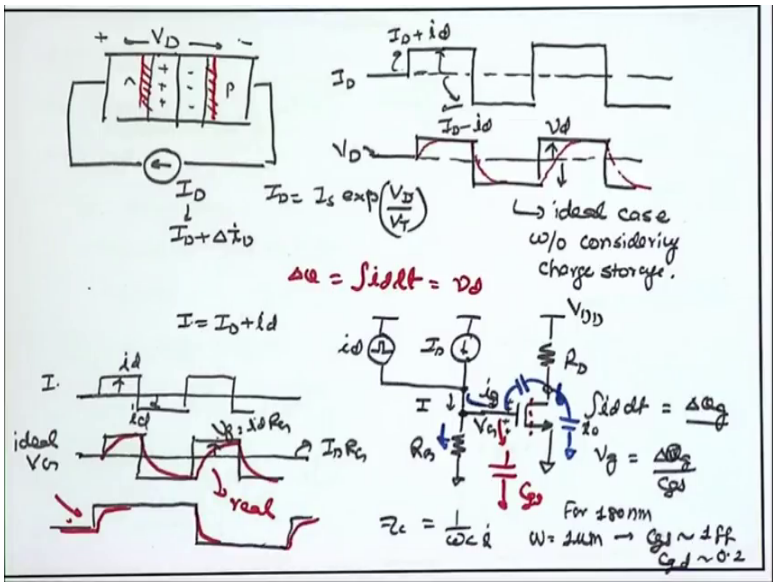

For example: suppose I having a DC current source across this diode. So, I am putting some DC bias call it I diode. And we know that there is a exponential relationship. So, I diode is equal to I saturation exp V D upon V T (Refer Time: 09:33). So, this is the exponential relationship approximately for the diode. So, that is going to develop some V D across the diode.

So, there is some V D across the diode; suppose it is reverse bias. So, V D is higher on the n side. Now if I want to say step up the current from I D to delta id; id plus delta id

this is a I am applying the small change in current. So, suppose my DC current is something like this I have I D to begin with I am stepping it up id plus small id, and then again stepping it down in the opposite direction making it I D minus delta id and I keep on doing this.

So, as compare to the DC I D I am increasing and decreasing the current injected in to the diode. So, if I do not consider the capacitive effect, I do not consider the charge storage effect across this device what is the behavior of V diode; that is the effective potential drop across the diode that we expect. If I do not consider this charge storage mechanism we expect that the movement you ramp up this current to id plus delta id the voltage across the diode will also go up according to this expression, because I D is increasing vds also increase.

So, ideal condition without considering the capacitance the V D should also go up and down as compare to the DC level; in reference to the DC level it just keep going down. This was the DC V D across the diode on the top of that we are imposing some small V D increase and decrease in the opposite direction commensurate with the increase and decrease in the current. That is the ideal case without considering charge storage.

But now if we consider the charge storage mechanism we know that in order to change the V D we will need to expand or reduce this charge stored. And that charge stored it is whenever you are trying to change this charge increase or decrease this charge that will happen only after a finite duration; after integration of this current. So, the additional charge that you are trying to get that is going to come because of the integration of the current. So, that is going to take some i d t charge.

So, if you are talking about delta id that will integrate over time and then only give you the additional charge delta Q small id dt. And that is going to result in an effective potential drop V D small signal drop across vd. So, this is not going to be instantaneous. So, as a result what we expect is that there is going to be some finite delay the actual ray form is going to have some finite delay in rising up and again its falling down it is not going to ideally just go up and down.

So, we see that whenever there is a charge storage mechanism present the signal change over here it is becoming sluggish is getting delayed, because you need to integrate that

change in current to accommodate or you know produce that additional charge which is present in the depletion region.

Same thing we can say for the junction capacitances in the MOSFET. Likewise another example that we can take is the gate of the MOSFET; suppose you are having ideal current source I D which were supplying to a resistance R G which is connected between the gate of the MOSFET and ground. You have a R D connected between the say V DD and the drain of the MOSFET and the source is once again say grounded. On the top of this if I impose another pulse current source just like this one and as a result I change the total current going in. So, the total current going in it will be I which is equal to I D which is the DC current source this is constant on, but on the top of that I am applying this small signal id going up down up down, so I have plus id.

So, ideally if I do not consider the capacitance of the MOSFET, if I do not consider the charge storage mechanism inside this MOSFET. So, the moment I D goes up the voltage also goes up. So, an total current I if I plot as compare to this I am putting it up and down by small id; ideal if I ignore charge storage mechanism the total gate voltage V G instantaneously will go up and down that is this voltage level is just I D times R G. So, the DC level is ig times R G and on the top of that if I am changing this current by small id it will go up and down instantaneously. And this level this difference we can call it small V G which is equal to I D times R G. If we will have this much jump every time you increase the I D by small id the gate voltage should increase instantaneously reduce instantaneously, if I do not consider the capacitive behavior or the charge storage mechanism of the MOSFET.

But ideally once again what is going to happen? In order to increase the voltage over here you are effectively changing the V GS and whenever you change the vgs this positive charges must be balanced by equal amount of additional negative charges in the channel. So, whenever you are trying to increase this gate voltage it must be compensated by equal increase of negative charges inside the channel so that the electric field is once again neutralized. So, the electrostatic will force the electrons over here to accumulate and balance the additional positive charge that you will trying to produce. For negative cycle of the I D you are trying to reduce the positive charge here that is you are trying to reduce the voltage over here; that means it is going to reduce the negative charge over here.

Once again this charge storage will not change instantaneously you need to provide, you need to integrate the current over here for a finite duration whatever is the small current going to the MOSFET I call it ig. So, whatever is the current going here to the gate of the MOSFET it will integrate id dt and that is going to provide over a time t naught it is going to provide delta Q that is the total additional charge that you are putting on the gate of the MOSFET delta Qg. And corresponding to that the change in the gate to source voltage can be written as delta Qg by cgs. So, delta vg will be just delta Q g upon cgs by definition that because cgs is defined as Qgs times vg. Or in other words cgs is equal to del vg upon del Qg.

Now that means, let once again rather than this voltage going instantaneously up and down it will take finite amount of time to raise and fall, if this is the real characteristic. So, once again because of this charge storage mechanism we are not able to change this voltage instantaneously, likewise we are not able to change this channel charge instantaneously. It will respond after a delay when we have been able to integrate the required amount of additional charge to produce the new V GS across the MOSFET; that is the between the gate and the source.

So, this is how we can understand the effect of parasitic capacitances. So, if not that we have a additional capacitances connected between the gate and source or gate and drain. It is originating because of the basic physics based operation of the MOSFET. The physics of the MOSFET is inherently producing this charge storage mechanism and in order to change the gate voltage, you need to change the total charge stored across this oxide what on the gate as well as in the channel, and for doing that you need to integrate this current for a finite amount of time to produce that delta Q and hence to produce the delta v.

And therefore, you are having a equivalent RSC effect. So, it is something like replacing this MOSFET by a equivalent capacitance over here. So, I can you know model this MOSFET by equivalent capacitance where the capacitance is defined as small signal cgs approximately for the timing ignoring the cgd. And it is accounting for the charge storage mechanism.

So, what we see from here without even going into circuit analysis doing small signal frequency response and all those we can conclude that whenever we have this kind of

charge storage mechanism present in the device it is going to slow down my operation rather than ideal high speed it is going to slow down my signal transition and affect the speed at which the circuit can perform. If the cgs is larger and larger this curve will be more and more sluggish. And therefore, the speed at which the circuit is operating will be more and more sluggish.

So, that is the basic effect that these parasitic capacitances produce, they are slowing down your circuit, they are slowing down the circuit response and as a result of which your overall circuit performance speed bandwidth is going to be suffer. Therefore, we call them parasitic capacitances. Their role or their importance becomes more significant at higher frequencies, because at lower frequency the time duration is much larger, the curve, if the period of the signal is much larger.

Then as compare to the period the signal will able to raise much quickly. So, we can ignore this finite raise and fall time. So, at lower frequency their effect is not that much visible, but as we go towards higher and higher frequency the signal may not be even able to follow; the gate charge may not be even able to follow the input current. As a result this may become more and more sluggish and the amplitude may reduce. So, the effect of these small parasitic capacitances arising from the charge storage mechanism becomes more and more prominent at higher frequency.

And therefore, the parasitic capacitances their role comes into picture for high frequency response and not so much for low frequency. For low frequency operation we can treat them almost absent, we say that they are acting like open circuits that can also be understood from the point of view of complex impedances on the capacitances. So, if you are having the complex impedance of the capacitances z c defined as one upon omega c you will include the phase factor I ought omega c for larger frequencies the impedance reduces, and therefore they can no longer be treated as short circuits we need to take into account their finite impedances.

At low frequencies one upon omega c becomes very large and therefore we can almost ignore them because their capacitance values are pretty small. It will be for 180 nanometer technology I would say if I look at 1 micro meter channel length the cgs will be of the order of few femtofarad cgd will be relatively smaller, as we see cgd just coming because of the overlap. So, cgd will be approximately a fraction of femtofarad

0.2-0.3 femtofarad. So, their effect becomes more and more prominent at higher frequency. Therefore, we include these parasitics for high frequency model of the MOSFET.

Let me add these capacitances that we just defined on the MOSFET model.

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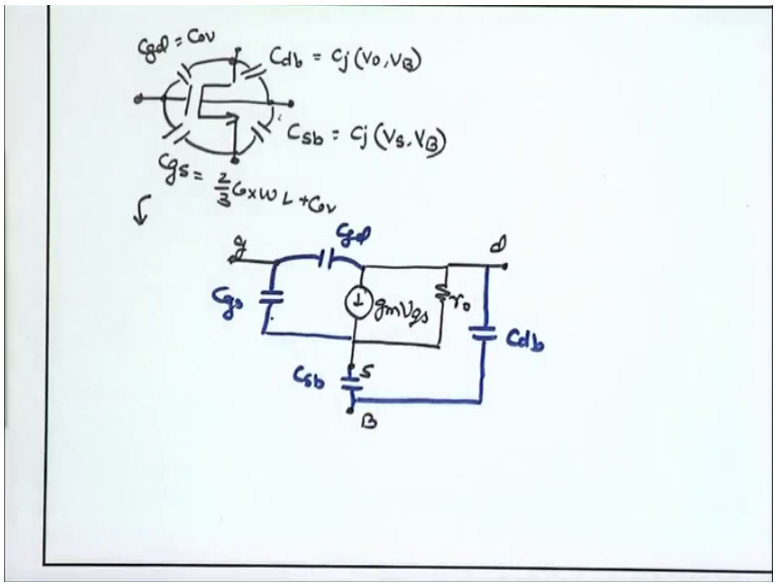

So, we define cgs, I will just call it cgs earlier term we used by c effective, but let us call as cgs this is just equal to 2 by 3 Cox W L plus C overlap in saturation region. We define cgd which is just equal to C overlap for saturation region. We define the junction capacitance which is coming between drain and the body, I can call it C db it is the junction capacitance c j, and it is the function of course of V D and V B because it is a diode across which we are measuring this capacitance which is appearing between drain and body. And likewise we have C sb which is again the junction capacitance dependent upon the V S and the V B.

In general for normal MOSFET operations NMOS substrate will be always preferably kept at ground potential or 0 potential, because we do not want to forward bias the diodes; if you increase the body potential the p n junction associated with the p substrate and n source p substrate on the drain junction can get forward bias. So, it is preferred that the substrate of the NMOS is kept at lowest potential that is at 0 voltage if 0 is the lowest potential available to you in I C. Source can be at higher potential than 0. In many

circuits we may see that the source are going to be settle higher potential than 0, drain is definitely higher than the source.

So, drain to body junction is always reverse bias, source to body junction can be either at equilibrium provided the in case the source is at 0 the source as well as body both are at 0, if source is at higher potential then this is also reverse bias. So, both this junction capacitances are coming because of the reverse biased diode associated with the drain and junction source and junction. And likewise we have the other capacitances between the gate and source gate and drain coming because of the channel charge modulation and the C overlap and cgd comes only because of the C overlap.

So this basically completes our high frequency model. So, if I replace this MOSFET model with the corresponding small signal model that we have just seen. So, start with the small signal model gm vgs ro and then we had this terminal drain and the gate and the source. This is the earlier model. The low frequency model that we started with now we need to connect these capacitances; I can define another terminal call it the body terminal over here and I can draw the capacitances between these two terminal. So, between the gate and the source between the gate and a drain I have cgd between the gate and the source is have cgs, between the source and the body I have csb, and between the drain and the body I may have cdb.

So, this is the high frequency model including the small signal parasitic capacitances arising from the code device physics of the MOSFET. And we are going to see how to analyze circuits in for high frequency regions where we need to take in to account these parasitic capacitances.

So, before I proceed let me stop here and see if there is any question; let me see. So, we have some questions collected. So cgd; as I said means that the one of the question is whether cgd is equal to C overlap. So, as we said in saturation region we do not have the control of drain voltage on the channel charge if I go back to my original earlier slide.

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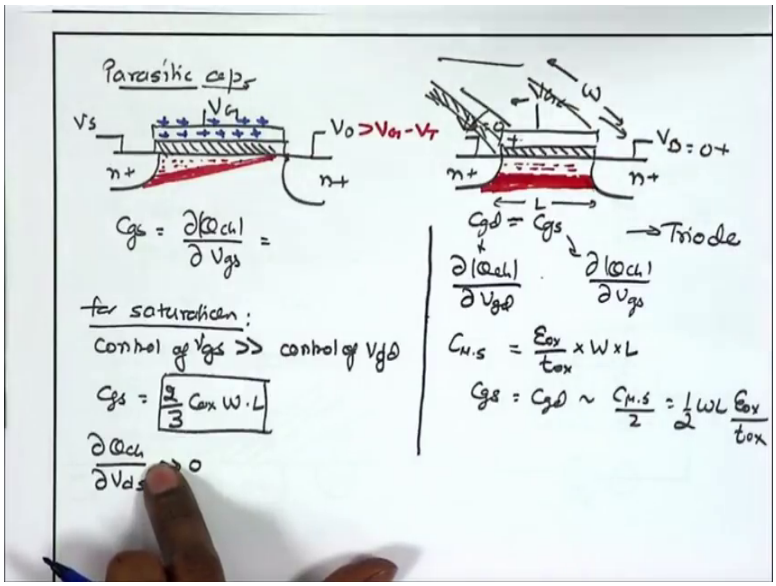

If the device in saturation the channel charge is pinched off on the drain side you do not have much channel charge if you increase the drain voltage little bit there will be some pushing of this channel towards the source, but that total change in channel charge will be very insignificant. Therefore, approximately we assume that the effect of V D on channel charge is almost negligible, therefore del Q channel by del vds or vdg is going to be almost negligible that component is negligible.

But, we do have the overlap capacitance which is always present that does not need the channel to be present; so that is what we discussed. So, we have a the overlap region; the charges on the gate are being balanced by negative charges in the n plus region. So, that is the required channel to be present channel can be completely depleted even if it is off you do have the effective C overlap present between the gate and the drain under all condition; likewise for the source. So, for saturation region because we do not have the cgd because of the channel charge the only capacitance between cgd that arises in the saturation region is the C overlap.

So, another question probably again requiring some more discussion on the topic of circuit response or speed response effect of parasitic capacitances on the speed response. Once again revisiting this particular example what we said is if you do not consider the charge storage mechanism; if you do not consider the capacitive behavior of the MOSFET I assume that there is no current flowing in to the gate.

Ideally MOSFET does not have any current flowing to the gate if we talk about DC current there is no current flowing to the gate of the MOSFET; DC current is 0. Therefore, there should not be any current here, whenever I increase the I D to id plus delta id that entire increase in the current should immediately go to R G. And therefore, the gate voltage should immediately go up from id R G to id plus small id times R G. So, we are expecting in instantaneous jump in the gate voltage because it is just control by R G we are not considering the capacitive behavior of the MOSFET.

But we know that in order to arrive at this larger v g which is higher by id R G because this voltage we are expecting that when we increase the current to id plus small id the gate voltage will increase by I D times R G. But in order to increase that much gate voltage I must also ensure equal amount if negative charges being produced in the channel so that this additional positive charge which is id R G times this effective capacitance that is balanced by the negative charge.

So, in order to allow this effective additional positive charge I must divert some of the current to the MOS gate. Initially some part of the current will be utilized in increasing the positive charge count on the gate. So, it is must said gate is stealing away some charge, that current is not passing through the oxide through the oxide there is no current, but the gate is accumulating that positive charge for some duration till the effective V GS across this MOSFET is equal to the final value, because this is the final value we expect right under for long duration if I apply this additional I D the final value should settle to id R G plus small id R G. But that additional voltage will mandate more positive charge on the gate and more negative charge in the channel. And that means, that initially when you are increasing the I D to id plus delta id; some amount of the current or some amount of the positive charge will be stolen by this gate to increase the positive charge count and hence increase the voltage, it will not happen instantaneously.

So, the current in R D will not jump instantaneously from I D to id plus delta id. First it will be diverted to the gate of the MOSFET store some more positive charge and then finally once it has the reached to the steady state value. Again the rest of the entire small id will start flowing from R G. Then the output the gate voltage settles to the final value.

So, that is because of the charge storage mechanism. Once again I can replace this MOSFET by a equivalent small signal capacitance cgs and say that when you are having

this cgs and then we are trying to increasing I D to id plus delta id there is going to be RC time constant associated with the charging of this capacitor. The voltage across this capacitor will not jump instantaneously, because for that you need infinite amount of current. You will take some finite amount of time to increase the voltage across this capacitor by integrating the small current flowing in to the capacitor for finite duration then only the voltage of the capacitor will gradually raise and reach the final value.

If the cgs is larger and larger if this effective capacitance between this point and ground is larger and larger you are going to take more and more time to integrate the current and we know calls the same voltage increase. So, here this form will going to be more sluggish, and as a result your circuit response is going to be slower because the you are trying to increase the gate voltage instantaneously by increasing the drain gate current. But this capacitance because of the charge storage mechanism is slowing down their behavior.

Same thing will happen on the drain side as well. So, here because you are trying to increase the drain voltage instantaneously by increasing the gate voltage, but we know that there is again effective charge storage mechanism between the drain and the gate, drain and the bulk. So, whenever you are trying to increase the drain voltage the effective potential across the drain and the gate, drain and the bulk also it will take certain time to settle to the final value because we have a charge storage mechanism associated with this.

So, you have some effective capacitance between the drain and the gate and also between drain and the bulk assuming that the bulk is grounded, you cannot charge change the voltage on this capacitor instantaneously it will take some finite amount of time for this additional gate voltage to produce the required additional current in the drain and then changes the voltage across this capacitor. It will have some RC time delay associated with the charging and discharging of this parasitic capacitor. And that produces sluggish response slow down the response of your circuit. That is the basic mechanism.

We can always do the mathematical analysis, we can always find out the complex impedance of the capacitance and do the network analysis by KCL KVL find out the frequency domain transfer function, but the basic mechanism how do the circuit is slow

down is because of the charge storage mechanism of this parasitic capacitances that is the origin.

Another question if a cgd is 0 charge concentration what happens to the charge concentration, conservation. So, cgd is not, so if cgd is 0 in that case you are just saying that the overlap length is 0. So, effectively if I assume that the overlap length is 0 we are not going to have any cgd, and therefore in this small signal model if I look at the capacitance coming between the drain and the gate that will be absent. So, that does not valid my charge conservation any manner only thing is you do not have a charge storage associated with the change in drain to gate voltage.

Student: Junction capacitance.

Now, the junction capacitance is not there; another question is whether there is any link between the cgd and the junction capacitance. So, ideally there is no link between the junction capacitances arising because of the completely different phenomena. So, the cgd is appearing because of the depletion region between the drain and the source, whereas the cgd is appearing because of the overlap capacitance in saturation region. So, cdb has no such direct link with cgd.

Another question regarding the dependency on junction capacitance on W. So we have already shown that ultimately the junction capacitance depends upon the area. So, if I look at this junction it is going to extent toward the W. So, this entire area of this junction this bottom place and this side wall is going to give you the junction capacitance, because the depletion region is surrounding this entire junction. So, is proportional to W and the junction depth. So, larger is a W larger is the junction capacitance.

So, now we have completed the high frequency model of the MOSFET. Next thing that we need to look into is the noise model, noise analysis associated with MOSFET. So, any more question before we proceed towards noise model? Now let me talk about the noise model although we have little time left before we leave for the break. So, I prefer if there is any other question before I go for the noise model; any other broad question.

So, gmb there is another question; a good question on gmb that we have not discussed which can also be important. We have skipped this in favour of time because we already had an short of time and gmb will require discussion of threshold voltage, how does a

threshold voltage depends upon the substrate to source potential and what is the dependency from there we can apply we can figure out the expression for g m.

So, given the time constrain it will be difficult to cover that because that requires consideration of threshold voltage, the origin of threshold voltage, physics behind it then we can derive the small signal parameter. The first thing is talking about the threshold voltage. And I am afraid we do not have enough time to go in to that detail. We can give you references, of course in certain cases gmb can be important and there are some interesting circuit schemes where gmb can be used for some interesting signal processing applications that that is too, but we are skipping that.

Hot electron: another question is on hot electron, so these are short channel effects. Those are more important I would say for digital circuits where the channel lengths are very short and you can have very large electric field within the short channel that can create hot electron effect. For analog circuits the starting point was that mostly we were going for relatively larger channel lengths, because we want larger ro, larger output impedance, stronger saturation region characteristics.

Therefore, hot electron effect may not play very important role unless your DC voltage at the drain is very high. There are certain reliability issue definitely if your DC voltage at the drain is sufficiently high you can have a hot electron effect, you can have some reliability issues, you can have NBTI PBTI which are related to somehow you know the electric field high electric fields created in the drain region or in the channel (Refer Time: 37:53) to the drain region.

But once again they are the hot electron effect is more of an reliability issue associated with some the short channel device; we may not focus too much on that and while considering the analog circuit design. Any other question? I guess we can start with the noise model in the next slot rather than starting it right now.

So, just a brief introduction about noise: so we have so far studied about the parasitic capacitances the high frequency model, the low frequencies, small signal mode, we have looked in to the physics of the devices how this capacitances are coming and how do we understand the effect of this capacitances on the device behavior and ultimately the circuit behavior.

Now, let us talk about the noise model how do we include the effect of noise, how does noise originate, what is the physical mechanism behind this. So, once again we may not be able to go into the detail of the device physics and its derivation, but at the higher level excepting certain formulations excepting certain well known facts we are just going to formulate the noise model which can be incorporated into the small signal model that we have developed so far and then see how they are going to be used.

Before we go towards the noise model of the MOSFET it is first of all important to understand how noise is represented in circuits. So, what is the concept of mean square noise or RMS noise, how are we going to add different noise sources of we have two different independent noise sources available how do you add them can we directly superimpose them or we did not to do something else what do we do to their power, noise power or mean square value.

Likewise, we also need to see what is meant by noise spectral density. So, one thing is the amplitude of noise or you know magnitude of the voltage or current fluctuation because of noise that may be produced in a device the other important characteristics is what is the frequency spectrum of noise; how it is it distributed in frequency if I have any signal I can take a frequency response and find out what is the frequency spectrum in at which frequency it is picking. That means, at that frequency the signal content is highest or in other words the signal is having that particular frequency content maximal.

So, likewise we also need to look into the frequency characteristics the spectrum of the noise sources. In general there are two main categories of noise sources which are encounter in device in terms of spectrum. One of them is white noise that the frequencies spectrum is white it is flat. That means, all frequencies starting from 0 to infinite they have almost equal magnitude of you know noise component.

Other dominant frequency spectrum that is encounter in devices which creates a lot of problems specially for low power low noise circuit design is one upon f noise whose spectrum is it increases with 1 upon f. At lower frequencies the noise becomes stripper and stripper higher and higher. And therefore, we are dealing with low signals we are trying to amplify a process low frequency signals coming from sensors biomedical sensors and in different kinds of sensors that low frequency noise becomes very critical

and it corrupts the signal. And therefore, we need to take certain special considerations to handle that low frequency noise at circuit level.

So, when we looking into this two noise sources the noise source with one upon f characteristics and noise source with white characteristics, and we will look into the origin of these two noise source in the device very briefly trying to formulate the expressions compact expression trying to make sense of that expression; not going to the derivation just trying to justify that expression. And then use that noise model in incorporate that noise model in our small signal analysis.

So, there are three thing we are going to do: first is definition of noise, representation of noise in time domain, addition of independent noise sources. Second thing is frequency domain representation of noise in form of noise spectral density. And the third thing is incorporating noise model in the MOSFET understanding the origin of noise in the MOSFET and including small signal parameters corresponding to the noise model in our model to complete the entire picture; low frequency, high frequency, and then the noise.

So, this recipe will help us in doing analysis for the circuits that we are going to encounter doing the DC analysis based on the DC equation doing the small signal analysis based on the small signal low frequency equations, looking at frequency response bandwidth of the circuits resulting from the parasitic capacitances, and finally talking about the noise analysis, because of the key noise sources in the transistor and also the resistors; resistors are another component which inherently have voltage or current equivalent current noise present in them. And that is related to the transport of electrons.

So, when you are having electrons being transported across the resistive channel it propagates in a zigzag fashion we have lot of carriers colliding with this crystal with lattice and it is not a straight lines, it is not like a bullet it follows a zigzag pattern, lot of collisions, lot of scattering takes place and over these scattering and collisions there is an effective thermal fluctuation effective thermal voltage created across the two terminals of that device.

So, without going in to details we can understand that this origin of the noise voltage in a resistor it is basically because of this random temperature dependent fluctuation of the electron trajectory or a carrier trajectory in that device. And as we can expect that if your

resistance is larger that means your collisions encountered by the carriers is stronger or they are having longer channel or path to travels resulting longer resistance we expect that is noise voltage is going to be larger, because that effective random fluctuation is going to be larger. Likewise if the temperature: the temperature of the device goes up when once again this random thermal motion is going to increase and as a result of which the effective noise voltage across the two terminals of the resistor is going to increase.

There are two things coming in to picture: the effective equivalent resistance value, larger is the resistance value more is the random nature or random fluctuation in the trajectory of this carrier leading to effective larger noise voltage. And then higher is the temperature larger is thermal fluctuation in the trajectory once again larger is the noise voltage.

So, we can say the effective noise voltage produced across a resistor of value r is proportional to two things: first is the r and second is the t. And the proportionality constant happens to be 4 k where k is the Boltzmann constant. So, the effective noise voltage across the resistor is 4 ktr. That is a starting point and that is without we have not gone into the frequency domain representation of the noise, but we will do that soon and we start again. So, this is the noise spectral density of the; noise voltage produced by a resistor of value r.

So let us continue from here, let us look in to these three points when we come back that is the representation of noise, manipulation, addition, subtraction of noise, representation of noise in MOSFET and its capturing it in the small signal model that we have discussed so far.

Thanks a lot.