Analog Circuits and Systems through SPICE Simulation
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Lecture - 37
Sampling

Welcome back, and let us review our discussion on the Sampling unit.

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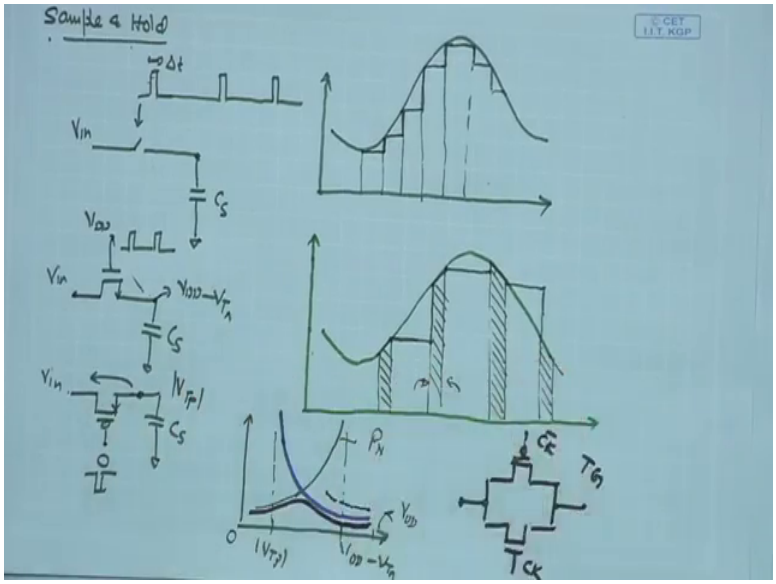

So, the simplest sample and whole unit can be seen as a switch in series with the capacitance we can call it the sampling capacitance C S and we have the switch signal which is turning on periodically at the rate determined by the micro-strain. And if I assume that this on duration is sufficiently small as compared to the overall sampling period we can assume that this switches getting on only for a very small duration.

And in that case whenever for this small delta t the switch gets on the C S will be sampling the input signal. And when the switch gets off immediately after this t on the capacitor should ideally keep that voltage stored, because there is no other path for the charge to get dissipated. So, that should be the ideal behaviour of such a system when this delta t or the t on approaches 0.

So, if this is my analogue data coming in at different instances if I am looking at the C S if I assume that these are the locations where this t on is coming which are very narrow

pulses my output will be constant after each t on and it will be changing only when the t on goes high and cross point that the switch gets on. So, this will be something like close to true sample and hold and so on.

So, these are the this is the output waveform the stair case waveform the pure gate going to get at the C S. Of course, in real time you will have and overall nonzero pulse rate and hence you may obtain a track an hold waveform whenever the switch is on. So, if I zoom out the waveform in the real scenario if I look at the sampling pulses they are going to be on for a finite duration and just zooming out the sampling pulses.

So, I am not maintaining the scale between these 2 assume that this is a different scale I am zooming out the sampling pulses. So, the sampling pulses on during this duration and therefore, when the switch is on during that duration the voltage at C S will be a faithful replica of the v in ideally and when the switch gets off it will stay constant again when the switch gets on it will again try to track the input signal. And once the switch gets off again it will stay constant. So, this is the waveform we can expect if we are looking at the track and hold scheme with my ideal switch. So, I have just assumed that I have just zoomed it out and the sampling frequency is still very large.

So, this is the duration in which the switch is on of course, if we want this entire sampling duration to be allocated to the digitization process we would like to reduce this as much as possible I would like to reduce the t on as much as possible. So, that a to d converter can utilize the maximum of this sampling duration in conversion of the analogue signal into the digital value. So, favourable to minimize it as much as possible and also let minimization could require certain design consideration with the switch what kind of a sizing what kind of transistor configuration we are choosing for this switch.

So, let us look at the implementation of this switch choosing transistors and the simplest configuration can be just employ a simple NMOS switch and you have the C S over here and you are driving this NMOS with a pulse and you have the v in over here we know that for the NMOS. However, the maximum input voltage that you can sample is going to be equal to VDD minus VT if the gate voltage the clock voltage is having amplitude of VDD because the moment input signal reaches VDD minus VT the VGS drops to below VT and as a result the current in the switch will drastically reduce and hence it will not able to follow the input signals fast enough, because of leakage current if visually with

for long time it may still be able to follow, but for sufficiently first sampling it will not be able to carry the input signal over here it was stop at VDD minus VT.

And likewise if you have a PMOS input or a PMOS transistor there also we know the overall behaviour if you are having the input signal over here as the input signal goes lower the PMOS will try to discharge this capacitor towards v in if the v in is going lower and the clock signal of course, that you need to keep the PMOS on is 0 when the driving signal is 0 or the pulse is 0 then it will be turning on.

And we know that in order to have sufficient current through the PMOS. So, that it can discharge this capacitor this voltage should be at least mod VT or mod VTP. Therefore, PMOS can conduct at the max till mod VTP V in equal to mod VTP likewise NMOS would fail if the input signal is going beyond VDD minus VT or you should call it VTN.

So, if I plot the resistances of this NMOS and the PMOS switch we have the curves if I mark this point as say VDD minus VTNM this one as mod VTP. So, how does the resistance of the NMOS switch look like? So, input as we have seen in our case can go all the way from 0 to VDD. So, the input can range from 0 all the way close to VDD. So, this is the point to VDD. And if I la talk about the NMOS resistance as the input voltage as the input voltage approaches VDD minus VTN the VGS reduces to 0.

As a result the resistance of the NMOS will be increasing very stickily it will be interring the sub-threshold regime as a result close to this point you have the NMOS resistance peaking likewise the same thing happens for the PMOS this is your r of n likewise if I talk about the PMOS we know that if the input signal is lower than mod VT this is 0 for keeping the PMOS on if this is 0 and input signal is lower than mod VT. Then, once again the VSG becomes too small. And the transistor in turns into sub-threshold and the current will be drastically reduced. And hence the resistance of the PMOS switch will be drastically reduced and hence resistance of the PMOS will be peaking when you the input signal is approaching mod VTP.

On the other hand if the signal is large then there is no problem with the PMOS it can easily charge the capacitor from height to us from for a higher signal likewise for the NMOS if the signal overhead is low that is also not a problem it can easily discharge, because v this is VDD and even the signal is low you have sufficient VGS. Remember if the signal is going low this becomes the source terminal for NMOS and it will be sinking

the current it will be trying to discharge the C S. And then that case the terminal over here becomes the source and in that case your sufficiently large VGS for smaller v in therefore, the resistance of the NMOS if I say keeps dropping for a smaller V in.

Now, if I the for a good switch I would like to have a overall resistance which is constant and it makes sense. Therefore, to combine these 2 if I combine both NMOS and PMOS then the overall resistance will be a parallel combination of these 2 given by the lower of the 2 and therefore, if I combine these 2 I have an overall resistance of the trans of the resulting switch given by the superposition of these 2 resistances. So sorry, so you have the overall resistance being the superposition of these 2 switches and the value will be lower than the lowest.

And as a result you are going to get a curve something like this which is relatively constant over a wide range from 0 to VDD. And therefore, we have combined switch which can be termed at the transmission gate a combination of NMOS and PMOS where you can have a clock signal going to the gate of NMOS which will turn it on and at the same time you have the clock bar going to the gate of PMOS, because when the NMOS is turning on you also need to turn on the PMOS simultaneously. And therefore, you need the inversion of the clock signal as a clock bar de demarcated over here.

So, in this case you can have an overall resistance across the switch which is remaining relatively flat across the entire input range and it can follow or it can sample input signal starting from all the way from 0 or going all the way to VDD. So, this can be term as a transmission gate which is very effective in sampling operations or analogue circuits where we have constant sampling of analogue data.

Now, we will we need to look into the design consideration that we just discussed we saw that in order to maximize the digitization duration. So, that the ADC can exploit maximum of the sampling time I would like to make this duration narrow and that would imply certain constraint on the choice of the C S the sampling capacitor and also the switch.

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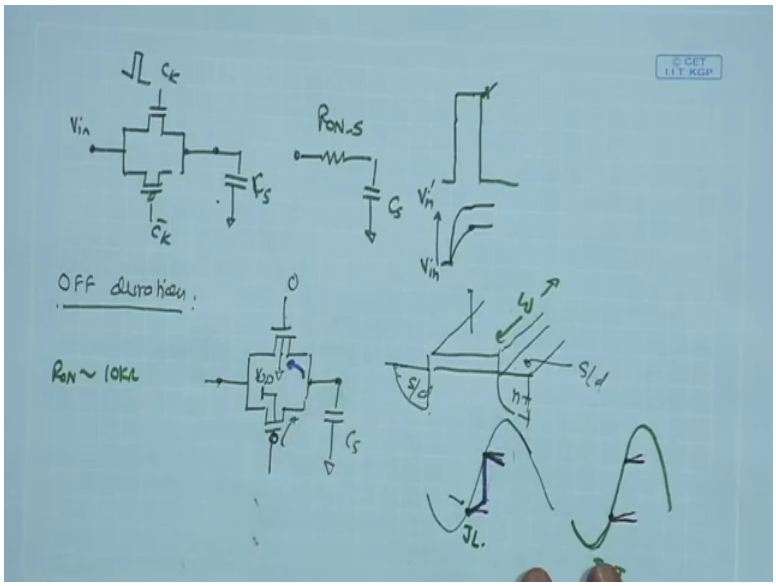

So, let us look at that. So, if I talked about the sampling circuitry consisting of the transmission gate which is sampling the input signal v in onto the C S we know that the overall on duration must be smaller than the r c time constant provided by the switch ultimately as we have seen the switch is going to have some finite on resistance given by the parallel combination of the r on n and r on p.

And as a result under on condition this can be represented as r on of the switch and you have the C S. And therefore, the time constant provided by this one upon r on times C S the corresponding time constant r c should be significantly smaller than the duration. Therefore, when we are trying to reduce the on duration by making the drive pulse narrower we would like to make sure that the on resistance times the C S is giving us the time duration which is sufficiently smaller than the clock pulse.

So, that the signal over here is faithfully able to charge otherwise you know that if you are having an r c time constant which is much larger than the input clock what can be the result. So, you will be having a very narrow pulse within which you are trying to sample the input signal and suppose the input signal is going high the output signal will not be able to follow the step.

So, it may stop and at an intermediate point the expected value ideally would have been a much larger value depending upon the jump between the v in the previous and the current samples of v in, but the switch being large resistance it will not be able to follow

it will have a larger r c time constant. As a result the final value that you are sampling will end up being smaller than the actual value.

So, we do not want that we would like to have the r c time constant of the switch smaller than the on duration. So, now, what is the pros and cons of doing that we can look at the overall C S as well one option is that we can go for a smaller C S that may also allow us to reduce the dimension of these 2 switches and therefore, both we have the independent to choose both the C S as well as the w of the switches but.

Now, we have to look at the overall operation in the off duration also what happens in the off duration when a switch is off and under that duration what is the role played by C S and the transistors. So, the ideal functionality is that during the on duration the input signal should be faithfully replicated on the C S as fast as possible within that on duration and when the switch is getting off the signal stored over here should be remaining stable it should not change significantly.

And we need to see what is the effect of the non-idealities of the switch on this expected behaviour to do that we can we can first of all look at the off duration. For example, what is going to happen if the switch is getting off and what is the behaviour expected for the signal stored on the c s. So, when the switch is off we have the NMOS gate voltage 0 and PMOS gate voltage VDD. Remember that source and drain definition of NMOS and PMOS of course, are interchangeable depending upon the polarity or the sign of V 1 minus V 2. So, I am not drawing the arrows.

Now, when the when these 2 switches are off we do have the leakage currents flowing in these MOSFETs these are not ideal switches even when the MOSFET is off it does have some leakage contribution and depending upon the technology depending on the dimension of the switches the technology node the dominant leakage component can be different. So, in the MOSFET we have several components of leakage surface several ways in which the leakage current can exist we have sub-threshold leakage we have junction leakage we have gate leakage current

So, you have to see which one is dominant we talk about say 180 nanometer CMOs technology which we are using our simulations there the sub-threshold leakage will still be relatively small gate to sub-threshold leakages yet smaller. However, the reverse bias junction leakage can be this significant and that is something which also increases

proportionally with the w of the transistor. So, sub sub-threshold leakage for example, can be reduced if we are having longer channel length that imparts the relatively longer channel behaviour to the MOSFET and that can reduce a sub-threshold leakage current, but if we are looking at the junction leakage; for example the junction leakage happens, because of the reverse biased diode if you are looking at the cross section of the MOSFET and you are having the gate terminal over here say for the NMOS you have n plus drain terminal.

So, I am just drawing the cross section this is the gate terminal this is the say source or drain and another source or drain now we know that in the reverse biased configuration of the diode there can be significant increase in the leakage current across the diode and here if you look at the conditions suppose when the signal is when the signal is towards the suppose when the signal is going up. So, we are having both the transitions in the signal. So, you have the up going slope and the down going slope of the input signal.

So, you may be sampling the signal at this particular point and after that the switch is getting closed and you are expecting that is signal over here will remain constant at this point and under that condition if I look at the situation at the NMOS gate you have overall gate voltage of the NMOS which is 0 you have the substrate generally which is connected to ground and you have the in the signal which is sampled over here which is sufficiently low suppose the signal over here is sufficiently low.

So, in that case of course, the reverse bias for the drain or source to bulk junction for the NMOS will be relatively low whereas, if you look at the PMOS. So, PMOS substrate it will be connected to VDD. It will be having the PMOS substrate in general connected to the VDD and the signal is low here we have for the PMOS which is having a p plus junction over here which is relatively low which is equal to the sample value over here, whereas the substrate junction is VDD.

Therefore, the reverse bias across the p plus n junction for the NMOS is going to be stronger in this case what do we expect from there you will have significant reverse bias current flowing from the substrate towards the source drain terminal of the PMOS over here as a result this can lead to increase in the overall sampled voltage.

So, what we expect here is that you will you are going to get a slight increase in the sample voltage rather than being constant it will show some increase. And then next time

when you are putting the switch on again it will go towards the new value again depending upon the condition the switches over here it can show increase or decrease. So, when the input signal is low or the sample value over here is pretty is small close to ground then the reverse bias current of oh sorry reverse bias junction leakage of the PMOS is going to dominate and it is going to increase the sample voltage little bit. Let us see what happens when the condition is reversed when that input signal sampled over here is high. So, suppose you are going towards the upper side.

So, this is a high value under that condition as we said the body terminal of the MOSFET is 0 and the body terminal of the NMOSFET is 0, whereas the sample signal is high and that case the n plus n plus drain n plus drain of the NMOS is having a potential which is sufficiently high, whereas the body terminal which is p is low is ground under that condition the n plus p junction of the NMOS is going to have strong reverse bias.

Therefore, the reverse bias junction current of the n plus p diode in the NMOS is going to dominate and therefore, it is going to cause dissipation of the charges store on the C S right. And that would imply that as compared to the sample value we would expect that ideally this sample value should once again remain flat, but rather than remaining flat it will go down little bit right and that will be determined by the leakage current how low it droops the leakage current junction leakage current is fast larger the droop will be smaller.

So, this is the dark curve over here shows the actual waveforms will be getting when you are going towards higher signal level the sampled voltage can droop and divagate from the actual signal whereas, when you are going towards a lower signal level the sample signal stored in the capacitor can show a little bit of increase this is true when your junction leakage is a dominant component. So, this is if you have sub-threshold leakage becoming dominant then the picture can be a little different.

Your sub-threshold leakage happens between source and drain. And in that cases become beneficial because the signal will be able to follow the C S will be able to followed the signal over here. And in that case if the signal is going up little bit the signal the data value over here it will be just trying to follow it, because of sub-threshold conduction is happening in this way and likewise the signal is going down the data over here will be also going down along with the signal.

So, if you are looking as scale technology node say 45 nano meter or lower there the sub-threshold can be sub-threshold conduction can be dominant there also of course, the signal over here will change as compared to the sample value, but at least it will be trying to follow the direction of the signal at this point. So, in this case if I say that this is for the junction leakage the junction leakage being dominant if I take another example where the sub-threshold leakage becomes more dominant there if this is the sample value at a particular incidence.

And we want this to be remain constant rather than remaining constant will increase little bit, because the input signal is increasing and likewise if I talk about the other half if I am sampling that it over here also we will have the same polarity, because the input signal the next sample it is increasing therefore, it will slightly increase and if I going to towards the down going slope it will just have the opposite effect.

So, this is the case for sub-threshold conduction when the sub-threshold conduction becomes dominant this is the case junction leakage becomes dominant. So, the technology we are using right now there is notice that the junction leakage is going to be the dominant component. And what does this junction leakage depend upon we can see that the junction leakage will depend upon the cross section area of the junction and what does the cross junction area the junction depend upon which transistor dimension is going to be the w.

So, if you increase the w of the switch irrespective of the l if you increase the w of the switch the junction leakage component will increase resulting in more and more dissipation of the charge into the substrate from the PMOS or at the NMOS. Therefore, these loops will increase and the divagation of the sample signals from the sample data at the closing point it will also increase which can be highly undesirable.

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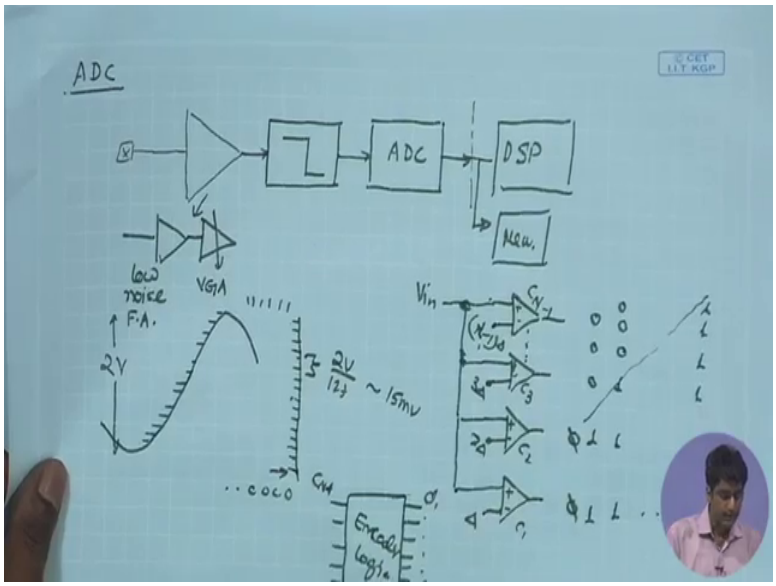

So, if I revisit my resolution requirement if I am dividing my entire signal range that is around 2 volt peak to peak range into 15 millivolts intervals I would not like the sample data to deviate by magnitude closer to 15 millivolt. That means, if the data droop or the analogue droop or increase in the sample value is high close to 15 millivolts we are using we are losing 1 LSB of the precision.

And one we are going to get a data which is wrong by one interval that is not desirable we are going to lose one l s b of information. So, that we should make sure that this droop or increase that is happening because of the leakage component is lower than that 15 millivolt interval in this case and these are the 2 things which is going to determine the choice of C S for example, what is the sampling capacitor dimension.

So, if I choose C S to be too small even if you have minimum size transistors it will lead to larger and larger droop if this. So, in our case for example, we are looking at relatively lower frequency sampling frequency is low. And if I talk about the on resistance of even minimum size transistor in 180 nanometers CMOs technology it will be not more than 10 kilo ohm.

So, if you even if you look at minimum size transistor when it is fully on either NMOS of PMOS there are values are close to 10th kilo ohm in 180 nanometer. So, r on we expect around 10 kilo ohm even if we are in 180 nanometer few tens of kilo met max. So, the triode region resistor of the on switches will be in this order even if it is minimum

size and then we are having the on duration the overall duration for which the data is supposed to be held is equal to the entire sampling duration almost.

So, if you are trying to reduce this on duration as we said if we look back to our sampling discussion if I am trying to squeeze this further. That means, for almost the entire sampling duration or the sampling period this capacitor is supposed to hold the data.

So, in our case the sampling period will be determined by the signal frequency content and if you recall our signal frequency content for the for the nueral potential that we have discussed this maximum frequency contained maybe a few hundreds of hertz at the max say kilohertz and as a result we would expect that the sampling frequency is say few kilohertz at max.

So, suppose the signal content the maximum signal content is say one kilohertz and corresponding to that the sampling frequency that you are getting is 2 kilohertz.

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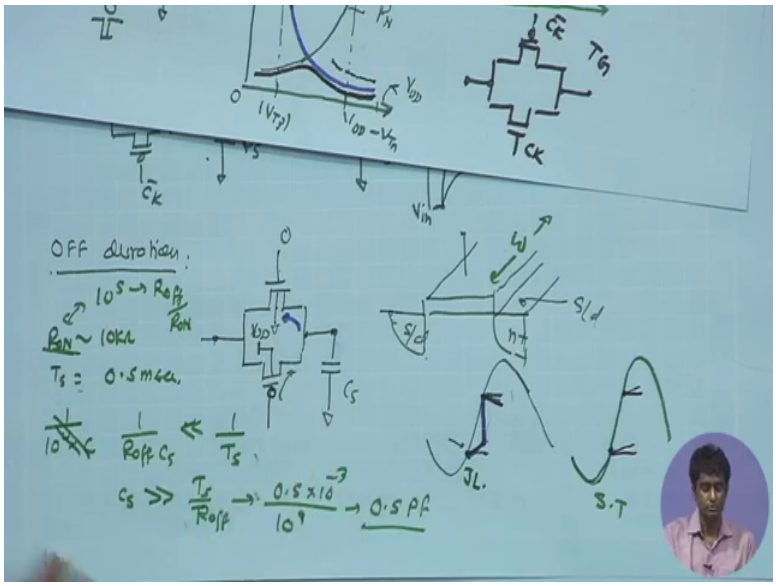

So, that t s is going to be 0.5 millisecond and then we are trying to make sure that one upon times the c that we are having that is the time constant provided by this is small this is this is on duration. Now this is going to determine the charging rate. So, for the of course, this charging rate if I look at I was talking about the leakage component what is the leakage current over here. So, I am mistakenly to good to get the on one for if I took

out talk about the leakage component of course, I will talk about the off resistance and for that I have to look at the leakage resistance sub-threshold resistance of this MOSFET and that depends upon the r on r off ratio that technology.

So, r on is 10 to the power of 4 and r off for the minimum size transistor that is going to depend upon the r on r of ratio provided by that technology and then r off if I estimate for a given technology I have to look at the r on r off ratio and for 180 nanometer I can have an r on of r off ratio of around 10 to the power of 5. That means, corresponding to this I can estimate what is going to be my r off for the minimum size transistor it can easily be of the order of 10 to power of. So, I have the overall r off this is the r off r on ratio. So, for a given technology we have an given r off r on ratio and that degrades as we go down the technology node.

So, for 180 nanometer 10 to the power of 5 or even better can be feasible for lower technology 45 nanometer it can go down all the rate to 10 to the power of 4. So, if the r on is 10 to the power of 4 r off can be 10 to the power of 9. And hence I must make sure that that r off that is the r off times the C S that is the discharge time that is the corresponding time constant that is much larger or in other words this is much smaller than the sampling duration t s that is the condition. We must make sure we are having. So, here if you look at the values I would get C S much be significantly larger than t s upon r off. And if I just put these number t s we have 0.5 millisecond and I have an r off which is maybe 10 to the power of 9.

So, this gives us something like a picofarad. So, I have C S things should be sufficiently larger than 0.5 picofarads. So, if I am choosing a c if I am choosing a C S of say few picofarad I should be safe with respect to the leakage. So, these are just numbers taken from a given technology that we are using your simulations. And the from that we can predict that what is the required value of capacitor and if you are going for minimum size transistor and then we can see the whether this minimum size transistor is also satisfying our required criteria for the on duration. So, in the on duration we have just discussed that the r c time constant provided by these switches should be lower than the overall on duration and as a result we must make sure that this on resistor in the period getting is satisfying that condition also.

So, if it is doing that then we are going to choose the minimum size transistor as it is for our design if not then again we have to trade off between these 2 we may have to increase the w by l over here, but at the same time we may have to choose a larger capacitance. So, that within the off duration it was not discharge. So, that trade off there while looking at the sizing of these transistors in the capacitor for the sampling. And we will also look into some of the non-idealities that if you are trying to reduce the r on by choosing larger transistor sizes what are the other issues or non-idealities associated with the switching of these transistor that can come into picture.

So, let us stop here for a short break, and see whether there is any question.