Analog Circuits and Systems through SPICE Simulation
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Lecture - 35
Transistor Level Design Of VGA (Contd.)

Welcome back and let us try to complete our discussion on sizing for the second amplifier the variable gain amplifier for our front end.

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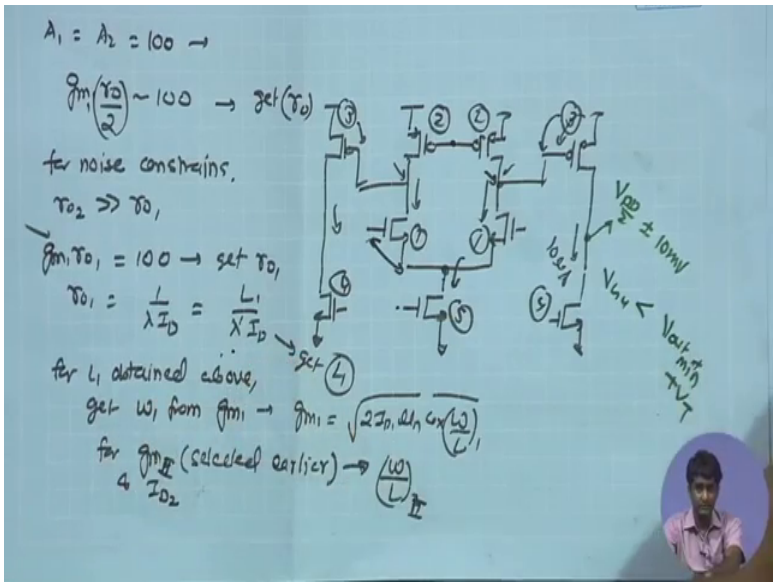

So, once again I had the same op amp circuit over here and we tried to distinguish the high level specification and for the time being I have taken some simplified assumptions just to focus on some of the mo more crucial points. So, I have assumed that the load capacitance over here is similar even if it is different than only difference it will make in the constraint over here this will determine a different value of gm 1 gm 2 based on the gain bandwidth product.

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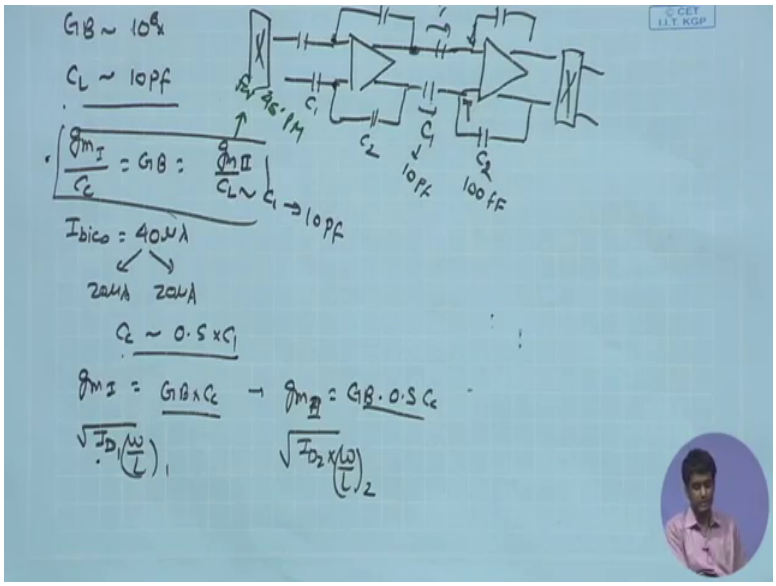

So, that is not a crucial factor, let us assume that the load capacitance faced by the second stage is also similar and that means, I am going to have again the same gain bandwidth product requirement for the second stage and that is going to have similar value of the C L and C c and likewise the gm 1 and gm 2.

So, since I will giving C L to be similar the C c also comes as similar and following the area constrained I will try to have C c half of C L and then based on that I need the values of gm 1 and gm 2. So, that calculated I have the gm 1 gm 2 and also I have the current budgets available total current budget I said that ok. Let us reduce the current in the second amplifier rather than going to forty microampere total current I can go down to set in microampere because my noise requirement is not so critical I can afford to have relatively higher thermal noise as well as 1 upon f noise corner.

So, I assuming those things I can reduce the I D 2 and I D 1 let us keep them 2.5 2.5 total current budget around 10 micro ampere for the overall second stage amplifier and then as a result of course, I will have to decide what is the ratio of this bifurcation what should be the I D 1 in the first stage what is the I D 2 in the second stage. And there also it will lead to the corresponding ratio of W by L 1 and 2, in the first amplifier design I did not considered the ratio of this W by L 1 and 2 so important I just allocated same bias current in the both the stages as that would mean that the W by L 1 and W by L 2 ratios are also going to be similar determined by this gm ratio. So, it because the gm of one of them is

half the gm of the other the W by L ratios will be correspondingly 4 times. So, that was the deciding factor over here.

Now we know that for the second stage amplifier one of the very important constraint will be the output swing because if you look at the number that we are using input signals say 100 micro volt the overall gain 10 to power of 4, overall closed loop gain of the first stage 100 second stage 100, 10 to power of 4 overall. The final stage over here the signal over here that we are getting that can be having a overall signal swing of 1 volt peak to peak right 100 micro time to the power of 4.

So, I can expect even up to 1 volt peak to peak signal worst case and I have to make my output stage such that it is capable to capable of handling such a large signal swing and to do that I have to look at the sizing of these 2 transistors carefully for the given current budget. Now in order to look at the sizing if I want a better swing over here I would like to have a smaller be overdrive for this remember what is the maximum and minimum voltage that you can have at the output V DD minus V overdrive of this PMOS is the maximum and the minimum side just V overdrive of this NMOS. So, in order to get better swing all I need to do is minimize the V overdrive of the PMOS.

And V overdrive of the NMOS for the output stage how do you minimize the V overdrive. So, V overdrive as I remember it depends upon the I D and W by L because I D is equal to W by mu and Steve has W by L times V overdrive square. So, V overdrive is equal to root under I D upon W by L.

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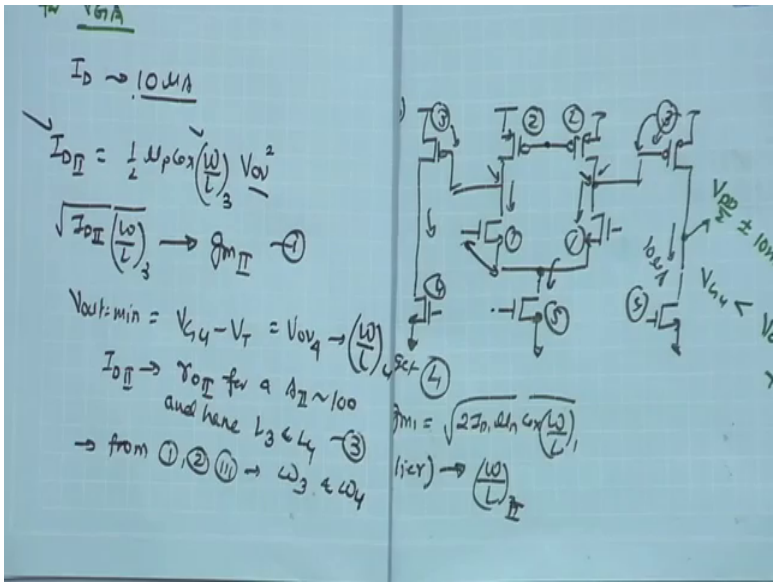

So, I can write it down for the output device keeping the amplifier circuit same side by side let us look at the V overdrive of M 3 and M 4 both of them I can write down I D of the second stage is equal to 1 upon 2 mu p Cox W by L I am call this M 3 because it is just a marked it as M 3 is W by L 3 times V overdrive square which is V G, V SG minus mod V t of this I want to minimize this and therefore I have 2 options either I reduce this or I reduce or I increase this or I can take the combination of both.

So, since the requirement is to get a certain gm I need the product of root under I D W by L 3 to be having a certain values. So, I need root under I D 2 which is the total bias current in the second stage I D 2 times W by L 3 that is determined by the gm 3 that I already or the gm 2 that I already have. So, that gm 2 is already determined from the gain bandwidth product requirement. So, this number I have this. So, this product must be maintained. So, if I am trying to reduce my V overdrive to get a better swing either I reduce the I D 2 and increase this that will help me in maintaining the ratio.

And therefore, I can you know go for half the current I can reduce the current in I D 2 to 1.2 rather than 2.5 and correspondingly increase the W by L 3 and that will keep the ratio of gm to same. So, I have similar ratio only thing is I have been able to reduce the V overdrive that strategy can be used to have a better signal swing on the upper side. So, I can trade off the bias current over here.

Now if I look at the lower side once again similar concern is going to come because we know that V out min is going to be equal to V G 4 minus V t and therefore, basically V overdrive and once again in order to reduce V overdrive 4 I would like to make the W by L 4 larger once you have the I D determinant. So, suppose I red reduce I D of the second stage to a smaller value maybe 1.25 microampere for that I can determine; what is the required W by L of M 4 to get a certain overdrive. So, this is going to determine my W by L required for M 4.

Now the I D 2 is known. So, this is going to give me the required value of ro to get the gm 2 and hence the value of L of the PMOS and NMOS. So, I D 2 is going to give me the ro 2 required for the overall gain in this stage and if I assume that the gain is still equally divided which is not necessary I can sacrifice the gain also over here a little bit because I am trying to reduce the bias current or in other words I can try to increase the gain over here a little bit. So, that it supports the reduction and bias current, but assuming that we are keeping the gain division almost similar. So, once again I can have a overall hundred gain in the second stage and that is going to give me the ro value for the given gm 2 value for a A 2 equal to 100.

So, for a given A 2 I can once again find out the ro 2 and hence L 3 and L 4 ultimately L 3 and L 4 determine the ro 2 for the given chosen current and that is going to give me L 3 and L 4 and W by L 3 and W by L 4 I have already determined. So, I can from there up to in the W of L 3 and L 4 from the earlier quantities we can obtain the W 3 and W 4. So, here we looked at the sizing of W 3 and W 4 and we notice that here the output string is becoming a major constraint and based on this particular constraint we are looking at other related issues that based on the output swing you first determine the W by L ratio.

So, that you are able to maximize the output swing based on that only we are trying to minimize the current over here reduce the current in this branch as compared to the differential pair, so that my overall swing over here is maximized. So, I took 2 steps I reduced the I D 2 that is the total bias current in the second stage I also tried to increase the W by L 3 to have the similar gm in the output stage. So, that those 2 things you have maintained.

And then of course, the L I said can be determined based on the ro requirement because I have the gain requirement A 2 based on that I can get the ro 2 and hence L 2 and then

therefore, W by L of these 2 can be determine. Now also we have to see the sizing constraint how it has changed for these 2 devices for the input devices we have already seen there the constrain is similar you have the W by L determining the gm 1 and hence the gain of the input stage because now we have relatively larger bias current available over here.

If we want to use the same bias current total bias current are located. So, I have reduced the bias current here. Therefore, I can use a slightly larger fraction of bias current rather than 2.5 I can use 3 or 3.5 microampere current here total and based on that I need to look at the W by L ratio of this 1 and also the L ratio the L value different divider noise the ro. So, here the gm determines the W by L and the ro determines the l. So, these are the constraint remains similar, but for this device once again the constraint is going to be slightly different here the L 2 is not an important constraint because 1 upon f noise corner thermal noise frequency is not going to be an important constraint.

Therefore we would like to rely on M 2 to facilitate better output swing over here remember first of all we have increased this W by L. So, that the V SG required for this device is going to be smaller and therefore, we are expecting that DC point over here will be larger and in the DC point over here is supposed to be larger remember we need to have a smaller V overdrive for this MOSFET, because if the DC point over here is supposed to be larger in order to facilitate more output swing at the final stage I need to have, larger DC bias point over here a larger DC point here means a higher maximum V out because maximum V out over here is vg plus mod V t. So, a larger DC potential here means higher maximum swing over here.

And a larger DC potential over here higher DC potential over here means smaller V SD or a smaller V overdrive and a smaller V overdrive would imply a larger W by L. So, I would like to have a larger W by L of this device. So, the constraint on W by L becomes more important I would like to have sufficiently large W by L for this device in order to ensure a smaller V overdrive. Remember in the common mode figure that we have studied how did we bias this was bias with the help of if you are going for a separate loop there it is biased with the help of a common mode feedback amplifier with reference equal to the V G of this MOSFET or V G of this MOSFET and in this case since we are expecting a larger DC potential over here we would like to have the V G over here also higher. And that would require a larger W by L. So, that is the differences with respect to

the earlier case some of the constraint getting relaxed and some other constraints coming in to determine the overall sizing.

So, and likewise we have the similar constrain for the M five here once again input swing is still not an important constraint because this 2 point are still DC bias points you are having, this points close to V DD by 2. So, you do not have much signal at this point therefore, the M 5 sizing constraint remains similar there is not much change. Output over here if you look at what is the swing at this point once again output swing over here close to 1 volt 1 divided by 100. So, we have at the max at 10 millivolts swing here.

Therefore, once again here also swing is not going to be very critical output swing at this node is once again is still not critical. So, we should just be careful about what constrain or what parameter is critical and what is not and based on that we can determine how to size and while you know getting advantage in terms of saving some bias current while not missing a bit any other specifications. So, these are the I have just presented some logical steps to facilitate sizing of the fronted amplifier and the second stage variable gain amplifier.

So, this is another issue that we have is the common mode feedback amplifier there we have already studied that for the common mode feedback amplifier if we are going for a single loop and we are not we are using the diode connected load for the error amplifier there of course, the gain requirement is not so critical. And therefore, the W by L and bias current all can be relatively lower sizing constraint can be relatively lower and also the error amplifier output comes over here as a common mode and whatever noise output is coming from the error amplifier that is also appearing in common mode. So, the noise consideration for the fully differential operation will still be relatively constrained for the common mode feedback amplifier.

Therefore even for the fronted amplifier when we are discussing the sizing of the common mode feedback amplifier the noise constraint will be relatively relaxed. We may not really worried a lot about the common mode feedback amplifier because just like the current source contributes in a common mode fashion, likewise a common mode amplified noise over here will also contribute in a similar fashion. And if we look at the input if you look at the common mode feedback for the joint loop like we are having single loop and sorry if you look at the common mode of the individual loops where you

are requiring larger gain for the common mode feedback amplifier there of course, you are using current mirror load for that and we are assuming gm ro gained from the common mode feedback amplifier.

They are some of the constraint related to the common mode feedback can be the input swing is what is the input swing that the common mode amplifier can handle.

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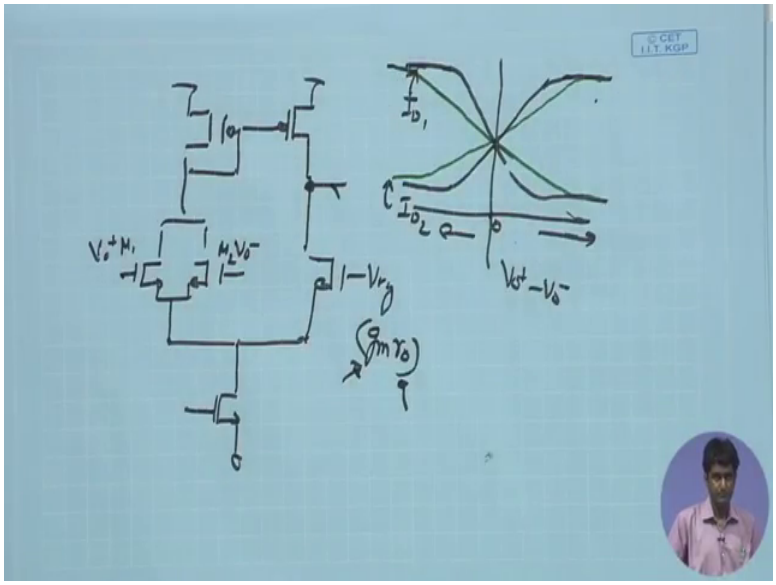

So, one of the important point that we are discussed in the simulations also is related to the input device dimension the gm of the input device. So, if you are using say in dual loop common mode feedback where we are relying on the diode connected load and this is your V o plus and V o minus coming and this is your V ref one of the important constraint would be of course, the gain we would like to have sufficient loop gain.

So, gm ro products should be sufficient and also we need to have a sufficiently large ro over here. So, that a compensation does work remember. For the common mode feedback the compensation point is this one we are creating a dominant pole over here because we add the capacitance between the output of the common mode feedback and output of the differential pair. So, this node gets compensated.

Now the other point is the values of the devices over here the W by L sizes over here and that is going to determine this overall gm ro product of this particular stage and whether we can rely on a larger ro or larger gm. Once again larger ro it will be favorable because

larger gm for input devices can negatively affect the maximum swing that these input devices can handle. So, if you rely on larger gm; that means, the overall signal swing that the input transistors over here can handle that will be relatively lower.

If you look at the differential pair response and look at the current I D 1 and I D 2 in the 2 devices say M 1 and M 2 as a function of say V o plus V o plus minus V o minus suppose to 0 and this side we have positive V o plus minus V o minus and of course, as a result I D 1 will be going higher on this side and as you make the V o plus V o minus negative the I D 2 will be increasing and I D 1 will be decreasing. So, this is your I D 1 curve and this is your I D 2 curve and smaller. So, this slope in this particular region this transition region is determined by the small signal transconductance of these 2 parameters which is also related to the transconductance here.

So, in order to get proper common mode feedback extraction we would like to have the gm 1 plus gm 2 equal to gm of this and therefore, if you want this error amplifier to handle a larger common mode we would like to make this slope relatively poor and hence that would imply that we should have a poorer gm of these devices. So, that will ensure that it is able to handle a larger V o plus V o minus, especially if your output signal is becoming large peak to peak signal is 1 board and you want this to be handle to able to be able to handle that large signal we would like to go for larger input handling capacity and that can be achieved by significantly reducing the gm that can be achieved in 2 ways either you reduce the W by L or you reduce the bias current.

So, if you reduce the bias current ro automatically will be increased and hence the gain can still be sufficiently large and remember that the gm ro product increased by root under k if you are reducing the bias current by k the gm ro products root under increases by root under k. So, that will still increase the gain. However, it will suppress the gm and hence it will try to increase the swing that this input device can handle. So, that is another important feature that people should consider while looking at the sizing of the common mode device.

And also another point will be to size this tail current source if you would make that tail current source sufficiently large it will be able to handle lower input signal over here and that also increases the maximum swing the referential swing that the out that the common mode device can handle that is another way. And we can have other alternatives

also in cases where the output signal spring is sufficiently large and extraction of common mode using this scheme is failing we can go for other schemes where you can have you can handle a larger output signal and where it is not constrained by such a differential swing.

So, we can take 2 minutes break after that we will resume the discussion.