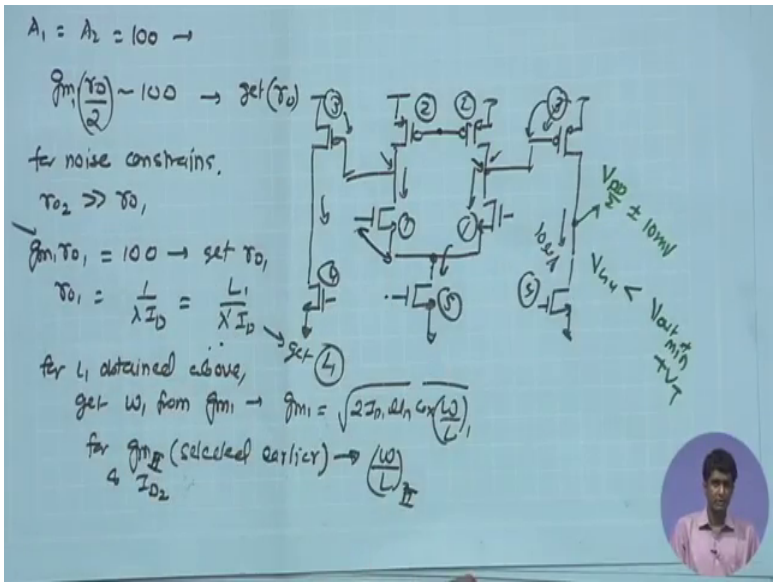
Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture - 34
Transistor Level Design of VGA

Welcome back. Let us resume our discussion on the transistor sizing, we were discussing in the last module.

(Refer Slide Time: 00:23)



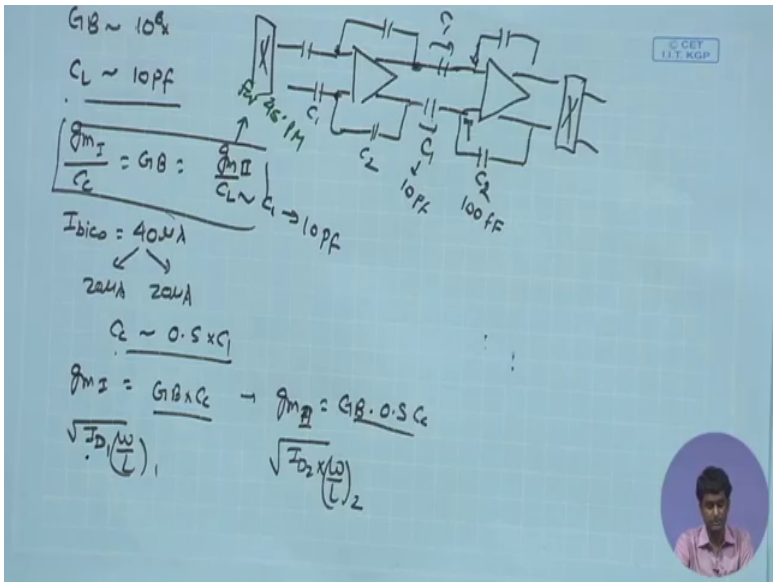
So, in summary we arrived at the sizing of the transistors W and L 1 of the input device W and L 2 of the load device over here as well as W and L 3 of the input device of the second stage. We also concluded that W and L requirement of the especially the W by L requirement of the fourth m 4 transistor is not so critical because signal swing is not so important for the first stage of amplification. And therefore, we can afford to have relatively smaller W by L for the load device.

And finally, we were discussing the W by L requirement of the m 5 and 3. Once again the condition that must be satisfied is that you we should have a sufficient headroom for the m 5. So, that it remains in saturation under all conditions if you look at the circuit configuration where this amplifier is being applied we know that the gate potential of this amplifier is being said with the help of the resistive feedback. So, in the very beginning we have seen that we can implement the very high value resistance using the

sub-threshold region transistors and we can establish and DC bias over here which is equal to the DC bias at the output nodes.

And we kept it equal to VDD by 2 or close to VDD by 2. So, that our overall swing is maximized at the output stage.

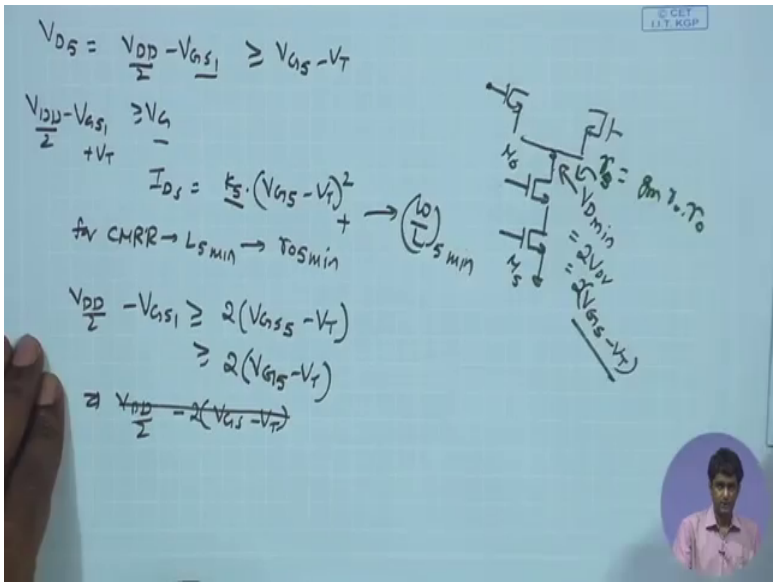
(Refer Slide Time: 01:48)



And if you look at the overall feedback operation if we have a feedback amplifier implemented using C, we know that the signal swing at this point is not going to be significant as a result these two points are going to be close to a constant DC potential you do not have much signal swing over here.

Therefore, signal swing is not going to be an important consideration and also the DC potential is known VDD by 2 for that I have a certain VG s drop for the m 1. And therefore, the VD 5 if I can say the VD 5 let me just keep the same figure so that we can refer to that.

(Refer Slide Time: 02:25)



So, VD 5 is going to be VDD by 2 which is basically the VG 1 minus VGS 1 and VD 5 must be greater than equal to VG 5 minus VT in order to satisfy saturation condition.

Now, the VGS 1 if you have already determined the W and L of the m 1 and also the bias current we have the VGS 1 also known. So, basically the VGS 1 becomes parameter which is known to us based on the par set values of the W and L and the id of the input devices. And therefore, I from here I can get the constraint on the vg. So, VG 5 should be less than equal to VDD minus with sorry VDD by 2 VDD by 2 minus VGS 1 plus VT.

So, this is the value of the minimum value of VG that I would sorry the maximum value of VG that I would need and we know that the VG is going to ultimately determined by the bias current and W by L of m 5. So, I know that id 5 is equal to the k 5 which is a constant parameter for m 5 the trans-conductance parameter VG 5 minus VT square. And from here I can set the desired k 5 to obtain VG 5 within limit and k 5 1 second depends upon W by L ratio. So, if I increase the W by L of m 5 I am going to get a smaller VG 5 required. And hence I can satisfy the limit VG 5 less than equal to VDD by 2 minus VG plus VT or in other words VDD minus VG minus VT which is just an overdrive voltage.

So, this constraint has such may not be very difficult to meet for example, in our case VDD by 2 means 0.9 and minus a be over drive of the input devices it may be close to say couple of 100 millivolt at max. So, this means that the VG should be lower than say 0.9 minus 0.2. So, around 0.7 and for a bias current that we are choosing in our

applications say around 20 microampere for this stage you having a VG 5 of lower than 0.7 is not very difficult W by L ratio close to 10 or 20 can easily achieve VG s required around maybe close to 0.5 volt close to very close to the VT voltage of the m 5.

So, since we know that one eighty nanometer technology model that we are using in simulations also the value of VTS around 0.4 volts. So, we can expect overdrive voltage of around 0.5 volt to be there if you are using nominal values of W by L say around 10 something, but another very important constraint that comes by determining the W by L of m 5 is common mode rejection ratio which is also going to play an important role in determining the W and L values of m 5. So, we know that the CMRR is active proportional to the r o of the current source which is in turn proportional to the channel length of this current source.

So, the CMRR we need a certain L 5 min because that is for a given bias current that is going to determine the r o 5 min r o 5 min and as a result for a given bias current this may set a required L value. So, from here I can get the L 5 min. And now I have the constraint on VG from where I can get the W by L 5 min. So, this combined with the k 5 constraint is going to give me W by L 5 min in order to achieve the required CMRR and also the L min required to sorry the L min required to achieved required CMRR and the W by L min to achieve VG which is lower than the max limit specified over here. So, these 2 constraint need to be considered together to arrive at the W and L values of m 5.

So, once again in symmetric W by L of m 5 being determined by the upper limit on VG which is once again coming from the required or the given value of VG 1 minus the VGS of m 1 which is also known given our W by L and id of m bar is known. And therefore, I have the upper limit of VG 1 known in order to keep m 5 min saturation and in order to get the L value we have the CMRR ratio CMRR constraint and for that L min I can get the W by L min, and hence at the W rro that minimum value or slightly larger than that minimum values that we are achieving both the constraints.

And remember in order to get better CMRR we may often go for cascade current source over here and in that case the swing constraint may become more critical and then W by L ratio of m 5 may become more critical. So, if you are going for a better CMRR and using cascade then we know that the required minimum drain potential over here for m 5 will be 2 V overdrive.

So, if you recall our discussion on cascade current source if you are having a cascade current source rather than the simple one and this is the common source terminal for the diff amp the first stage diff amp then the minimum potential over here is going to be VG minus the 2 V overdrive if we are using reduce swing cascade. So, remember we discussed certain techniques through which we can bias this cascade current source such that you can have minimum allowed drain potential over here equal to 2 V overdrive.

So, we have looked into such a biasing circuitry such that you can have the V d min over here equal to 2 V over drive equal to 2 V g s minus V t and therefore, in this case it will be important to minimize this VGS minus VT so that the VD min corresponding to the given gate voltages met. Once again our equation over here will get modified slightly only things we have to write is this V d min or the VDD by 2 minus VGS 1 that we have which is equal to the VD that is greater than equal to 2 V overdrive which is 2 VG s 5 minus VT or if I call this say m 5 and I call this m 6 just for the time being I can write this as VG 5, because this is the lower one and VG s 5 equal to VG 5.

So, this should be greater than equal to 2 times VG 5 minus VT and therefore, once again I am going to get the constraint that VG the; or in other words the V overdrive of m 5 is determined by this equation. And therefore, I can write down the expression for V G 5 from here and this V overdrive expression from here I can directly get the W by L required, because this is basically going to give me the k 5 required for a given id 5 id 5 already been set from the previous equations based on the band the gm requirements and the current budget that we have based on this I can get the k 5 required from here.

So, definitely in this case the W by L required will be larger because you are having the overall 2 factor coming over here. So, we can definitely have a larger W for m 5 in that case to cater for higher VD min to account for the 2 V over drive drop across the transistor so, that is only constraint we have this will be able to meet the CMRR you show much better because we are not relying on only the channel length or the r o to get the better CMRR.

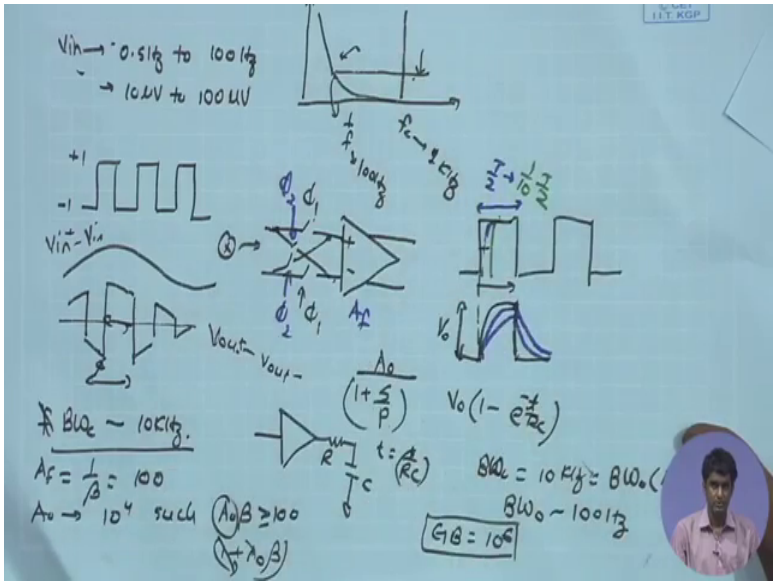
Now, my output resistance looking into this node we know this is going to be gm r o times rho. So, the r o is going to be or you can say the r s the overall impedance looking into this source terminal is going to be gm r o times r o and as a result I am not relying only on increasing the channel length. So, although I am having a larger overdrive

voltage, but here I can afford to have long to smaller channel length I do not need to really have very large channel length to meet the r o requirement because I have the gm r o factor coming in which can be pretty large.

And therefore, I can have relatively smaller channel length, but at the same time I am able to achieve much larger r o 5 and as a result the VGS of this individual devices can still be smaller, because the L can be taken as smaller in the earlier case we were dependent only on the L larger L means larger r o and therefore, we were forced to have a larger W just to have the same W by L ratio needed to maintain this VD min, but now once you have 2 stacks there the overall r o 5 gm r o times r o and as a result I am less strongly dependent upon l.

So, I can afford to have a smaller L for a given current and smaller r o for each of this individual device, but still get large gm r o times rho. So, that relaxes the dependency on L. So, this is regarding the sizing of m 5. So, we have basically completed the cycle starting from the in the initial high level specification down to the design or sizing of each of the transistors starting from the very beginning values. Once again will try to iterate and summarize our discussion starting from the very beginning looking at the signal characteristics.

(Refer Slide Time: 12:41)



Looking at the target of one upon f frequency and hence choosing the fc to be 10 times higher than that leads us to chopping frequency fc. And we are targeting a settling time

which is 10 times faster than this period that lesser to the open loop bandwidth the closed loop bandwidth and also the closed loop bandwidth, and the required closed loop gain of 100 and the corresponding precision a beta being greater than 100 for A 1 percent accuracy leads us to the open loop gain.

The open loop gain combined with the closed loop bandwidth gives us the open loop bandwidth. And once we have the open loop bandwidth and the open loop gain we have the gain bandwidth product once we have the gain bandwidth product I can go back and look at my transistors and determine the values of g m 1 upon c c and g m 2 upon cl, because these are going to be equal to gain bandwidth product. The gain bandwidth product of the 2 stage op-amp is equal to g m 1 upon c c which is equal to g b. And for 45 degrees phase margin I want my g m 2 upon c L which is basically p 2 for 45 degree phase margin I would like this p 2 value to be equal to the gain bandwidth product that is how I got this relationship.

And then for the power budget I have a total bias current of 40 I divided into 20-20 and also I assume that I would like to keep the cc significantly smaller than c 1 or the c L over here. And how did that c L come into picture that is again the input caption to the next stage which they really c 1 of the feedback amplifier that give me the c 1 value and I would like to keep the cc maybe half of that c 1 and that give me this c 1 and hence c L and also the cc and for the given bandwidth gain bandwidth product we obtain the value of g m 1 and g m 2.

So, that give me the g m 1 g m 2 I also have the id one id 2 from the power budget that give me the W by L of 1 and W by L of 2. So, till this point I have the W by L a ratio of one the input stage and the second stage input device. So, here 1 and 2 means you are looking at the g W by L of the input device of the first stage and W by L of the input device of the second stage.

Now once we have that now we look into the gain requirement A 1, A 2 of the first and second stage the overall gain requirement open loop is 10 to the power of four individuals 10 to the power of 2. And hence the for a first stage we said that the gain is going to be gm r o, because the noise constraint is going to tell us that will have to keep L l of m 2 larger. Therefore, I want to keep the r o of m 2 larger. Therefore, the gain is going to be determined by gm r o therefore, I said g m 1 r o 1 equal 200 that gives me the

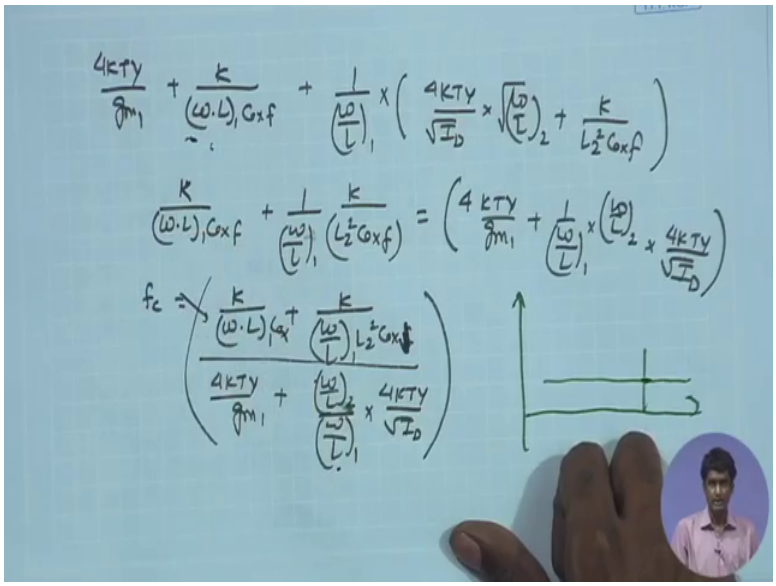
r o 1 value required I have the g m 1 value known from the previous steps. I therefore, might to need to get the r o 1 value and this is equal to one upon lambda id budget is fixed.

I can take that id and from there I can get the value of L required. Remember that the channel length modulation factor is depends on the L larger is the L larger will be the r o for a given current. And therefore, I need a certain L 1 min to meet my r o one requirement so that sets the value of L 1. And once I have this value of L 1 set I can go ahead and determine the W 1, because W 1 W 1 by L 1 ratio has been determined earlier. So, that gives me that W 1 upon L 1 and likewise if I have to go for the second stage once again I have the W by L of to determine g m 2 is also determine bias current is also determine.

So, I have the W by L 2 known and likewise in the second stage if I assume that the r o of these 2 devices are going to be similar because there is no significant noise constrain over here. So, I can afford to have r o of these 2 devices similar. And therefore, the r o factor becomes known gm 2 is known gm mins the second stage gm is known times r o is equal to the overall gain required from this stage which is once again 100. So, that gives me the overall r o required on this stage and which is once again going to give me the L required of this stage and once you have the L required and W by L required I can find out the W and L for the m three device.

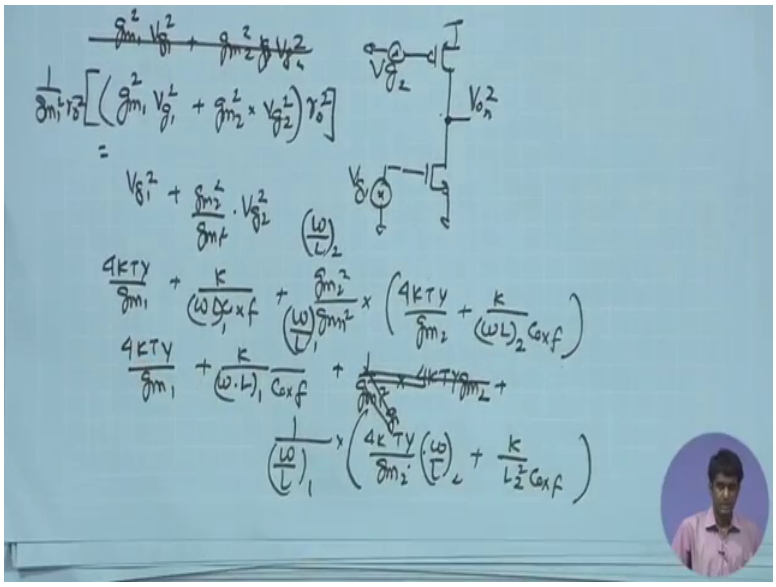
So, this is how I get to W 1 L 1 W three L 3 where W by L of the input devices of first stage W by L of the in the input device of the second stage. And then we looked at the load device and for that we can go back to our expression for the noise.

(Refer Slide Time: 17:29)



And we can look at the one upon f noise corner. So, this was our expression for the input referred noise that we arrived at earlier. And that was done by dividing the overall put noise divided by the gain from the input to output.

(Refer Slide Time: 17:37)



So, this is the expression g m 1 VG 1 g m 2 VG 2 square times r o square divided by the gain which is gm one square r o square from this point to this point. And then we have the overall expression for the total noise. And if you want to get the one upon f noise

corner I need to equate the 1 upon f component to the thermal noise component and that is how we obtain that one upon f noise corner of the amplifier.

And here we can see that if we if you look at the one upon f noise corner obtained by equating the white and the one upon f components I can look at the dependencies I in the denominator in the numerator I have W L 1 and W by L 1 times L 2 square. And this would suggest that in order to for a given W and L 1 that we have already determined for that if I have to minimize the second component over here I would choose a certain larger value of L 2.

So, that this gets further minimized and also if the noise constraint is not satisfied if I want to push the one upon f noise corner further it may be advisable to increase this first factor further that may imply increasing the W further and increasing the L 2 further I can also increase W L 1 both that will require you know larger increase in L 2 because it needs to cancel the increase in L 1.

So, that constraint again can be looked at attractively if the given W and L 1 that we have arrived at if it is satisfying the one upon f corner and just by increasing L to be are able to reduce it further that is meeting the one upon f constraint that is otherwise we have to once again increase the W 1 over here and L 2 over here to suppress the one upon f corners further. And apart from that we have also discussed how important it is to reduce the thermal noise floor. Remember the concept of noise folding which leads to the folding of the thermal noise to the lower frequency after anti chopping process. That means, the one of the white noise floor should also be sufficiently suppressed and for that I need to look at the other component the white noise component coming over here which is given by 4 kt keep upon gamma g m 1 and also you have the other term coming over here.

So, once again we see that that is depend upon g m 1 and W by L 2 and W by L 1 ratio. So, once again having a smaller W by L 2 also automatically helps us suppress the white noise component. So, that is not a conflicting requirement or automatically satisfied if you are trying to suppress the one upon f corner frequency only thing is you have the W upon L 1 coming. So, we have to make sure that the W upon L 1 ratio is sufficient and by having a larger L 2 ratio you have any way degrading the W by L two. So, this

component gets minimized if I am following the one upon f noise minimization likewise the first component also gets minimized if I am increasing the W of the input device.

So, the white noise constraint can also be simultaneously satisfied when we are trying to push the one upon f corner frequency both of them can be shifted toward lower values. So, assuming that whatever W and L 1 and the W and L 2 of the input stages than the second stages we arrived at that is satisfying the one upon f corner frequency, and white noise constraint we can go back and then look at the W by L off the bottom device.

And they are also we concluded that the bottom device is not having a significant W by L constraint, because the output swing is not a major constraint in our forin and first amplifier the W by L ratio can be W by L ratio of this one can be relatively lower, because the W by L ratio of m 4 is mainly governed by the minimum output swing over here. If we have a certain minimum output swing V out min that we out min I need to have make sure that the VG 4 is lower than V out min plus VT V out min plus VT that is the constraint.

So, if I have a certain minimum output voltage level V out min it will, in order to make sure that this is an saturation VG 4 must be lower than V out min plus VT. However, we have look into the overall amplification over here which is going to be at the max 100 close loop as a result our 100 micro volt getting multiplied by 100 and the max 10 millivolt and hence we do not have a significant constraint over here VDD this is bias VDD by 2 VDD by 2 plus minus 10 millivolt. And hence this may not pole a serious constraint regarding the VGS of the m 4 device specially when our current is small as just 10 microampere there for the driving constraint of m 4 is more involve sorry less involve.

Likewise, if I go for the last one which is the m 5 there we saw what are the constraint the saturation engine operation of m 5 is an important constraint, because here in our example that DC potential is fixed input range is not very important constraint for that DC potential I just need to make sure that this always remain in saturation. So, for that I need to fix the W by L to the required minimum value.

Second thing is the L value of m 5 which depends upon the CMRR ratio. So, for that we need to have certain minimum L for m 5 and we also saw that if you use cascode for m 5 you can relax the constraint on the L or the r o and still get a good CMRR. So, these are

the design constrain completing the discussion on sizing of the W by L for each of these devices.

So, we can extend the similar discussion to the next stage which is our variable gain amplifier where the noise constraint is relaxed, whereas output signal swing is an important constraint. So, very briefly we can connect this with the output stage noise sorry output stage the second amplifier stage sizing let us briefly discuss that. So, if I look at the steps which are the steps which are going to remain same. So, till this point getting up to the r o. And hence the L value there till that point we are having almost similar constraint. So, we started with the gain image requirement we looked at the required value of the cc and the required value of g m 1 g m 2 that remains same that is not affected by the noise constraint.

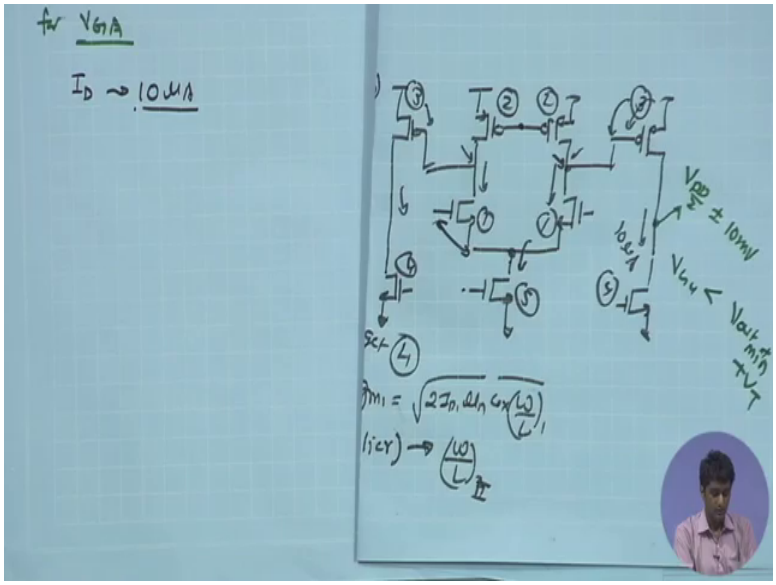
So, till that point I have no issues when we come to the gain of the first stage there we had included g m r o only because there we assumed that the r o of the load device is going to be pretty large because we are going to assume very large channel length, but for the second stage that may not be a very important constraint. And we can have relatively smaller channel length for the output device and we can assume that the r o of these 2 devices are similar and hence the gain can be striated as gm r o by 2 rather than g m ro.

So, in that case we can assume that both are having similar channel length and from there I can determine the r o or the L required for these devices. Once I have the L required for these devices once again the W by L is known from our previous step I can get the W by L for both these devices for the given g m. So, the gm value will give the W by L for the input device and I have the L over here. And once again I can see in order to determine the W of this device how do I you know need to what constrains do I need to follow.

So, in this case since the output swing is critical the W of the load device can be exploited to improve the output swing. So, that will be a slightly different step as compared to the sizing of the fronted amplifier let us see how the W of this one can be helpful. So, for that we first need to look at the output stage. So, till this point we have agreement with the analysis done for the fronted amplifier a second variable gain amplifier we are looking at the output stage and output stage. Once again we have for the

output stage. Once again for the variable I am calling it a VG or a variable gain amplifier because this is the second stage.

(Refer Slide Time: 26:07)



So, if I look at my system diagram in the very beginning we have discussed this is going to be the variable gain amplifier relatively lower constrained on noise is higher constrained on swing this is my VGM discussing. So, for the VGA I have I have several other optimization that I can also make I can also look at for the reduction in the bias current values as well if I look at the thermal noise floor you have the id of the you know first stage coming into picture. And therefore, having a sufficiently large id and gm of the input device becomes crucial in minimizing the thermal noise floor as well, whereas in this case you have relatively smaller noise constraint. And therefore, the constraint on one upon f noise as well as thermal noise going to be relaxed.

So, if I look at the overall you know noise expression over here I can afford to reduce the bias current of the first stage if the noise is not a such a critical constraint, because there is not going to play a very important role in determining the overall input effort noise of the whole system and that will also degrade the gm one little bit that can be compensated if you are increasing the W and W by L of the input device.

So, that can once again be compensated, but as we are seeing that the id one and gm one even if it is slightly degraded it is not going to affect my overall a noise input referred noise so much for this, because this is the second stage. So, I can relax the power budget

also rather than going 40 microampere I can go for relatively lower currents maybe just aggressively down to 10 microampere so that I can keep cutting down on the power budget. So, that is one possibility I can go for relatively lower bias current requirement.

So, I can go for an id or I total budget within say you know 10 microampere for the first stage we assumes the 40 microampere here we can go for 10 microampere 2.5 microampere in each branches and once again that would imply that would affect our selections of the gm as well.

So, if we stick to the bandwidth because the bandwidth of this stage is also going to be similar to the bandwidth of the first stage if we are applying chopping for this stage also and that in general is true, because in many cases the anti chopping operation will be performed after the second stage amplifier. So, you may have chopping at the first stage you have the chopping at the input of the first stage you have the first chopper switch here anti chopping we performed altogether after the second stage.

So, in that case also the one upon f corner frequency of this one may not you know be very critical because signal is still at high frequency. So, in that case once again the amplified over here has to process the same bandwidth. So, this is the bandwidth constraint remains similar as compared to the first stage. So, the gain bandwidth product of this stage also remains similar, because the overall signal frequency a signal characteristic is similar. So, that is another constraint that we have. So, the gain bandwidth requirement and the bandwidth requirements similar we have also by furcated the overall gain as the 2 half.

So, we are said that overall of gain of 10 to power of four is going to be reached by combining 10 to power of 2 10 to power of 2 over here. So, therefore, gain is also remaining similar bandwidth also remaining similar. Therefore, the gain bandwidth product for this stage is also remaining similar and next question is regarding the cl of the stage.

So, here we conveniently assume that at c L of this particular stage is equal to c 1 for this stage. Once again we have see what is the next stage output and that is going to determine ultimately what is my c L and that question will come clear. If we look into the subsequent stages whether it is a filter or whether it is any other block like an ad c. So, in

general after this we will have an anti aliasing filter a low pass anti aliasing filter and we may also have some component in the feedback that will be discussing later.

So, in effect those components will also provide an overall capacitive load the load over here can be resistive as well and in those cases the capacitive load will be dominant and we can assume the similar value of load capacitance for simplicity for the time being later when we look at the filters will have better idea about the input impedance is provided by those filter depending on the kind of chop topology. We are implementing whether this is capacitive filter or a GMC filter. But for the time being you can assume that the next stage is also capacitive load and overall capacitance is similar. So, in that case the com computation of the gain bandwidth product and the gm one gm 2 also remains similar.

So, let us stop here for a few minutes. So, here we have just tried to distinguish the sizing constrain of the second stage amplifier with respect to the first stage amplifier. So, any question to this point before we go ahead and try to look at the transistor level sizing of the second stage just minor differences, but you know to complete the picture will be looking at the remaining sizing constraint transistor level sizing constraint of this amplifier.

So, far we have just distinguish that what are the constraints which were applied here, but not applicable here and what are the additional constraints that are coming up which are applicable here and high level what are the con specifications which are similar. So, those are the things we have complete high level specifications similar gain bandwidth lower level specification transistor level noise not important swing important. And then the steps till which we are going to have similar effect is similar you know sizing is determination of gm 1 gm 2.

And from there we have some minor differences that we are looking at any question before we take a small break and resume the discussion on transistor sizing for the second amplifier. So, we can take a short break. And then, after that we can resume our discussion on the remaining sizing considerations and try to conclude our discussion on sizing of the 2 stages that is a fronted amplifier and the variable gain amplifier design.