Analog Circuits and Systems through SPICE Simulation
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Lecture - 32
Transistor Level Design Of Fronted Amplifier

Welcome to today's session as we discussed in the last module we are going to look into transistor level design and sizing of transistor for a two stage op amp that we have been working on and in the very beginning of the sessions we looked at the high level specifications for the system which is a biomedical fronted acquiring a neural potential data, and we derive certain specifications for the fronted amplifier for example, in terms of bandwidth gain, the precision required accuracy required and so on.

So revert back to that discussion and from there you will try to link the transistor level parameters the transistor dimensions, now we have all the other information all the other recipe required to do the sizing, we have the noise analysis, we have the frequency response, we have the compensation stability all that coming into picture also other considerations related to signal swing etcetera that we are also aware of. So, we have all these recipes based on that we can look at the transistor sizing required to meet the high level specification of the amplifier. So, let us get started.

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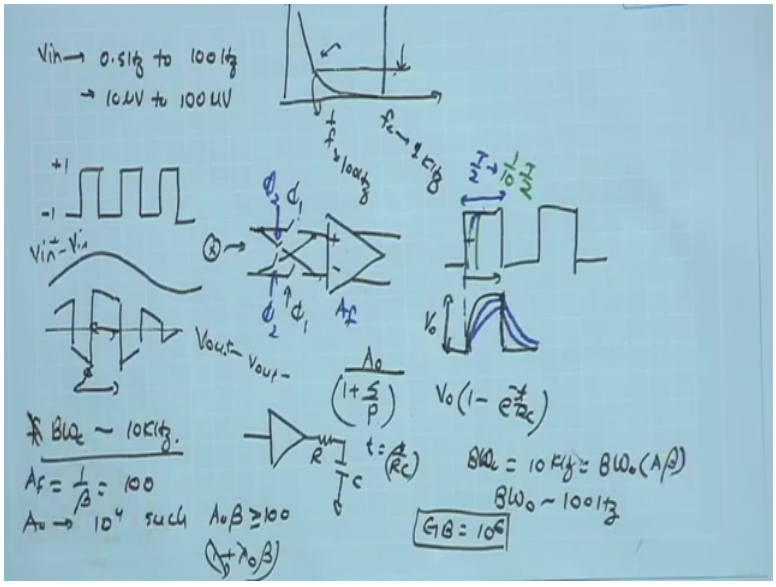

So let us recap very quickly the signal characteristic that we are looking at. So, we are looking at the neural potential signal which is having signal contained say from 0.5 hertz all the way to say 1 kilo few 100s of hertz basically 100 hertz. And in order to save this signal which is having a very small magnitude 10 microvolt to say 100 microvolt, in order to save the corruption of this signal from noise be discuss the concept of chopping and we considered shifting this signal to a high frequency with the help of a chopper, and we discuss the concept of 1 upon f noise and how chopping can help us in mitigating the 1 upon f noise effect.

So through designed an analysis we can of course, try to push this 1 upon f corner frequency towards lower side and we have seen in the different amplifier topologies that we have discussed how the 1 upon f noise depends upon the transistor sizing so and of course, the bias current. So, one target can be that for a given bias current limit that you have for a given current budget that you have in the circuit, you can try to push this 1 upon f noise corner towards as low frequency as possible, and likewise another target happens to be to minimize this white noise level for the noise spectrum.

And once you have done that then we decide the chopper frequency fc with which we are going to multiply the signal, and we assume that fc is sufficiently higher than this 1 upon f corner frequency maybe at least 4 or 5 times higher than the 1 upon f corner frequency so that the input signal is sufficiently isolated from this 1 upon f noise spectrum. And in our case if we are say able to push down the 1 upon f corner frequency to say 100 hertz, and then assume that the fc should be at least 5 times or say to be more conservative 10 times higher than that, then you have chopping frequency of one kilohertz available. So, suppose 1 upon f corner frequency is 100 hertz and the chopping frequency is accordingly 1 kilohertz and order of magnitude higher. This is a little bit more conservative I can go for slightly lower also, but let us target little bit conservative values.

So let us keep the chopping frequency to be 1 kilohertz. So, now this is the chopping frequency for the amplifier, from there we need to look at the amplifier bandwidth required to support this chopping frequency. So, once again if I look at the chopping behavior ideally if I do mathematical modeling, the chopping would imply multiplying of an input signal with plus minus 1. So, this is plus and this is minus 1 and you have the input signal varying, and mathematically I can just multiply these two and get my output

signal desire output signal, but when we are trying to implement this in the circuit ultimately, we have the amplifier input suppose this is your feedback amplifier with the feedback component included within this triangle.

So we are trying to have this implementation using cross couples switches and we have seen that during the first phase phi 1 the input gets connected to the first you know polarity plus minus and in the alternate phase phi 2, the signal polarity gets reversed and the signal will be getting connected to the minus plus terminals. And this effectively means that in the phi 1 cycle the signal over here is getting multiplied by the gain AF, if the closed loop gain is AF this in the phi 1 cycle it is getting multiplied by AF, in the second cycle phi 2 the signal is getting multiplied by minus AF. And hence, we have a plus minus AF multiplication happening on the input signal and ideally of course, that would mean that the output signal if I look at the fully differential output V out plus minus V out minus that will be just getting chopped accordingly.

So you will have the overall amplifier signal getting chopped so this is what we expect. So, if I look at V out plus this is your V out plus minus V out minus we expect the input signal I am assuming this is your V in plus minus V in minus input, signal getting multiplied by this plus minus 1 as a result every cycle you are getting the output signal changing the polarity in a stepwise fashion. Now this is a mathematical picture, but if you look at the circuit of course, circuit cannot have a ideal step like rise and fall time it will take some finite time to settle to a certain value.

So for example, if I consider one particular time instance where the phase is changing from phi 1 to phi 2 there of course, the signal the input signal is shifting the or reversing the polarity and within this rise time or within this duration the output signal should finally, settle to a times V in plus 1 is V in minus. So, if I assume that this is going to act like a step function. So, the clock function assumed that clock is the clock which is the phi 1 it is acting like a step function, and it is getting switched at a certain frequency given by fc 1 kilohertz.

So within the half time period of fc assuming 50 percent due to cycle within this half time period of fc, the signal which is coming at the output should be able to settle. So, the output signal finally, should be able to settle. If I assume say that the amplifier is a single pole system assume that there is one dominant pole. So, I can represent the

amplifier transfer function as 1 upon 1 plus S upon P where P is the dominant pole and this is basically representing a single pole RC system. So, I can represent this as an ideal amplifier followed by an RC low pass RC filter.

so I can represent this as a ideal amplifier with gain a and then RC filter where 1 upon RC equal to p and if I represent the time constant t as say 1 upon p or 1 upon; sorry, time constant as 1 upon p or RC we know that this kind of system is going to have overall you know time domain response given by V naught 1 minus e to the power of minus t upon RC. So, if V naught is the step that is the output is supposed to take suppose Vo is the step that is output is supposed to take in the this going to change from V to V plus V naught.

So this is the overall step that is expected in the output as a result of change in the input. So, this I am calling as V naught, another result for a single pole system we have an overall response coming like this V naught e to the power of minus t upon RC, and if the pole is towards lower frequency where the time constant is larger than we know that this RC time constant will be worse and the charging will be or the rising of the signal can be much slower. Likewise on the other side when you are going towards the negative phase phi 2 there I expect that a signal will be going down, there also if the RC time constant is large or the pole is towards low frequency rather than the signal going down quickly it will take good amount of time to go down. And it may so happen, if you can see it may so happen that the signal does not even reach the required value it does not even reach the final value. If the clock frequency is much larger as compared to the pole frequency the signal may not be able to reach the final distant value.

As a result the final value that you get is going to be dependent or it is going to be having non-linear dependency on the input signal. If your input signal change is smaller or the delta being that we are seeing over here is smaller then it will be able to settle more you know conveniently, but if the delta V input is larger it will take larger time to settle or it will not be able to reach the you know maximum value that is supposed to be there. So, it can lead to non-linearity and the ideal multiplication function that we are trying to implement that will not be achieved.

So you would like to have this settling as fast as possible. So, this rice time should be much smaller as compared to the overall half period of the clock. So, I would like my

signal to settle much faster. So, within one if this is T by 2, I would like the settling time to be close to one by tenth of this. So, I would like this settling time t settle within this the signal is settling to the final value if I call this T settle the time taking by the signal to reach the final value trusting for the sampling instance I would like this to be at least say to be conservative 1 upon 10 T by 2 and; that means, the pole frequency will be 10 to 20 times higher as compared to the frequency of the chopper.

So if the pole frequency is higher or the bandwidth of the amplifier closed loop amplifier is much higher, then the chopped signal at the input and the output finally, it will be able to settle properly to the final value. That is the reason why we need to choose the pole frequency much higher than the chopping frequency. So, if I assume that the chopping frequency has been taken as one kilohertz that would imply that the amplifier bandwidth would be even larger maybe at least around 5 to 10 kilohertz to be more conservative maybe 20 kilohertz.

Let us take with a reasonable number 10 kilohertz. So, if fc is 1 kilohertz let us go for the closed loop amplifier bandwidth as 10 kilohertz. So, we have discussed this briefly while discussing the chopping operation also that why do we need to have a higher amplifier bandwidth when we go for a chopping operation. So, chopping is helping us in shifting the signal towards higher frequency 1 kilohertz, but the amplifier bandwidth needs to be even higher than that, because the chopping clock is acting like a square pulse and within that the signal must settle fast enough and for a good performance I would like my signal to settle within one tenth of that half period.

So in this case let us choose the amplifier bandwidth to be 10 times fc let us call it closed loop bandwidth. So, f or bandwidth close that can be chosen as a 10 kilohertz. So, this is the such a modified requirement that we have as compared to that we started with what we started with in the very beginning. In the very beginning we did not consider the concept of 1 upon f noise you are chopping and we started with the name assumption that yes your signal frequency is from 0.5 hertz to 100 hertz.

So possibly I can design my amplifier to meet this particular bandwidth. In certain cases where the signal strength is sufficiently large, we may be able to do away with the chopping for example; if you are talking about some biomedical signals which are having much stronger amplitude rather than few tens of microvolt they will be having

few millivolts at least. So, in that case the signal magnitude is sufficiently large and even if the frequency content is down to you know close to even fraction of hertz, you can do away with chopping. But in cases where the signal magnitude is so low 10 microvolt or few microvolts there the 1 upon f noise becomes very serious and as a result I have to we have to go for the chopping operation.

So in case of the particular application that we targeted neural potentials they are of course, the signal content the frequency content is this what the amplitude is also pretty low and that would necessitate the use of chopping we are talking about some other signals like an ecg signal. For example, they are the amplitude coming from the electrode can be pretty significant or pretty large as compared to this field can be few millivolts. So, they are chopping may not be necessary, but for neural potential acquisition because of much smaller include amplitude chopping becomes very important almost necessary.

So let us now conclude that the closed loop bandwidth supposed to be 10 kilohertz and now we need to look go for the open loop bandwidth and the gain bandwidth product. So, the gain that was expected was the closed loop gain overall say we are going for around 10 to the power of 4 that is what we estimated. So, if for example, if you have in the maximum signal amplitude of 100 microvolt and then the closed loop gain is in the power of 4. So, the maximum peak to peak swing that you can have at the final stage is going to be around 1 volt. So, for a two volt we ready 1 volt peak to peak swing can still be tolerable if you design the amplifier properly.

So that the output stage swing is maximized then you can go for larger output swing and therefore, the overall gain that we are targeting from the amplifier stages and maybe even the filter stages overall it will be 10 to power of 4; and then we can divide this gain into two stages. So, we also discuss the rationale for that rather than going for single stage we can divide it into two stages and one single amplifier was supposed to have a gain of closed loop gain of around 50 to 100. So, let us you know take it to be 100 at the max more reasonable numbers are 30, 40 50.

So let us take let us be more aggressive let us take closed loop gain of around 100 for each stages and therefore, we have the AF which is going to be approximately 1 upon beta equal to 100, and also we have the A 0 and remember how did A 0 come into picture A 0 is determined by the precision required. So, the 1 plus A 0 beta term if you want to

ignore that one with respect to A 0 beta the overall A 0 beta should be at least 100 times higher than one if you are going for one precision and therefore, here if I am taking beta equal to 1 upon 100, I would like to have A 0 10 to the power of 4.

So this would give me A 0 around 10 to the power of 4. So, that such that A 0 times beta is greater than at least greater than 100 greater than equal to 100 that will ensure that you have one precision in the term 1 plus A 0 beta when you are ignoring this one with respect to A 0 beta you are incurring an error and that error should be less than 1 percent for that I would like this A 0 beta to be greater than 100 greater than or equal to 100. So, that give me the A 0 10 to the power of 4.

So from here we have the open loop gain of the amplifier, and we also have the closed loop bandwidth. So, from here we can also obtain the open loop the gain bandwidth product and the open loop bandwidth of the amplifier. So, the closed loop bandwidth is targeted to be 10 kilohertz and we know that closed loop bandwidth 10 kilohertz is going to be equal to open loop bandwidth sorry Bw this is going to be open loop bandwidth Bw open times 1 plus a beta one is small so times a beta approximately. So, here we have also seen that the a beta is we are choosing it to be around 100 and as a result the open loop bandwidth can be taken as 10 kilohertz divided by 100 and therefore, the bandwidth open is around 100 hertz that is what we looked at.

So open loop bandwidth of the amplifier that we are trying to design is around 100 hertz considering the gain bandwidth product requirement, and also we have the A 0 as 10 to the power of 4 and that gives me the gain bandwidth product GB is equal to 10 to power of 6. So, this is our modified set of gain and frequency consideration that we arrived at considering the chopping operation considering the 1 by f noise mitigation. So, the gain bandwidth product is a important feature of the overall open loop amplifier with which we can begin the design.

And now while looking at the design we have to recall how does the gain bandwidth product depend upon the circuit parameters of say the two stage op amp, and from there we can proceed step by step and look at the other parameters like the overall bandwidth and the signal swings and include them step by step also looking at the interface of the circuit with the next stage and the previous stage, we have to estimate the value of the

load capacitance which is going to play a role in determining the capacitance value compensating capacitor values.

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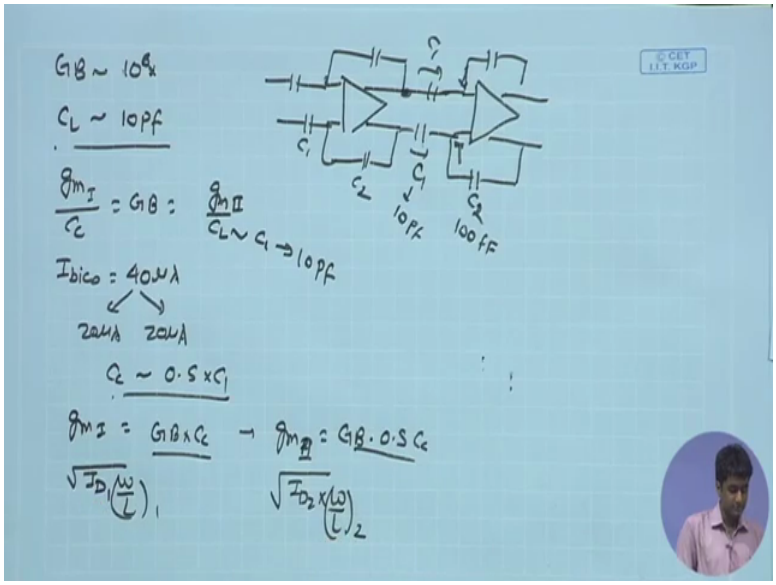

Let us start with the required gain bandwidth product of 10 to power of 6 and of course, if you look at the if you should look at omega there will be two pi 10 to the power of 6 in terms of hertz this is just in the power of 6 hertz. So, let us keep it 10 to the power of 6 hertz and you know if I go back to my two stage op amp we have derived the expression for gain bandwidth product overall bandwidth the overall small signal gain. So, we are going to just use those in order to arrive at the values of transconductance and the compensation capacitor etcetera.

One of the inputs required through the calculation will be the load capacitance, what is the load capacitance phased by that amplifier and what is that in again we have discussed that the load capacitance ultimately for the overall differential operation depends upon the next stage input capacitance. So, you may be having the next stage input capacitance acting as the load capacitance of this stage. So, you have in the next stage once again you know remember that this point is going to be ac ground for the another next stage amplifier, and as a result the overall input capacitance sorry other overall load capacitance experienced by the stage one amplifier, which is built of my two stage op amp is going to be given by this cc or sorry the C 1.

So if I call this C 1 and call this C 2, C 1, C 2 we know that the overall gain for both these three will be given by the ratio C 1 upon C 2, and if I look at this stage the two input points can be treated as ac grounds or rather they are going to be very close together they are going to have any signal swing significant signal swing as a result these two C 1 values appear as effective load capacitance for my output point and therefore, whatever is the value of C 1 we can take it as a load capacitance. And again value of C 1 depends upon the value of C 2 and the gain required and there you should remember the discussion that overall gain 100 that would mean a ratio of 100 between these 2 and C 2 minimum value will be determined by the parasitic capacitance of the amplifier.

So if the C 2 is sufficiently large as compared to the parasitic capacitance of the transistors, then the gain will be relatively well defined by the ratio of C 1 upon C 2. If you make C 2 too small and it becomes comparable to the parasitic capacitances (Refer Time: 21:35) amplifier then it is the gain precision or the gain is less precisely defined. So, I would like to keep C 2 at least few times maybe 10 times larger than the parasitic capacitance value, and we saw that maybe 100 femtofarad is a good value for C 2 and we have seen that the MOSFET dimension these are the MOSFET dimension that we have the overall capacitance that you can get at the output node may be of the order of few tens of femtofarad.

So I am taking around 100 femtofarad for C 2. So, that it is sufficiently larger than the parasitic capacitances at the output node. And then you have the C 1 which again needs to be 100 times the C 2 therefore, we can keep this of the order of 10 picofarad. So, it will be within few picofarad to 10 picofarad that is the expected range of C 1 and in the beginning we have also discussed that at least for a second stage we may need to keep the C 1 programmable or tunable because we may need to adjust the gain of the overall amplifier depending upon the input signal strength.

So sometimes of the input signal peak to peak is increasing, because of the change in the interface property of the electrode and the electronics then the overall gain over here may need to be reduced whereas, if the signal strength is reducing say from you know 100 microvolt it is going to 10 microvolt peak to peak in that case the overall gain of this amplifier stage may need to be increased. So, that depends upon the overall magnitude of the input signal and we have discussed this reason why we need to increase or decrease the gain. So, that we can fully utilize the dynamic range of the adc.

So very briefly we have discussed in the beginning that adc of the fixed input range, I would like to map the final output signal amplified and process output signal to the entire input dynamic range of the adc. So, will discuss that once we have a discussion on adc we will look into the dynamic range concept once again in detail, but if the dynamic range of the adc is a one volt I would like that the output signal over here is always mapped to that entire one volt range. So, that the final output peak to peak swing over here is close to one volt peak to peak.

So if the input signal changes I need to program the C 1 C 2 so that depending upon the strength of the input signal over here I am setting up the gain so that it is mapped to the entire dynamic range of the adc. So, there is there was a concept. So, one of these stages generally the second stage amplification is kept programmable.

Student: Sir this open loop bandwidth we were to consider all these loop capacitance coming or without this capacitance.

Open loop bandwidth ultimately you have to look at the total you know the open loop bandwidth depends upon the critical pole the P 1 which you are trying to compensate and load push towards lower frequency. So, that P 1 is not directly dependent upon the load capacitance as such. So, that it dependent upon only the capacitance the cc the compensation capacitance and the gain of the second stage, that is going to remind the open loop bandwidth. So, that does not have interaction with the.

Student: (Refer Time: 24:39) the output stage (Refer Time: 24:40).

So, as I said ratio is determined. So, in order to get a certain phase margin yes you need a certain ratio between the cc and the CL. So, that way it is related, but if I say that how is the bandwidth determined open loop bandwidth or the 3 dB cutoff frequency of the open loop amplifier as determined by cc and the gain of the second stage cc times a two times the Ro that gives you the RC time constant of the first stage. So, we have so that basically we can assume that the overall load capacitance CL faced by the first stage is say 10 picofarad.

So this is the CL given to us and now we can go back and find out the value of gm in terms of the two stage op amp circuit parameters that, we have we have seen that the gain bandwidth product depends upon the gm 1 upon cc where cc is the composition

capacitor and in order to achieve 45 degree phase margin we said that the gain bandwidth product should be equal to the P 2 or the second pole should be equal to the gain bandwidth product which is equal to gm 1 upon cc.

And but for the second pole value the this is the expression for gain bandwidth product the P 1 times the open loop bandwidth if you remember, and this should be equated to the second pole. So, the pole 2 P 2 should lie at the 0 dB crossing point and I for that I need to equate it to the gain bandwidth product that is what we discussed. So, I would like to make this equal to P 2; what is P 2 value? P 2 if you remember output stage this is going be given by CL the overall load capacitance at the output stage, times the R equivalent at the output stage that basically becomes 1 upon gm 2.

So for the two stage op amp the R equivalent the output stage is just 1 upon gm 2 and therefore, I just need to make sure gm 1 upon cc equal to gm 2 upon CL, and that is going to determine my relationship between these two parameters gm 1 and gm 2 cc and CL also I would like to have certain power constraints. So, since we are looking at a low power application I would start with certain power budget for the overall fronted amplifier, say I take the I bias total as 30 microampere for the total amplifier or say keep it 40 microampere for the total amplifier, and in that case each of the two stages is having 20 microampere each and that means, each branch is going to have 10 microampere.

So it is not necessary to keep the same bias current in all the branches like if you have the first stage differential amplifier, second stage common source amplifier, I may choose different bias currents for different stages and we know that the bias current generally in the first stage needs to be higher or the bias current requirement is higher and the reason is that we have overall gain requirement as well as noise requirement determined by the gm of the input device and specially for the noise requirement we need to have a sufficient bias current available in the first stage.

So, we can factor this bias current to divide the bias current uneven fashion also, we can preserve thirty microampere for the first stage and lower amount of bias current for the second stage or we can go for equal division also that is a design decision and alternatively if I start with a 20 micro 20 micro division and it finally, seems like it does not satisfy the noise criteria I may have to go back, and you know still some more bias currents from the second stage and divide it shifted towards the first stage.

So let us say that we can start with 20 microampere bias current for each stage, and this will give me 10 microampere each for both for all the branches differential branch as well as the output branch. So, this is requirement which is given to me from the top level specification I have estimate of power budgets, I want to stick within this or preferably I would even like to minimize this if my requirements are well achieved within this limit and I have lot of margin left for optimization, we may further try to reduce this bias current to save my power consumption.

So suppose this my bias current gives you a much better gain bandwidth product than required and much better bandwidth than required, then definitely you have an option of going down in reducing this bias current further so that you can save power whiles it is noise criteria. So, this is a starting value you have been given a requirement like this and then it is up to you how low you can go, but you should not cross this, you should not go above up this that is the starting point. So, in the beginning I can try to make the use of the entire power budget that is available to me and then if it comfortably meets all the specs then I have the target of minimizing power consumption also I can go back and try to see how low I can go in terms of this bias current.

So that I can minimize my power dissipation overall while maintaining while maintaining the other specifications specially the noise and the bandwidth. So, I have say the bias current requirement coming over here and then I have the overall the cc and CL ratio suppose to be determine considering the overall area, if you remember the capacitance C 1 they are the largest capacitance over here as compared to C 2 this value is much larger and as a result they are going to meet the most area consuming part of the fronted amplifier.

So whenever you are going for capacitive feedback or even resistive feedback the larger passive component takes the maximum amount of area. So, if you look at the you know physical design of the chip, this C 1 the area will be much larger than all the other transistors area that are building this amplifier and therefore, it would be put in to minimize the values of the C 1 and also the corresponding compensation capacitor. So, compensation capacitor also if it is close to the C 1 or the CL, then again this also becomes a dominant factor and that is also consumes lot of area.

So it would be important to minimize both these areas both these values CL and cc. Now CL we have already estimated that for a well defined gain and gain of 10 to power of 4 overall and hence a closed loop gain of around 10 to power of 2 for one stage, I need C 2 upon C 1 ratio of 100 and as a result I am going for a minimum possible value of C 2 100 femtofarad. So, that is to minimize C 1. So, C 1 is given to me I means this is the minimum value of C 1 possibly I can have to satisfy my range of gain value that I want and then when C 1 is determined I am looking at these values.

Now cc and CL; so CL is basically nothing is, but the C 1 of the next stage. So, I can say CL is equal to C 1 which is equal to 10 picofarad, and then if I make cc equal to C 1 then again I am doubling the area just doubling the area, because cc 10 picofarad means twice the area. Now if I want to be little bit more conservative I would like to push the cc value to the smaller number so that I can save area. So, I will like to make it picofarad in that case I am only 50 percent additional areas being used if I go a little bit more aggressive make it to picofarad then of course, the area consumed by this cc is significantly less as compared to the C 1.

So let us start with a estimate that let us keep cc equal to 50 percent of C 1. So, that it is not adding more than 50 percent areas compared to C 1 definitely one of the important design constraint can be to minimize the cc as well and that again translates to the ratio of gm 1 gm 2 and sizing of the gm 1 gm 2 transistors and so on. So, if the area is very critical and you know every micro meter square is going to count in your design therefore, in those cases you would like to be more aggressive over here I would like to be more you know 0.1 time C 1 or 0.2 times C 1 because I worry about every micro meter square I have to pack. So, many channels I have to pack maybe several times of such channels to acquire multi channel neural potential data.

So that is I will be really conservative about area and there I would like to be more aggressive I will choose a smaller number over here. So, that the overall area can be as minimum as possible for the time being let us just keep this cc as point 5 times C 1 and as a result I have cc value determine and then I have the gm 1 gm 2 ratios individual determine a also the individual values of gm 1 gm 2 can be determined from this equation right. So, once I have determined the C 1 10 picofarad and I also have the ratio C 1 and cc I have basically the value of gm 2 as well as gm 1 known. So, from here I can get the value of gm 1 which is the again bandwidth product time cc and likewise gm 2

which is or let me C 2 the ground number gm 2 is equal to gain bandwidth product times CL which is 0.5 times cc.

And now once we have say the gm 1 gm 2 value determine and the bias current of the two stages determine I also have the value of w by L estimated; because gm 1 gm 2 determined by the ID 1, if I call m one as input device ID 1 times w by L 1 and this is proportional to ID 2 times w by L 2. So, I have these two products determined and as a result since I have already chosen ID 1, ID 2 to be around 20 micro each, I can look at the w by L ratios of these two devices, but w by L of the first stage since it is just double that of the second stage I would need 4 times larger w by L over there to meet the criteria. So, that is giving me the information of w by L for the input device of the first stage and input device of the second stage.

So, this is the w by L ratio we have not determine the w and the L, but at least w by L ratio estimate is here for the input devices of the first stage and the second stage now. So, we can take two minutes break after that we will resume the discussion.