Analog Circuits and Systems through SPICE Simulation
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Lecture - 31
Comparison Of Dual Loop & Single Loop CMFB

Welcome back. And, let us resume our discussion on the dual loop feedback and contrast it with the single loop common mode feedback that we were discussing.

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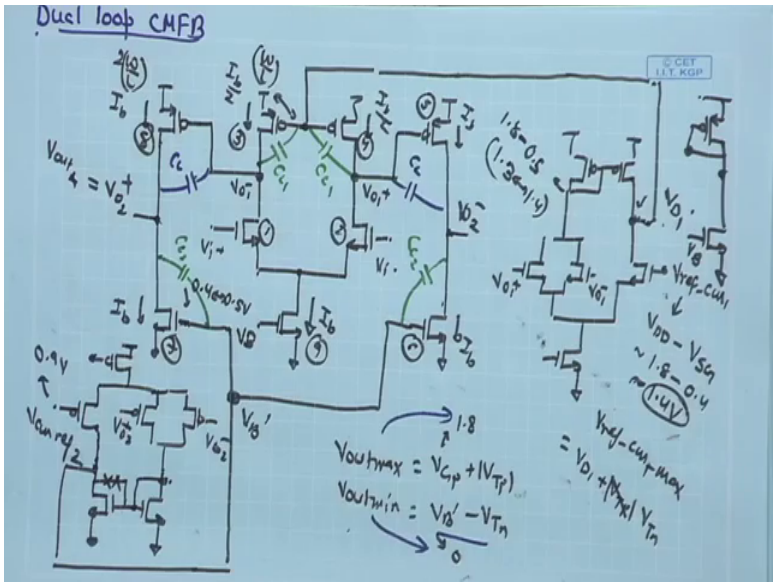

So, we have discussed the basic advantage over here that you know in the two stage common mode feedbacks we are having the advantage of setting the bandwidth of the common mode loop and the differential loop separately and optimize them separately. Whereas, for the earlier case that we had discussed for the single loop common mode feedback we had noticed that the overall bandwidth of the common mode loop as well as differential loop would be dictated by the single C c that was used for compensating both the loops.

So, there of course, both the loops are constrained to the same bandwidth and that may not be the optimal case and that is the major advantage that you can say for a 2 loop common mode feedback for the 2 stage op amp. For the single stage couple of other issue that we need to also address and you know couple of question that we are asked regarding the single loop compensation I would like to briefly address that before we

proceed towards the next topic and continue our discussion on cascode amplifier that we started last day.

So, here if I revert back to our previous discussion on single loop we argued that to keep the amplifier the overall loop gain for the common mode feedback within bound or within reasonable value. We would like to keep the error amplifier diode connected. So, we would replace this current mirror load by a diode connected load. So, that the gain of the error amplifier becomes unity and then traversing the loop you have overall gm ro square gain. If you keep this current mirror load then of course, for the tool loops we have gm ro whole cube and then the compensation and stability can become more difficult more challenging for the for the overall common mode loop.

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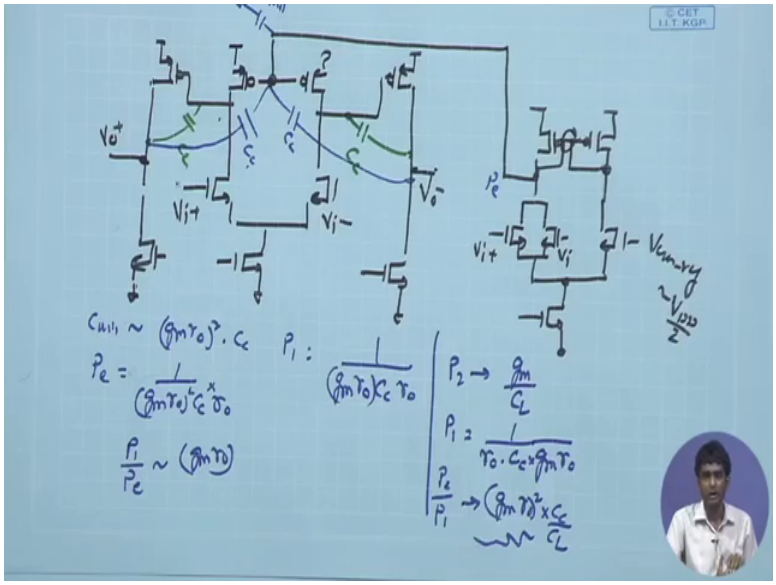

So, let us revisit that case and try to see try to address couple of other queries related to single loop feedback particularly one of them was interesting and it has got to do with joint compensation of common mode and differential. So, here once again we are assuming that the output common mode is taken from the final output stage.

So, if this is your V i plus and V i minus I have the V o plus and V o minus and my error amplifier is going to the take the V i plus V i minus V cm ref and this is going to be close to V DD by 2, because this is the output common mode I would like the output common mode to be V DD by 2 and then you have and we had reverts the polarity. if you remember just to satisfy negative feedback I have to take the output over here because if

the common mode over here goes up. That means, the signal over here will be going down and that will be bringing the PMOS gate voltage down that will make this up and as a result this will again be brought down. So, I would have the reverse polarity for the error amplifier.

So, this is what we discussed and we also suggested that let us get rid of the current mirror load and have a diode connected load disconnect this node of course, you have to for the diode connected load you have to disconnect this otherwise you are shorting both the outputs. So, you have to disconnect this sender connection and make both of them diode connected so that the gain of this stage is given by gm 1 upon gm 2 and as a result you are having overall gain of the common mode feedback loop given by gm ro, gm ro of the 2 stages this is going to give you unity. And there also we discussed that the in this particular case the best place to pull the compensating capacitor would be this only because this is a high impedance node this is the high impedance node and the gain from this point at this point is also large gm ro as a result you can get a sufficiently large miller multiplied capacitor over here.

Whereas this node we have converted into a low impedance node and as a result if you put a capacitor over here it is not going to you any advantage, significant advantage because the impedance at this node is low and therefore, the pole over here will be at relatively higher frequency. This, it will be difficult or infeasible to make this the dominant pole if we are choosing to put a diode connected load for both the transistors over here.

So, this for the natural choice we arrived at and we concluded that this C c is also good to compensate the differential loop. So, both the sides we are putting the same C c it is also going to compensate the differential loop and both the bandwidths for the differential loop as well as common mode loop are going to be governed by the C c only and therefore, we do not have the freedom to optimize both of them separately. That is what we discussed last time and therefore, we explore the alternatives where we can have the 2 isolate loops 2 different loop and then we just now discuss a transistor level mid based implementation of the both loops. And the stability considerations looking at the conflict between the 2 loops and making sure that the stability analysis of one of them is not influenced by the other, this is an important conclusion that we just arrived at.

Now, here another important question was that can we you know go for a compensation cap between the output of the error amplifier and the second stage and in that case can we go for a current mirror loop. So, if I stick to current mirror load; that means, this stage you are going to have a large gain of gm ro and then put a cap between these 2 points for the composition of the common mode loop this is what is going to be the pros and cons whether it is a good scheme whether it is going to give us appropriate compensation for the overall loop response for the common mode.

So, once again first of all we need to make sure that it is not disrupting my differential operation it is not disturbing my bias point not the bias point, but actually the frequency response for the differential operation. So, once again if I assume that for a differential operation this overall common mode signal is not so strong and the common mode level is not disturbed. So, for the differential signal this is always AC ground for the differential half operation this point is not going to have any signal as a result once again for the output node C c is going to appear as an additional load capacitance. In fact, it is able to mitigate any interaction between the C c and the load or the effective capacitance coming at the first node.

Now, the only way the common modal response and the differential response is going to interact is the effective C c coming at the output node for the differential response we will have to represent this C c at the output node between output node and AC ground because for the differential response this is AC ground. So, that is well and good, let us not really interfere with our differential response.

For the common mode response the advantage we are getting over here is that from this point at this point gain is gm ro square another result the multiplication that you get for the C c will be large and hence the effective capacitance over here can be pretty large. So, the effective capacitance that you get over here C miller if I call it, so C miller will be of the order of gm ro square times the C c which can be significantly larger as compared to gm ro time C c 100 times larger.

And it will advantage, it will give us advantage only if there is an current mirror load if there is a current diode connected load then once again pole at this point pole of error amplifier if I call it P e at this particular point that will still be given by 1 upon gm ro square times C c times the impedance over here for the diode connected case would have

been just 1 upon gm, that would just lead to gm ro square time C c which is going to be similar to what we get over here.

So; however, if I have this current source, current mirror load in that case the impedance over here is large it is close to ro by 2. So, the order of the pole gm ro square times 3 times ro this can be pretty small it can push the pole towards low frequency. So, it can help us in achieving better compensation expectedly. So, at the higher level if I look at it can push the pole at P towards lower frequency, so that because of larger miller multiplication achieved by C c. But the other issue is for the differential operation once again we are going to anyway have this C c the green ones which are coming into picture. If I am compensating the loop with C c between the output of the first stage and the second stage the effect is that a dominant pole over here gets pushed down towards lower frequency at the same times the second pole over here puts gets pushed towards higher frequency.

So, that helps in pole slipping and achieving a overall good phase margin, but in this case if I look at the overall common mode loop for the common mode loop this C c is still going to come into picture between the output of the first stage and output of the second stage which is again going to have a miller multiplication and as a result this is also going to be another pole over here which is going to be I can call it P 1 which is going to be given by gm ro times C c and just looking at the order. So, just ignore the factors of half and all that you get because of ro by 2 etcetera, I am just looking in the order. So, gm ro times I can call this you know just assume that these 2 C c is also close. So, gm ro times C c times ro, you are going to get another pole P 1 over here. And if I look at the ratios of the P e and P 1 in the common mode loop we are going to get a ratio of gm ro.

So, if I look at the ratio of the higher pole P 1 upon P under this scenario it is going to give you gm ro which is not sufficient for getting up at 5 degree phase margin right. In order to get a 45 degree phase margin as we have seen the ratio should be equal to gm ro square, the overall open loop gain of the amplifier gm ro square times the first pole should be equal to the second pole or the dominant the dominant pole times the open loop gain of the amplifier should be the second pole. So, that is going to give me 45 degree phase margin.

And how is it ensured if I use C c over here in that case we have seen that the impedance at the second node at output node becomes approximately 1 upon gm of that stage another result the P 2 that you get for the 2 loop 2 stage compensation this is the P 2 that you get is close to gm upon the overall C L that you have at this node. And the P 1 that you get is ro times the composition capacitor miller multiplied composition capacitor. So, C c times gm ro. So, this is the order of the 2 poles that I get when I am using miller compensation between the output of the between the input of the second stage and output of the second stage.

And here I can see that the ratio of P 2 upon P 1 is going to be given by gm ro square times C c upon C L if I assume that these 2 are close together I can say that the order of magnitude of P 2 1 P 1 is gm ro square which is good for or sufficient for giving me a 45 degree phase margin. Whereas, if I use a C c over here and use a current mirror load over here what I am seeing is that the ratio of the 2 poles is gm ro which is going to be it is going to be very difficult to achieve 45 degree phase margin over here only way you can do that is you use a C c the blue C c should be much larger if you use that much larger than the C c use for the differential operation then possibly you can achieve that. And in that case you can also possibly go for ro over here which is much larger than the ro of the first stage of the differential amplifier, in that way possibly you can still try to achieve the C miller over here which is much larger than the miller multiplication of C c for the differential operation.

So, there are 2 constraint that will come into picture that you need to use a large I call let me call this C c 1 just to distinguish or C c star you will have to use large C c star, so that this node becomes dominant and the pole contributed by the second one is still much lower. So, I would like to ensure this ratio P 1 upon P e to be gm ro square. So, this means that the ratio of C c and c star and c must be very large or in other words C c star times the ro of this stage divided by the miller multiplied light capacitance of C c times ro of this stage should be pretty large. So, it has of course, you know tradeoffs with area. So, you will have to put a lot of area to obtain an overall 45 degree phase margin for this scheme.

Advantage will be that yes you can compensate the 2 loops in a very different fashion you can have the common mode loop with much lower bandwidth as compared to the differential loop, so you are able to isolate these 2 pretty well, but at the same time you

are having to pay a heavy price in terms of much larger C c star required or you may have to go for a larger ro over here. And then once again if you look at the loop gain in order to get advantage of this measurement application the loop gain over here should be gm ro cube because this has to be current mirror load then only you will get a large impedance over here and any advantage of the C c star. So, in that case the loop gain becomes gm ro cube and that can further interfere with the stability it can make the compensation more challenging.

So, this choice it may have negative impact on the overall design for the 2 stage op amp. So, this is another issue that we should keep in mind you can try it out you can in the simulation you can try it out, that if you are trying to apply this scheme and putting a C c star between the output of the error amplifier and the output of the op amp whether you are able to isolate the 2 loops properly and you are able to have the compensation for the common mode feedback achieving enough space margin, you will notice that you will either require to make the ro of this stage pretty large or you will like to make the C c star pretty large as compared to C c. So, area trade off and also stability becomes more challenging.

So, while you are trying to solve or isolate the common mode compensation from the differential conversation with the help of this hoping to have a better conversation for the common mode we can see that the in the overall picture you can end up messing up the stability of the common mode. So, this is another option that can come to mind if you look at where to put the capacitor for the differential and the common mode. So, the common mode we can say that hopefully we can take advantage of this one, but we are seeing some issues this point is clear.

So, in one of the assignments we can ask you to you know you C c star for compensating the common mode feedback loop and see; what is the value of C c star required to achieve common mode stability while having a C c for differential stability as well. So, in presence of C c how do you use C c star how do you find out there are write value of C c star for getting the stability for the common mode loop.

So, that also has to be taken care of. So, if you have any question regarding this how to you know what are the concepts involved and why we are probably not going with this connection C c star, it should be clear enough. Let us we proceed towards our next topic.

So, overall stability analysis having these three loops together it is a good exercise. So, in general if you are going for more complicated circuits, maybe filters they are also similar concept apply you may have multiple loops and you may have to take care of the stability of those loops. Likewise we may go for switch capacitor circuits or more complicated feedback system sigma delta modulators for ADCs and so on.

There you have similar cases we have multiple loops we are meaning to take care of stability of each of those loops. So, here we are dealing with a front end amplifier only and trying to see the stability considerations in order to make the DC point stable enough and at the same time make the differential response stable.

So, anybody by simulation exercises have been recommended so far they are very much aligned with the discussions we had for the single loop common mode feedback as well as now we have done regional discussion on the do a loop common mode feedback. So, there is a good combination the DC biasing point also you should be aware of the you know kind of amplifiers to use whenever you are requiring feedback kind of topology to use whether you use a PMOS input device, NMOS input device, what kind of you know DC biasing to get for references etcetera and then when you are looking at multiple loops how to look at their interaction whether the composition is 1 loop is interfering with the composition of the other loop, whether the composition of common mode feedback is interfering with the you know differential compensation. So, those things are important to be understood.

So, that you can appreciate what is going on the simulation and you can in fact check those effects like if you are for example, the interference of the common mode feedback you can check whether you know we are looking at the stability of the differential loop sorry the first common mode loop if you are deactivating the second common loop what happens.

So, there are nice examples it will help you understand the overall you know interaction between these loops. Likewise this is also a nice example where rather than putting this C c for the compensation I am allowing this to be high impedance I am allowing this to be large gain gm ro by putting a current mirror load and then I am putting a C c star and then trying to see whether this scheme at all helps me in getting compensation what are

the you know pros and cons. So, all these analysis we are trying to do a give you a better idea of the design choices that we are making.

So, even if it is not a good choice in some condition in some other conditions it may become a good choice where you are possibly area constraint is smaller and you want to have common mode having much lesser current. So, that the gain of this stage is large and you are having a large ro anyway. So, in those cases you may end up using it, so you if you are simulating it and trying to see; what is the disadvantage you should be at least aware of this trade off.

So, in the simulation exercises you should apart from following the step that has been suggested you should you have to go that one step further and try to think about the problem at hand you look more deeply whether it is just DC by C in whether its frequency response whether it is noise analysis. So, another exercise on noise analysis also has been suggested where you have to size the transistor appropriately. So, that the 1 upon f noise corner is pushed towards lower frequency and then you have to make sure that the bandwidth of the differential amplifier for the differential operation along with the C c compensation is sufficiently higher than the 1 upon f corner frequency. So, that is another interesting example you can look at.

So, just designing this front end amplifier is having so many tradeoffs, so right. So, far we have not given your transistor level design example where you can at least estimate the values of the C c and the transistor size is W by L etcetera given higher level specs. So, here I have just shown you so far the steps for analysis that for noise analysis this is the step this is the sizing direction through which you can reduce the noise, this is the ways you can compensate the differential loop and common mode loop, but they can we need to take another example where given these specs at higher level that we have arrived for our front end amplifier how to arrive at these values of C c, C c star or other sizes of these transistors.

So, calculations can give you a starting point and in general from that starting point you can do the simulations and you can tune the transistor dimensions or the component values in a right direction to approach the right specs. So, in general for calculations we will be using second order model which is not very accurate of course, it just gives you a starting point that if you have estimates of the device parameters or you have the values

of the device parameters given from the technology like the k n, k p of the MOSFET, the noise parameters of the MOSFET, the lambda value of the MOSFET, if you have these parameters given. Or even if you can estimate these parameters like in a second order model we use just lambda V ds and that lambda is not explicitly mentioned in the higher order models it depends on many other parameters.

So, in order to extract the parameters that you use for second order calculation you can do a DC sweep on your MOSFET and extract what is the effective lambda. So, ultimately you are using long channel lengths right. So, MOSFETs in the analog design you will be using long channel than 1 micrometer is not really that if you are using 180 nanometer channel then the devices will be here a minimum channel length. We are using pretty large channel lengths for example, for noise we consider this to be having much lower channel length. So, that you can have a input referred noise small or 1 upon f noise corners can be pushed towards lower frequency.

So, that imposed us using long channel lengths for this 1 maybe even 10 micrometer that is pretty you know common even for 180 nanometer devices you may be using a lot channel then for these guys which are probably 10 micrometer, 20 micrometer that is not uncommon, likewise for the input devices you are probably using at least few micrometer. So, that the gain is sufficient. So, the devices that you are using are relatively long channel although you are going for steel technology. Steel technology may give you advantages in terms of you know I's, in terms of in terms of the ft of the devices , but in order to maintain overall integrity of the analogue signal you have to get a large better ro. Or in order to get a good input referred noise, good stability and compensation. We are seeing that ultimately we had forced to use longer channel lengths for these devices and therefore, the second order model is good enough for most of the analysis or most of the health calculation you will be doing to arrive at the required sizes and for that you do not have for this.

For example if you are using a PTM 180 nanometer models in your LT spice simulation or even some TSMC or UMC model in your Kainene simulation. They are using much more higher level models, but from the DC analysis for this device dimension you can calculate you can estimate what is your gm, what is your ro, what is your k n, k p, what is your lambda and based on that you can do some handle collation and estimate what is the W by L etcetera required for meeting certain specs.

There are some other specs also that we have discussed in earlier classes, like the input swing, input common mode range, output common mode range, combined together with other specs that we have discussed - why is bandwidth stability your, there are some others like slew rate etcetera that will be coming into picture, common mode rejection ratio all these combined together so many parameters combined together will be leading us to some initial values of W by L and the C c their composition capacitor other components etcetera required.

So, we will take one example where whatever analysis we have done for this different different properties noise, bandwidths, stability, input swing, common mode range, then we combined together giving us some starting point for the device domination and the component values with which we can start the design. And then based on the simulation results you can fine tune the design in the right direction to get closer and closer to the spec or get better and better in terms of optimization of various literatures like power consumption noise and bandwidth etcetera resolution etcetera.

Student: (Refer Time: 26:05) output (Refer Time: 26:07) first stage (Refer Time: 26:09) V o plus V o minus how was fixing the output (Refer Time: 26:13) first stage (Refer Time: 26:15).

(Refer Time: 26:16) this is the ultimately the output common mode is provided over here input of this error amplifier in this case is V o plus V o minus.

Student: (Refer Time: 26:25).

That is assume that it is you know fixed with the help of the voltage over here. So, the error amplifier output will provide a certain voltage over here which will lead to a required voltage over here to get a desired voltage at the output. That is what happens in the single loop.

So, we are not directly enforcing certain voltage over here in the case dual loop we are enforcing certain voltage over here which is equal to the V gp of MOSFET and we discuss; what is logic behind that. But in this case we do not we are not controlling this directly we are allowing the single loop to establish a desired voltage over here which is required to establish our desired common mode over here.

So, the common mode over here is going up, I would like this voltage to be going up as well, so that it goes down. So, that is it that would that would require that this voltage should be going down. So, that would require that error amplifier should be going down so that this is going down and as a result this is going up as a result this goes down. So, this is controlled by the common mode feedback. And there one of the other issue is that you do not have a very fine control over this, this can end up being too low also or too high also and therefore the transistor over here can end up in triode more easily.

Whereas, when you are defining this at a desired point say equal to V gp then it is much more ensured or you are having appropriate DC point over here. So, that is another advantage of using dual loops you have a well defined voltage over here which is you are setting equal to desired value. But when you are looking at only the output and allowing the feedback to set the value over here this is only dependent upon the column mode feedback it is it can be it can go low or high depending upon the loop response and then it can the first stage can end up being in trouble.

We will resume our discussion on Cascode.