Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture - 30
Dual Loop CMFB Design (Contd.)

Welcome back.

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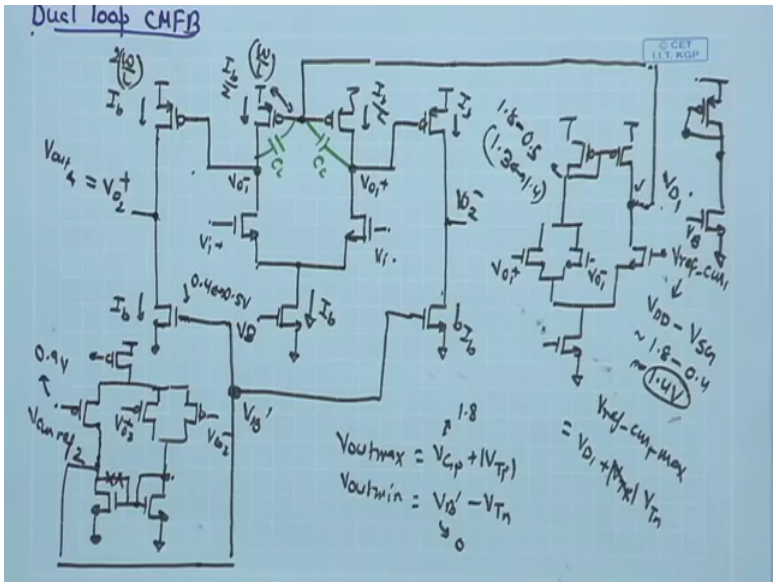

Let us resume with our discussion and before that I can once again check we have any questions.

Student: Sir, (Refer Time: 00:25) V out may be (Refer Time: 00:27).

V out min.

Student: (Refer Time: 00:30).

Now, what I am saying is V out min the minimum value it can acquire is close to 0, total.

Student: Sir, in the (Refer Time: 00:40).

So, this is I would say.

Student: (Refer Time: 00:42).

The.

Student: (Refer Time: 00:43) 0.4 to 0.5.

Sorry.

Student: Sir in the circuit they we are written it (Refer Time: 00:48).

No, So the gate voltage V b.

Student: (Refer Time: 00:54) yes.

So, (Refer Time: 00:55) that what is the minimum voltage you can have at the output that is V g of this minus V t V t is also close to 0.4 0.5 volt. So, you can go all the way close to 0.

So, why I have written V g equal to 0.4 0.5 because V t is close to 0.35 or 0.4 therefore, if you are assuming that the current is small the V gs will be close to V t a little bit higher than V t and as a result the gate voltage is going to be close to this you know 0.4 volt. Another result the minimum output voltage you can have is there is a V g minus V t which is close to 0 or you know few tens of milli volts.

Any other questions before we proceed. So, this DC biasing conditions for the common mode feedback is important how we are (Refer Time: 01:39) determining the amplifier topology the reference points, reference bias is crucial.

So, now let us talk a little bit about the compensation, we have already discussed the concepts of compensation for the single loop as well as common mode the dual loop common mode feedback, let us address some of the questions that we had asked so the design examples a little bit more clear.

So, you have the first loop given by the error amplifier over here and the first stage differential amplifier and what we suggested is that in order to compensate that you can use a C c between the gate of this PMOS and the V o plus or V o 1 plus and minus. And in the common mode half circuit the way it appears is, it appear between the input and output of this common source page in the equivalent common mode half circuit. In the equivalent common mode half circuit remember we tie these 2 drains together gates together. So, this becomes a common source amplifier with input as the PMOS device

and the drain voltages as the output signal and the C c also appear between the input and the output of this common source stage. And therefore, at this point you get a Miller multiplied capacitance and that can that appears over here and this is going to push the capacitance or push the pole over here at the output of the error amplifier to low frequency.

And likewise if we look at the other loop, for the other loop once again we have the input coming from the output of the second stage. So, output V o plus V o 2 plus V o 2 minus are coming at this split pair and the output is going to the NMOS gate. Now if I look at only the second loop and apply a open loop analysis there I am assuming that the common mode feedback of the first loop is operating well and it is giving you a stable DC point over here and hence a stable DC point over here.

So, these 2 will become AC ground and I can forget about the first stage and only look at the second stage along with the error amplifier which is scattering to the second stage. So, in that condition the assumption is that the first stage is completely stable you do not have to worry about it this therefore, becomes DC bias and in the overall analysis I can put this at AC ground therefore, the second stage PMOS becomes the active load and NMOS becomes input device for the common source amplifier.

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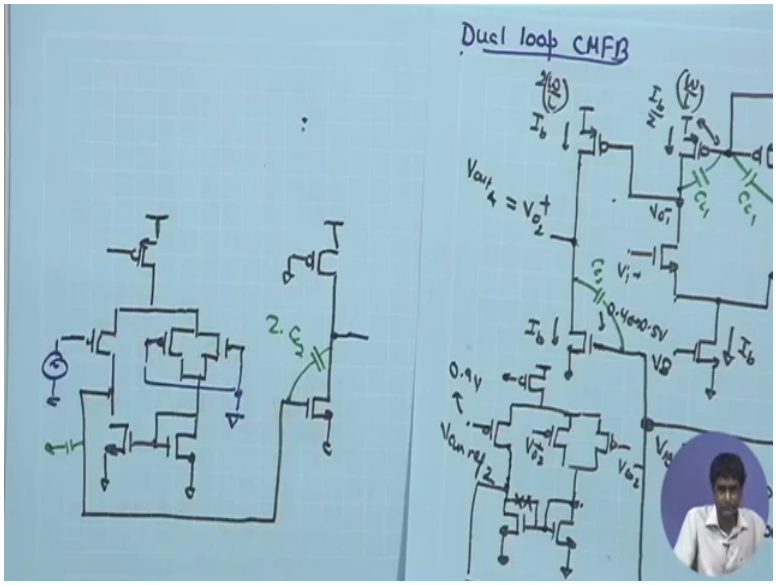

And therefore, if I just you know first it is the sake of completeness if I draw this, I have my original the error amplifier that the way we have just drawn.

This is going to the NMOS stage and for the common mode operation once again we can tie these two together, these two nodes will be tied together therefore, these two PMOS an involve becomes overlapped and we have an overall common source amplifier with NMOS as an input device and PMOS as load device. The gate voltage of these 2 PMOS is going to be AC ground because they are coming from the previous stage the first stage and that is the fixed DC bias. So, therefore, the gate voltages of this become AC ground and our output is taken at this point which is you know coming back through the input.

So, in the common mode once again we can tie these 2 transistors together and club them into a single transistor and their input is basically coming from the output of the common source stage. So, while opening the loop once again I can apply a DC potential over here I have set it to AC ground and apply a test voltage over here and look at the final signal over here. So, this is what we have done earlier for the first stage. And in this case again if you want to compensate this loop we will be looking at placing a capacitor between the output of the first stage and output of the second stage.

Student: Sir.

So, that is what we do in Miller compensation. So, again you can put a C c 2 let me call the previous stage 1 C c 1 and this is C c 2. So, we are going to put another composition between the output of the error amplifier and output of the second stage. So, the differential loop if I draw it in the actual circuit you are going to have a capacitor between the output of the error amplifier and the output of the 2 stages and just to be accurate if I am combining these 2 capacitors in parallel for the common mode half circuit C c 2 over here will combine to give you 2 C c 2. So, actually this should be 2 C c 2 that is just to keep the numbers correct.

So, but structurally this is how it is going to appear in the differential circuit it is going to appear between the output of the error amplifier of the second stage CMFB and the output of the second stage in our overall amplifier. And as a result once again it is going to compensate the pole of the error amplifier it is going to result in a large Miller capacitance at this point which is going to push the pole over here at this high impedance node towards low frequency.

This is the overall compensation scheme is same as what we have discussed for the differential amplifier based on Miller compensation where the lower pole is pushed

towards lower frequency because of this large Miller multiplication and the second pole is pushed towards higher frequency because of the impedance of the effective impedance of the second stage dropping at higher frequency because of this C c. So, that is what happens and we have seen; what is the effect of that in overall compensation and stability.

Apart from this of course, we have seen for the differential operation once again I also need to make sure that there is a compensation capacitor between the output of the first stage and output of the second stage. So, that is going to be there for the compensation of differential response. So, if I look at the C c for the differential response it appears between the output of the first stage and the second stage that is going to push the pole at the output of the first stage for the differential response to low frequency that is the purpose of C c. And however, we also need to make sense of this entire thing that in presence of C c my overall loop response for the common mode for the first common mode as well as second common mode is not getting disturbed it is same as what we expect.

So, just for a check here if we look at the first loop in presence of C c what is the impact on the first loop or for the common mode feedback. Likewise for the differential compensation when we are looking at the differential response and counting the effect of C c what is the effect of the other C c value C c 1 and C c 2 on the differential response that also we need to be aware of. So, that while designing we can make sure that the C c 1 values and C c values are chosen such that the differential response the target differential response for the bandwidth is also met and the common mode response is also met

Now, if we look at the first loop of the common mode feedback is the C c over here going to significantly affect the first loop common mode response.

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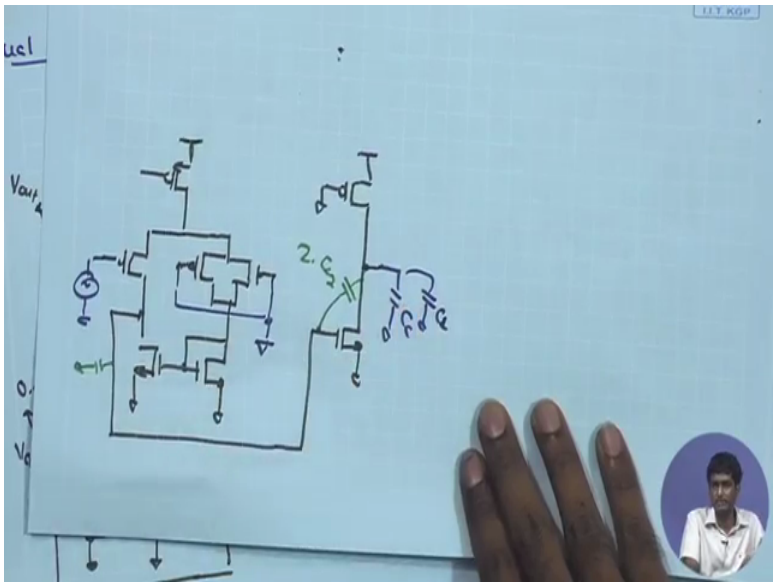

So, if I look at the half circuit of the first stage for the common mode response, let me draw the half circuit of the first stage only. Input let me number this is your M 1, M 2, 3 4 and you know 5 6 7 8.

So, now I am going to combine this 1 and 2, this is 1 plus 2 and this is 3 plus 4 and you have the this is your M 5 I guess I can call it M 9. So, let it be 9 and then I have my error amplifier I can just denote it by symbol and the reference V cm ref and this is how I have it. And then I have the compensation capacitor once up I have open this loop I had basically I can apply the input over here also and I had the capacitor between this input in the output. And also I have the second stage connected. So, after this in the differential response as well as in the common mode response I have second stage also. So, if I draw the common mode half circuit for the second stage I can once again club these transistors M 8 and M 5. So, on both these sides I can join M 8 and M 5 and M 7 and M 6. So, I can call it say 8 plus 5 and here I can call it 6 plus 7. So, this is the second stage.

And I do have the C c appearing between the first stage and the second stage. So, the C c for the differential loop compensation I have between the output of the first stage and the second stage and this one, the first one that I have drawn is C c 1 which is for the composition of the first common mode feedback loop.

Now, here we said that C c 1 is going to have a Miller multiplication and therefore, at this point at the output node you can have an overall multiplied Miller capacitance. So,

for example, if I open the loop over here as we did in the earlier analysis other than this point. So, in this analysis we can say that the C c 1 is going to lead to a Miller multiplication over here and therefore, this output of the error amplifier gives you a dominant pole and so this is this pole is going to be pushed towards lower frequency and this is this stage is going to act like the second stage of my 2 stage op amp just like we have unlike the 2 stage op amp where we put a compensation capacitor between the first stage output and second stage output.

So, this is basically acting like the C c between the first stage output in the second stage and this is giving you a Miller capacitance over here. What about C c. So, if I am putting a common mode signal, after making this if I am putting a common mode signal over here and it leads to some signal over here and you are also having another signal over here. So, is the C c going to play any role in this loop?

If I assume that the second stage is controlled by a separate common mode feedback loop which is stable; that means, if there is a common mode signal coming over here the second stage will be able to track it and it will make sure that the common mode signal over here has not changed. It will make sure that it is you know remaining constant equal to the common mode reference value which is provided for the second stage. So, this remains equal to V cm ref 2 because this is being guided dictated by the second common mode feedback loop.

So, by I am analyzing the first common mode feedback loop and I can assume safely that this point is going to remain constant at V cm ref 2. If it was not constant then definitely we would have the C c coming between the output of the first stage and the second stage and as a result this would also receive Miller modification the C c times the gain of this stage. As a result not only this point, but the output of the second stage in the first common mode feedback loop would also experience large Miller multiplication and hence loading at this point for the common mode response which would mean that you know both the poles have been shifted to low frequency and therefore, the target of having a 45 degree phase margin would not have been met.

But that is not happening because we are assuming that the output common mode of the second stage is being dictated by the second loop and it is fixed to the V cm ref therefore,

even if you change a signal over here this is not having any fluctuation because this is this is being dictated by the common mode feedback loop of the second stage.

So, as a result the C c will not experience any multiplication. C c would experience multiplication for the common mode only if any excursion in this signal would produce a much larger excursion over here then only the Miller multiplication comes into effect because a small change in voltage over here produced as an overall terminal voltage across the capacitor which is much larger and for that you need to supply much larger charge on this site.

But that is not happening because even if you put you know there is a small signal excursion over here this is remaining constant therefore, that multiplication factor, but C c is not going to come. So, we can assume that the effective capacitance coming over here it will be just C c because this is remaining constant therefore, DC ground. So, whatever capacitance C c you put for composition of the differential loop it will appear as it is between this point and AC ground.

So, that is not achieving a Miller multiplication which is going to disturb or push back this loop also sorry this pole also towards low frequency. So, I only want that for the common mode feedback with the first loop only C c 1 should be or the pole over here should be pushed to lower frequency not this one. I have expect that this pole should be pushed towards higher frequency because of the overall impedance of this node reducing.

So, you should be able to visualize the combination of this error amplifier and the common mode half circuit of the first stage as a 2 stage op amp which you are compositing with the help of C c 1 and as a result of which it is pushing the pole at the output of the first stage of this effective op amp to low frequency whereas, the second pole over here is getting pushed towards higher frequency because of the impedance of the second stage is dropping at higher frequencies as we have discussed earlier. Remember that impedance looking into this node becomes approximately 1 upon gm of this PMOS transistor and as a result it shift towards higher frequency the pole shift towards higher frequency.

So, this is an important point should be aware of this that C c is not interfering strongly with your common mode feedback of the first loop. Any question related to this

discussion. In fact, you can check this in the simulations what you can do to check this is if you keep if while opening the first common mode feedback loop if you keep the second common mode feedback loop intact keep it operating then you will see that you will be able to ob obtain a good phase margin by the help of the C c.

But if you turn this common mode feedback loop off and just try to biases with a constant DC then this signal is going to have swing because of the applied common mode signal over here both the common both the outputs will have common mode swing. And as a result this C c will also achieve large Miller multiplication and hence this pole will also move down towards low frequency and therefore, it will fight once again with this pole and then your phase margin will not be achieved.

So, you can test this in your simulations also by activating and deactivating the common mode feedback of the second stage while testing the stability of the first stage common mode feedback loop. I remember whenever you are act deactivating a particular loop you have to make sure that the DC bias point at this point is you know close to what you had in the closed loop condition that is something you should make sure, any question.

So, if I likewise look at the second loop. So, if I am looking at the second loop once again the DC point over here is being determined by the first stage and we are assuming that this DC potential over here is fixed relatively and that is dictated by the first common mode feedback loop. So, while analyzing the second common mode feedback loop we assume that these 2 DC points are fixed and hence the gate voltage DC points are fixed and as a result once again the C c for this stage also comes just as it is right through from this point this is seen as an AC ground.

So, fine analyzing the second loop common mode feedback and taking the effect of C c 2, the C c for the differential operation also comes between this point and AC ground it is not going to have any multiplication as such of course, it is in the reverse path from this point to this point you do not have gain. So, as such it should you should not get confuse about the Miller multiplication of C c 2 anyway, but even then we can see that this point is going to be relatively constant because it is being controlled by the common mode feedback of the first stage.

So, while you are opening this loop and looking at the stability of the first loop while keeping the common mode feedback of the first loop intact and looking at stable to a

second loop there once again the C c over here just appears as it is between the output of the second stage and AC ground.

So, if we recall our common mode half circuit on the second stage this is the second stage of my op amp. So, here you will have C c appearing between this point and ground it will not really have any multiplication as such. So, again C c is not significantly interfering with the compensation of my second common mode feedback loop it is just appearing as an additional load capacitance over here.

And in general the second stage will also have load capacitance because of the next stages. So, when you are applying multiple stage of amplification this will also phase load capacitance because of the next stage. So, anyway you will have a C L over here which is dictated by the input capacitance of the next stage amplifier which can be significantly large few picofarads as we have seen in our examples therefore, this is anyway having a pretty large load capacitance which can be larger than C c significantly larger than C c. So, this is definitely not affected much second loop is not affected much by the C c.

First loop you can say that yes in the first loop at least you are having an additional load capacitance provided by this compensation capacitor for the differential compensation. The second stage not so much because it is already having load capacitance which can be significantly larger as compared to C c, but from that you mean anyway have C L which is much larger or significantly larger than C c. And we can also look at the reverse picture that whether the differential operation differential mode operation is affected by the C c 1 C c 2. So, whether the differential feedback sorry the differential compensation is having an interference because of the capacitance that you have put for the common mode feedback.

So, once again for that I will look at the input signal applied over here and I will be looking at the output signal V o 2 plus and minus I can use the capacitor feedback and look at the voltage division coming out of that also as we have discussed in order to look at the A beta you need to look at the capacitance division also. So, from here you will be connecting those 2 capacitors and tap tapping the centre point and that will give you the A beta factor that is for the loop gain.

And then we can check the overall differential half circuit and for the differential half circuit if I assume that the input signal is anyway differential and the common mode gain of the circuit is poor. So, at these points you will have effectively differential signal coming even if the input signal that is acquired for the sensor it is having asymmetry right.

So, if you remember our discussion the 2 electrodes that are coming they are taking the signal in the vicinity of a certain area of the brain and they are kind of close together. So, they are not acquiring exactly same signal they are signals can be relatively different and you are trying to process the difference between those 2 signals. So, at least at the first stage if I see they are the input signals are not fully differential, but even then if I assume that the common mode rejection ratio is good the common mode signal coming over here will be much smaller as compared to the differential signal. So, the signal over here is fully differential and for the differential operation the signal that you get over here is close to 0.

Because if these 2 signals are differential the signal over here will be summing up to 0 as a result this C c 1 and C c 2 will anyway appear between this point and AC ground sorry; the C c 1 that 2 C c ones over here will appear between these two point and AC ground because we are assuming that this point is constant or stable because common mode signal over here is not sufficiently large even if there is some minute common mode signal it is not sufficiently large that it disturbs this point significantly. Because if there is a large common mode signal over here present over here then of course, the common mode loop will come into action and will try to stabilize the output common mode level over here to the same value, another result you may get some signal coming at this point. But if I assume that as in general the common mode signal is going to be very small

This is going to be more or less constant and hence AC ground therefore, C c 1 C c both the C c ones appear as it is. So, for the differential half operation for the differential half circuit also while doing the frequency response you will have to treat the C c 1 as load capacitance or additional load capacitance coming at the output of the first stage.

Likewise if I look at the C c 2 over here they are also following the same argument that overall differential signal over here is large, but as a result of this the common mode signal over here is not going to be very significant because if the signals over here are

differential and common mode at the input is not changing significantly then the output point output DC point bias point provided by the second common mode feedback amplifier is also going to be relatively constant and as a result this is going to appear more or less as a DC bias point and hence an AC ground for the differential operation as the result the C c 2 also appears as it is between the output and AC ground

So, it is basically can be clubbed with the load capacitance that you have for the differential operation and as I said the load capacitance can be significantly larger than the C c 2 that you get. So, for the differential response once again the C c 2 are going to appear between the output point and AC ground as it is without Miller multiplication and they can be clubbed with the load capacitance.

So, once again they are not interfering so much with the frequency response of the differential operation. Only thing is that when you are compensating the differential response with C c 2 sorry, the C c over here you have an effective C c 1 also coming over here and intentionally if you try to make the bandwidth of the common mode loop small by putting a large C c 1 then you have to make sure that the C c that you are putting over here is taking into account the C c 1 that comes over here for the differential operation.

As I said in general you may like to keep the common mode response or the common mode bandwidth low it is not required to be high because it is just catering to DC bias unless the signal is supposed to have a very you know common mode signal which is sufficiently strong. So, unless that happens I would like to keep the common mode bandwidth I can afford to keep the common mode bandwidth smaller that can save me some bias current. In some application you may need to keep the bandwidth of the common mode loop also similar to differential case in case you have significant common mode disturbances coming and there is a chance of getting these output common mode for the first and second stage getting disturbed.

So, in that case you may like to track it closely, but in other case says if your supply voltages are very stable and you do not have much of a common mode disturbance coming in from other sources we can afford to make the common mode feedback relatively lower frequency and in that case you may go for larger C c 1 and C c 2. And in that case I have to make sure that the effective C c 1 coming over here for the differential

loop is not really your accounting for that C c 1 while choosing the value of ccs for differential compensation.

Any question before we take a short break. There is another small point related to again another query that was asked for an alternate ways of compensation. So, probably we will be looking into that briefly. So, before that any issues related to whatever we have discussed over here regarding the compensation for the differential and the common mode loops, the 2 common mode loops and the differential loop and their interaction.

Student: Sir, in this differential operation (Refer Time: 27:33) load capacitance (Refer Time: 27:33) phase (Refer Time: 27:34) unwanted.

As I said load capacities will lead to an overall effective loading and then you know to calculate the poles at the output you have to basically rely on that load capacitance plus this C c 2 that comes into picture. So, C c 2 as I said is also appearing as effective load capacitance especially if you are trying to make the common mode loop slower it is appearing as an effective load capacitance because this becomes an AC ground for the differential operation.

So, ultimately the choice of C c depends upon the load capacitance the little choice of C c for the differential operation becomes upon depends upon the load capacitance. The composition depends upon the load capacitance because that is determining the output pole output pole of the second stage depends upon gm upon C c gm of the output stage divided by C c therefore, of course, it affects the phase margin, depending upon total effective C L only if you determine the C c.

So, in this case you have to just keep track of the discussion that we had in the last day where we talked about opening the loop in simulations and how to do the bias while keeping the DC points intact at different points. So, for the dual common mode feedback loop also you have to make sure that while you are opening the loop for the DC or the stability analysis for these individual loops and then for the differential loop the DC conditions are made remaining intact. And while you are opening 1 loop say the first common mode loop the other 2 loops are intact or while you are opening the second common mode feedback loop the other differential loop and the first common mode loop is intact. So, those considerations you definitely you should be able to make while doing simulation.

Like while when you are doing differential simulation and trying to assess the stability of differential operation we would like to keep the first the 2 common mode feedback loop intact. So, that they are taking care of the DC biases of the output node and input node we had some special consideration that we discussed that day.

Student: Sir, simulation point of view if we for a phase margin we determined first stage C c 1 then again C c is C c 1 C c 2 after (Refer Time: 29:45).

So, there are 2 different loops. So, C c 1 C c 2 can be pretty close. So, these values are just to stabilize these 2 you know feedback loops and amplifier configuration bias currents are similar, so they can be pretty close. C c can be different because of the bandwidth requirement you can have a different you know pole for the differential operation as compared to the common mode operation.

So, if you are for example, trying to keep the bias current in this error amplifier lower in that case the bandwidth over here will be lower and you can the compensation after compensation you will be getting a lower pole over here. But for the differential operation you may have bandwidth requirement signal coming is much faster you would like to maintainers probably larger bandwidth for the differential case.

So, there that will be the main concern which will be which will let us choose different values of C c cc 1 C c 2. So, C c 2 and C c 1 can be close because these 2 loops are common more feedback loop and there is speed response demanded for a particular application may be closed. C c will be different because the response sort by the differential loop can be faster. For example, if you have to use a compensate the feedback differential feedback considering the capacity of division.

So, as I said last day your differential feedback is having the capacity of division as a result the loop gain is the A 1 A 2 that is gm ro square or the times the beta factor which is small maybe 1 upon 30 or 40. So, that already gives you better stability for the differential loop as compared to the common mode loop where you have the overall loop gain given by gm ro times gm ro that is just maybe 30 40 times larger than the differential loop.

So, compensation for the differential loop can be easier if I consider that beta factor and then the required C c value may also be smaller. So, that can make a bigger difference. In

some cases you want to be aggressive and conservative. So, you will try to compensate the differential loop also for the worst case that because of the parasitic effects at higher frequencies the beta approach is 1, that will be the worst case and therefore, I will consider the loop gain of the differential case also to be gm ro square then the C c value will be large. But you can take that 1 stage that for the differential loop you have beta factor and that is reducing the open loop gain overall the sorry. So, overall loop gain has been (Refer Time: 32:10) reduce by the factor of beta and it (Refer Time: 32:13) you can afford or smaller C c for the differential case.

So, that will allow you to compensate the differential loop separately and the common mode separately. When we used same common mode loop for both the cases then we are relying only on one C c to compensate both and in that case it is basically tied with the larger gain gm ro, square gain that is obtained for the entire loop and that basically leads to over compensation of the differential loop that is what we discussed last thing.

So, let us come back and we can discuss the dual loop I mean a single loop case and try to look at another interesting point it was raised in last discussion and also contrast the pros and cons of the single loop case with the differential dual loop case. We will resume our discussion and try to finish the comparison between these 2. So, and arrive at some conclusions regarding the choice of single loop versus dual loop.