**Analog Circuits and Systems through SPICE Simulation**
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**Lecture - 27**
**DC Biasing For Open Loop Analysis**

Hello and welcome to today's session, where we are going to look into first some of the simulation techniques that will be required for analyzing the feedback scheme that we discussed including the high resistance implementation and the common mode feedback and the differential feedback. So, we have seen that the stability analysis for these circuits is going to play an important role in the overall analysis of the system under consideration and therefore, I am just going to describe briefly the steps to be followed to implement or to do the stability check for the common mode and differential loop.

Let us get started with the overall feedback scheme that we have and look into both the feedbacks common mode and differential and the then look into the stability analysis that we are going to do at stimulation level.

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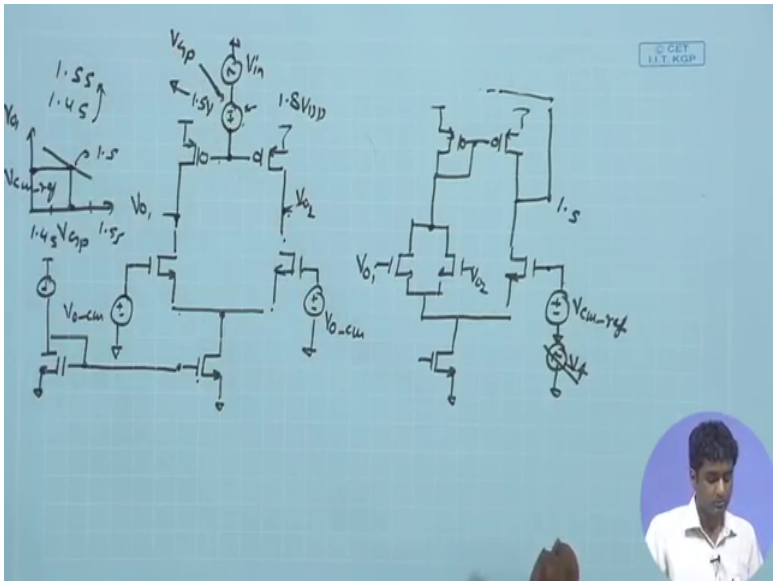

So, theory point of view we have already discussed how to do the simulation how to do the stability analysis, but in order to implement that in simulations and verify our concepts that we have learnt in the theory it will be important to just discuss how we are going to follow these steps in the simulation.

So, let me start with a single stage defame where I am trying to compensate it with the help of a common mode feedback error amplifier. So, let me redraw the topology that we discussed. So, this is our error amplifier and we have discussed the common mode half circuit where we need to open the loop. So, here I am drawing current mirror load configuration for the error amplifier where I have the V o 1 and V o 2 coming at the inputs and you have the reference signal over here and what we discussed was that the output of the error amplifier is fed to the input of the PMOS.

Now, in order to open the loop we can open the loop at several points. Now one option is that we can you know disconnect the output of the error amplifier from this PMOS gate and then we can take this as the input point keep the connection between V o 1 V o 2 and the NMOS as it is. So, I will keep this connected, but I will disconnect this one and then apply the signal over here and observe the final output over here. So, that is one way of opening the loop and doing the stability analysis.

The other option is that as we have discussed in the theory session we can open the loop over here. So, we can disconnect the input of the error amplifier from the 2 outputs and then trace the keep the connection between the output of the error amplifier and the PMOS as it is and then observe the final output coming over here under that condition we said that we will be applying a AC signal over here. And of course, since it is going to be a common mode operation both the outputs will be changing in the same fashion and therefore, that behaves as my final output that is the a beta factor.

So, this signal observing this signal is equivalent to observing the a beta times the input signal. So, there are the 2 ways in which we can do it. The consideration, however, that we should be aware of is that the DC biasing condition of this particular circuit as well as the error amplifier should remain unchanged because remember the small signal parameter that we use in the stability analysis is the gm, the ro etcetera that depends upon the DC bias conditions of these transistors.

And therefore, the small signal parameters gmro should remains constant or same for the open loop as well as closed loop conditions. And that would imply that the DC bias voltages and the currents especially the currents in the MOSFET they should remain almost constant almost same as the closed loop case and to do that if we talk about the first case when we are for example, opening the loop over here. So, in that case my V o 1

and V o 2 is till connected to the input of the error amplifier these 2 are anyway set to AC ground or their respective DC bias point.

So, if I talk about the exact simulation of course, whatever DC bias point was applied at these 2 inputs we can keep it as it is. So, we can and remember when you are using the common mode feedback we had set the output DC point with the help of common mode feedback while for biasing the input we used a resistive divider over here sorry, large feedback resistor over here Rf 1, V o 1, V o 2 to the input devices and that ensure that the input DC point was equal to the output DC point.

While opening the loop also we can do the same analysis we can also keep the same Rf because as long as we are ensuring that the V o 1 V o 2 DC points in the open loop conditions are going to remain same that will also ensure that the input DC point over here are also same. However, if you if you look at the input signal over here that if you are having a overall signal coming over here it will induce some signal at this point also unless you have some a significant input capacitance placed over here for establishing an AC ground.

Therefore in order to ensure that this point is at AC ground either we need to put an capacitor over here along with the Rf or the other option is that you remove the Rf and then apply only ideal DC voltages over here with values equal to the closed loop condition. So, the closed loop condition we know that we had put the common mode DC output voltages over here. So, we can just connect DC voltages over here which was equal to our V o cm under closed loop condition. So, I will put just the same V o cm over here this is anyway coming from the reference current meter branch. So, I do need to talk about this.

So, this is this may be coming from a reference current meter branch and here if I am opening a loop over here for that I also need to make sure that whatever DC point was available with the help of the error amplifier at this point the same is maintained. So, before opening the loop suppose the amplifier give us a voltage of say 1.5 volt DC over here for a 1.8 volt V DD. So, after opening the loop when we are applying a signal over here we have to make sure that I apply a same 1.5 volt DC and on the top of that apply my AC signal V in to check the open loop response because the DC bias condition must be maintained.

So, under closed loop it was giving me 1.5 volt DC and therefore, after disconnecting also I keep the same 1.5 volt DC and that will effectively ensure referee that this V o 2 and V o 1 the DC common mode the this is also remaining more or less close to the previous value. And therefore, in the then the open loop simulation the DC value over here and hence the DC value at the gate of these 2 split transistors they will also remain similar. And of course, here we also need to keep the same V ref I would say V cm ref that we had under the normal closed loop operation and then apply an AC signal on the top of that V test if you call it.

So, the test signal the AC signal sorry, in this case we are you know not applying the test signal over here, but we just need to put it at the required V cm because in this particular case first case I am assuming that the input signal was applied over here. So, you just need to make sure that this is also at the same V c in brief that you had applied. And one point to note is that this is a high impedance node and therefore, even a small change in this DC voltage 1.5 volt can result in a significant change in the DC bias over here. So, because if you look at the input point over here with respect to this a particular DC plus AC combination this is acting like a common source amplifier with input as the PMOS and these are just acting like the load device.

So, if you remember our discussion on the open loop analysis this behaves like an cascode device with the gate as AC ground and therefore, with respect to the signal over here the input pair this is act like a common source amplifiers input pair and whereas, the NMOS transistors over here and the NMOS of the current source acting like the cascode load. Now if we therefore, want to look at the signal over here a small change in the DC level even 1 millivolt of change can produce a large shift in the DC potential over here.

So, remember we are designing this circuit for an overall gain of greater than 10 to the power of 4 the open loop gain of this amplifier such that 2 stages over all can be 10 to the power of 4 or higher and as a result each of these stages the differential stage and after that the common source stage can has a gain of 10 to power of 2 or higher. So, few 100s it can reach 1000 and as a result of few millivolt of shift in this 1.5 can also result in you know significant shift 100s of millivolt shift over here and therefore, it is we prudent to read this values carefully in the simulation also if you look at the DC value you have to put very precise values over here which was same as the value provided by the feedback circuit.

And if you are not getting exact same DC potential over here it is also advisable to sweep this 1.5 volt DC across the mean value. So, you are expecting that is a 1.5 volt DC putting over here will give me the right DC potential over here which was under the a closed loop condition. But if it is not coming exactly and you want to be more precise about the DC bias point and make sure that in the open loop condition it is DC bias is remaining same or very close to the previous one, you can sweep this DC potential. So, in the simulation analysis you have the option of DC sweep. So, you can select this DC potential and sweep it across 1.5 volt.

So, maybe you know 1.5 you can go from 1.55 to 1.45 and within this range you can take large number of steps say you know a few tens of steps and see the overall characteristics of the DC point over here. So, if for example, if you do such a DC sweep, if I call this you know V gp if you see this V gp from the lower value 1.45 and 1.55. If the value is you know going up the output voltage will be going down and whatever point you get the output potential same as the previous value that is your V cm ref you can take you can pick up that V gp and put it over here right.

So, you can feed the V gp I am calling this the V gp the DC potential you can sweep this little bit across the expected value of 1.5 and at whatever point you get the output DC this is your the y axis I am plotting the V o 1 or 2. So, at whatever point the V o 1 reaches V cm ref very close to that we can pick up that value that will be much more precise. So, you will make sure that the output DC point over here is very close to the required DC point under closed loop condition and also make sure that the DC point over here for these two V o 1 V o 2 that you are having that is also close to the close loop condition and the gms exit are very well matched.

So, this is the condition you should just check for a while opening the loop and once you have opened the loop then of course, you can apply the AC signal over here and then look at the final output coming at this point.

So, here I have just you know trying to complete the analysis from simulation point of view. So, in the real simulation how you will be doing the analysis to obtain the overall phase margin and likewise if you are looking at you know compensation so that is for the compensation part once again you are either going to look into the capacitances place between the output over here and this point or we can look at the capacitance place

between the output node over here and the output here. And if we look at the overall capacitance coming between suppose you are putting the capacitance between this point and this point then of course, the main amplifier also is having the mirror effect and the overall capacitance over here will be multiplied whereas, for the other node when you are you know putting the capacitance that effect is not coming into picture.

So, if you have a cap which is connected between say in the compensation scheme that in your using a cap between the outputs over here and the output at this point. So, that can lead to mirror multiplication between the caps, between you know the input stage and the output over here and, but that is however, going to load the main amplifier also which is not very advisable. However, if I am looking at the mirror effect between this point and this point the after opening the loop we can see that the capacitance will not be coming in the you know loop simulation or you know the open loop simulation because that is the loop over here has already been broken. So, in order to load this particular point with the capacitor it will be advisable to put a measure multiplied capacitance value over here. So, that is you know one possible solution.

So, let me talk about the other scheme or other alternatives that we also need to see, so some of you who have tried the other way in which the loop can be opened say at this point. So, once again similar considerations, if I am opening the loop at the input point. So, there also we just need to make sure that the overall DC conditions is maintained.

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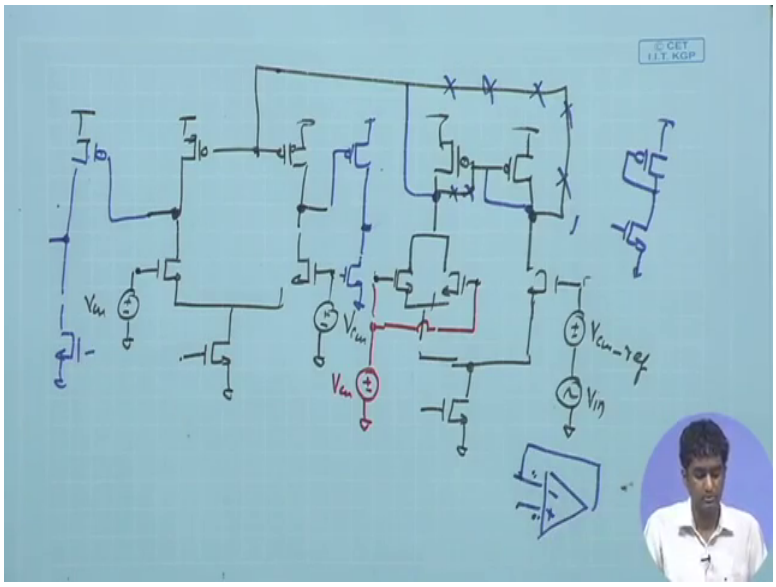

So, under this condition we know that once again the input point anyway they are supposed to be at the common mode DC level. So, I will just put the same V cm over here the DC level expected and this is the same DC point and the differential pair or the split pair that you have we are breaking the loop over here and therefore, these 2 DC point these 2 gate voltages need to be connected to the common DC point. So, I will connect these 2 with the same DC level that I was expecting V cm and then at the other input once again I anyway I have the V cm ref applied which is equal to the expected V cm.

So, this is the DC potential and then you apply the v in for testing over here and then complete the loop. So, in this case once again we have taken care of the DC biasing. So, the input DC potential over here is maintained and we are trying to observe the output voltage over here and as a result we have the overall we have the overall DC conditions maintained all throughout in the main amplifier as well as in the error amplifier

So, this is the condition you need to check while doing the open loop simulation for the common mode feedback we have. Likewise if we do the common mode feedback for the whole a two stage there also you know similar biasing conditions need to be checked and ensured that the overall error amplifier and the two stages are maintaining the same biasing scheme. And suppose you are using the same, you know single loop for the common mode feedback then overall it remains the scheme remains same only thing is after that you will have another two stages added which are the common source stage. And you are basically trying to. So, these are the additional stages which get added and your output you are taking it from these 2 points.

The other thing that you also need to make sure is that you are checking the polarity of this one. So, some of you have pointed out that when you connected the 2 stages in the loop of this particular scheme was not working and that is because you have probably not change the polarity because for the single stage if you look at the you know polarity this is the correct polarity because it is giving us overall negative feedback.

So, you can trace it back and check whenever you have doubt. So, assume that output common volt for just assume that you are just having the single stage in that case you have just trying to trace and figure out that yes this connectivity was correct to do that what did we do you remember a few increase. Assume that the output common mode

voltage has increased because of some reason and as a result this was connected over here and therefore, this common mode voltage going up means this voltage going up and; that means, the PMOS gate voltage going up and PMOS gate voltage going up means the vsd must you know go down and therefore, sorry a vsd must go up as a result the drain voltage must go down and that will again bring my output common mode voltage close to the required value.

So, that was the mechanism of negative feedback we discussed; however, if you are having the other stage inserted then also we need to take care of the polarity in the resulting closed loop. And therefore, now if you see this voltage going up that would mean that these 2 outputs over here will be going down; that means, the input voltage over here will be going down and as a result this will be going up and sorry this will be going down and I do not want this down going voltage to be applied over here. So, rather than that I would like this particular drain voltage to be applied at this point and to do that I will make this the output node and the therefore, I will have to connect this make this they are connected and take the output from here.

So, this will be out and this becomes my new output this will be also out and when I am taking the V o 1 and you know V o 2 from here in that case in order to ensure negative feedback across the loop I have to you know change the polarity of the diode connection output has to be taken from here and then we can once again follow the loop and make sure that yes you have overall negative feedback in the common mode loop. This voltage going up means output of these 2 common sources going down; that means, the input of these 2 p NMOS transistors going down; that means, this voltage going up and that going up means once again it will help in bringing these 2 voltages down.

So, that is supposed to be the case. So, you just take care of the right polarity if you are using the same single loop for the overall common mode feedback. However, if you are using 2 loops like for the first stage or separate loop in a second stage a separate loop then polarity remains same and that is something you should be aware of. And in this case if you are using 2 stages, if you are using 2 stages and they are also ultimately when you open the loop using the second scheme that we discussed you would like to maintain the output common mode at the same point and in that case it may more challenging because the gain from here to here is large and you are applying the signal over here and the you want to make sure that the output DC point over here is close to the common

mode point that you expect. And therefore, the sweeping scheme that I discussed that becomes all the more important because you do not need to be precise you need to precisely locate which point you want to have at the biasing the DC bias. So, that the output DC levels over here obtain for the closed loop operation they are very close to the common mode voltage that was obtained using closed loop.

In the single stage gain you had the gain from the gate of the a PMOS to the output given by gm ro by 2 or gm ro precisely and however, in this case the gain from here to here is further large or gmro square therefore, a little bit of change in the DC potentials here can change the output DC point significantly. Therefore, if you want to ensure that the output DC point should be very close to the a desired value in the closed loop you just whatever DC you are applying at this point for example, you can sweep it a little bit across the ideal you know red value and that will ensure that you are able to find out the right precise value of the DC so that this point it at the required value.

Student: Sir in the error amplifier for the first part where we are (Refer Time: 22:21) to gates we want them to be equal to the output of the common source amplifier right.

Yes.

Student: So, we want the output as the common source amplifier to be close to V cm ref right. So, why are we getting V c and we should (Refer Time: 22:34).

That is V cm ref means V cm is V cm ref that is your expected value. Only thing is that little bit of change you know or if you are not doing it very precisely the output can swing by a large fraction. So, in the feedback loop there is a negative feedback and it will try to adjust with little bit maybe by a few millivolts or a fraction of millivolts. So, that the output is coming close to the desired value where you open the loop that negative feedback or the stabilization effect is removed therefore, the required value over here to achieve the same volt may be slightly different so it may not be exactly same. So, for that you need to just do this sweep in the open loop case. So, that the output point is coming close to the desired value.

In the negative feedback eventually it will not be exactly same. So, it will have some error because remember in the negative feedback what do we assume if the if there is an error amplifier we assume that once you connected a negative feedback these 2 are

exactly same, but that does not happen because if there is a finite gain amplifier or there will be some minute difference between these two, these two inputs and that is the ensured by the negative feedback.

Therefore either you have to read the voltages very carefully in simulators it may not show all the decimal places. So, in that case if you want to get the precise value you are having the negative feedback and you want to get the precise value of the DC potential over here and you need to basically do the sweep as we suggested over here. So, rather than I am choosing the exact V cm ref you need to sweep it a little bit and then find out the exact V gp in this case for example, to get the exact right value of the output voltage.

And likewise in this case and you are opening the loop here you need to maybe sweep this particular DC voltage so that the output potential over here is equal to the required v ref. What I am just trying to point out that if you just simply open the loop it is not necessary that under the open loop if you apply this V cm ref over here and the same V cm over here it is not necessary that you will get the same value V cm over here like you were getting in the closed loop. Why, because in the closed loop condition the amplifier finite gain of the amplifier will ensure some minute difference between you know the effective common mode coming over here and the common mode that you are expecting over here and when you open the loop that is that mechanism is not present.

So, you need to you know make sure by sweeping this value a little bit. So, that the output DC potential over here is equal to the required common mode because remember the gain from this input point into the final output is going to be pretty large gmro cube and as a result a little bit change over here can produce large changes in the output DC potential and therefore, just to ensure that the output DC potential is a close to the V cm ref it is not it does not have to be very exactly close 0.1 millivolt close, but at least you know few millivolt within few millivolt difference should be close. So, that you are getting accurate common mode now accurate open loop analysis.

Student: Sir (Refer Time: 25:42) to avoid the (Refer Time: 25:44).

As we have said the in this case we have a fight between the differential operation and the common mode operation. So, you try to add capacitor between the output of this one and the output of the error amplifier. So, that does have the mirror effect coming over here, but it also has mirror effect coming over here.

So, we discussed how to isolate that you in sort of buffer and then use that, so that will basically introduce mirror effect here strongly. So, that will try to have a large composite effective measurement applied capacitance over here, but you do not want that measurement of like a capacitance over here because in the closed loop if you see that capacitance also comes between this point and this point you are having a signal path from here. So, we discuss that let us have a buffer and then connect the capacitor between you know this point and the buffer output at the first stage. So, that the buffer output is having low impedance even if it there is a mirror effect coming over there it will not affect. So, ultimately it is if you are having a buffer after this for the compensation path of between the buffer output and this point you can put the capacitor. So, that.

Student: (Refer Time: 26:49).

No, that is in case you are using a single loop. So, in the single loop if you are using this entire common mode feedback then I suggested that to keep the loop gain within bound let us have both the PMOS they are connected. So, that the loop gain is within limit gmro square it is not going to gmro cube because in this loop if it goes, again goes to gmro cube all the 3 nodes that you are having in the loop they are having equal or equivalent you know open loop pole values.

So, if I look at the original case where I am having the current mirror load you should be able to distinguish between this 3 terminologies current mirror load means only one side they are connected diode connected load means both side they are connected and current source load like this, this is the current source load where none other connected. So, when I say current mirror load; that means, only one side is diode connected other side is you know not having diode connection.

So, if I use the current mirror load for the common mode feedback for the 2 stages together then the closed loop, the loop gain is pretty large it is gmro cube. And it may lead to more instability therefore, and the other serious issue is that all these three nodes the output of the first stage second stage and the common mode output they are almost having similar magnitude of the pole. So, compensation becomes a little bit more challenging. Therefore, it may be advisable to use diode connected load for the error amplifier.

So, in that case if the error amplifier gains becomes smaller close to 1 because once you do the diode collection on both side means you disconnect this gate and do the diode connection on both side then the (Refer Time: 28:37) of this error amplifier becomes gm 1 gm of the input paired divided by gm on the load pair just like the you know differential half circuit you have a diode connected load. So, if you have both of these diode connected this center connection removed and both of them diode connected; that means, the gain becomes gm 1 upon gm 2 gm of this device divided by gm of this device and almost close to 1 and in that case the loop gain will be of the order of gmro square. So, it will be a little bit easier to compensate and in that case what we have seen is that you can add a composition capacitor right over here as we do it for the differential case.

So, if you add a composition capacitor over here for the overall 2 stages then anyway you are having the overall 1 of the poles in the loop being becoming dominated and the error amplifier in that case is not having dominant pole because you have diode connected both of them as a result the impedance at these 2 points drops it is close to 1 upon gm as a result this is not going to interfere too much with your pole compensation. So, in that case the dominant poles are in the main amplifier only and there is the output of the first stage and output of the second stage and then whatever compensation we discussed for the differential scheme applies here also.

So, there we are trying to compensate the basically implies that we are trying to you know have the similar composition for definition as well as common mode loop also because once you put cap here then it also compensate the differential operation and the same time also compensate with the common mode operation. Then resume with the rest of the discussion.