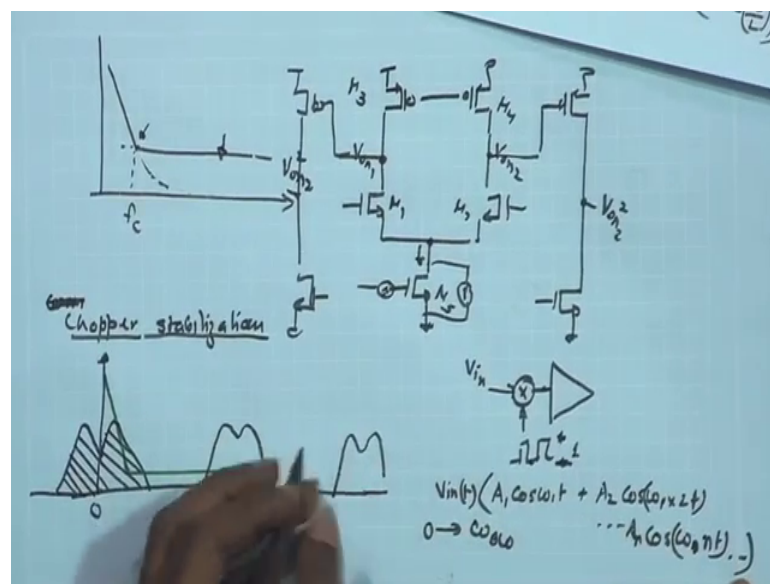


Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture – 26
Chopper Stabilization

Welcome back and let us start with our review over a discussion on noise and we will be looking at the differential amplifier circuit active load.

(Refer Slide Time: 00:23)



That is being used for building our op amp and then we will be looking at some of the sizing issues related to reduction of this corner frequency 1 upon f_c , and also look into some other techniques that can be used to indicate this 1 upon f_c noise, which also involves tradeoffs with some other design matrixes. So, let us look at these topics one by one. So, if we look at the differential amplifier operation, we will be looking at the differential half circuit, and then we can say that ultimately our differential half circuit going to be same as what we have just analyzed active load circuit.

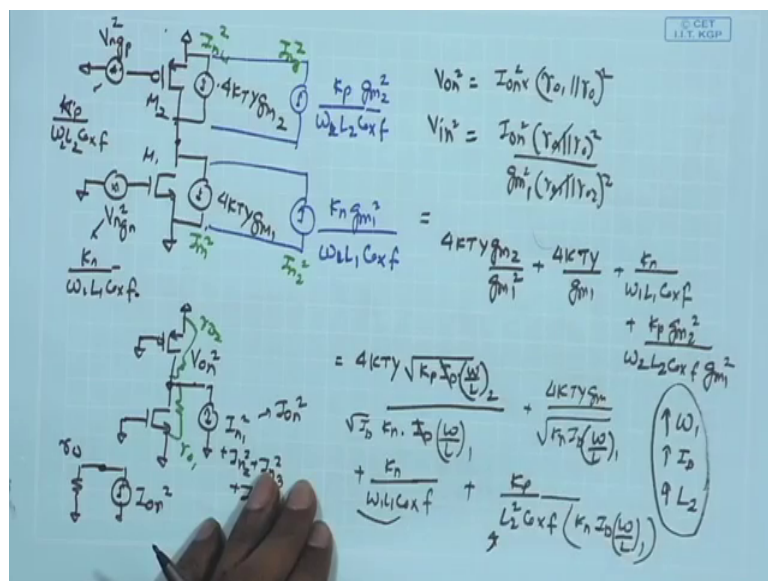
If we however, look at the common mode we have just got to take care of another transistor which is at the tail current source. So, you have M_1 M_2 M_3 M_4 . For the differential case we do not have to worry about the tail current source we said this is a c ground. So, anyway we do not have contribution coming from this one for the common mode also if we look at the 2 paths, you have some equivalent noise voltage and current

because of this transistor, and this is going to result in an overall equivalent noise current going through the drain of this M5. For the common mode therefore, this is the same source which is contributing to the V_{on1} and V_{on2} . So, if I consider effect of only M5 its effect acts appears like a common mode because it is a single source.

So, its effect is getting divided and you are having overall noise current flowing in these 2 branches and coming at the output nodes over here, and these are correlated because they are coming from the same source. So, they you can have an overall noise coming in the common mode operation because of this transistor, and we are not concerned with the common mode signals so much. So, and if overall common node noise which is much my new desk compared to the signal can be relatively less significant as compared to the differential operation where it is not appearing. So, this is just a small point to be noted over here. Now if we look at shape the minimization of f_c , if we revert back to our expression and try to see what it takes to minimize f_c in order to cater to our low frequency signal. Remember we are talking about signal content which is going all the way to 0.5 hertz and we need to pass up 2.5 hertz of signal.

And our higher cutoff frequency for the high pass response source. So, that we designed with the respect with the help of that feedback resistor r_f for input dc biasing, that was also supposed to pass that 0.5 hertz. So, we need to ideally shift f_c the 0.5 hertz if it is rely only on sizing and the once again.

(Refer Slide Time: 03:15)



Referring back to our discussion earlier, if we look at the $1/f$ frequency that will be obtained by the ratio of these 2 terms. So, we just equate these and get the f at which these 2 are equal, and that again mandates much larger L_2 value, that would mandate a large ID value because in this ratio ID will be coming in the denominator term, and that will once again mandate a larger ID value and along with that also larger w by L_1 value.

So, these are three terms we will like to increase ID , w of the input device that is making it larger size and likewise making the channel length of the output device or the load device much larger. These are the three quantity that we figured out in order to push this $1/f$ frequency towards lower and lower values. So, we see the try a trade off with the bias current first of all and in our case when we are having a low power application we are talking about multiple channels, you know each of them having such a dedicated fronted amplifier, bias current is having severe constraint and therefore, we cannot just go on reducing we just cannot go on increasing the bias current, to cater f to $1/f$ noise requirement.

Likewise the other terms if you go on increasing w_1 or the device size L_2 they are going to affect my bandwidth because we are going to increase the device parasitic capacitances and slow down my overall frequency response, and we need to you know cater to up to at least you know hundred or 1 kilohertz of signal. So, being conservative we would like to push the upper cutoff frequency slightly higher than the signal content. So, signal content is a 0.1 to 100 hertz, we would like to upper cutoff frequency to be at least a few 100s of hertz 2 kilohertz and we must need all those constraints while we are sizing these input devices and the channel length of the load device larger.

So, if we just rely on those 2 considerations, we will definitely have conflict with our bandwidth requirements we will also have conflict with our power budget that we are having for the overall amplifier.

So, we need to look into some other techniques through which we can possibly have a better solution for this $1/f$ noise. And before we go there we can also you know once again quickly revisit the second stage, and just conclude that its noise which not so, very limit as compared the first stage therefore, we are focusing more on the first stage noise and without doing noise of an analysis we know that the whatever noise is produced by the second stage I can call it V_{on}^2 square over here ultimately magnitude

point of view there going to be same, because they are symmetric devices. So, the mean square value is supposed to be same and if we want to refer it to the input, it gets divided by the phase first stage gain as a second stage gain. So, V_{on}^2 if you want to find its equivalent input referred noise, we are gets divided by $g_m r_o$ by 2 whole square, as a result its contribution will be much lower as compared to the noise produced by the first stage. So, we are concerned with minimizing the noise contributed by the first stage and we will just make sure that under no condition the second stage noise is degrading too much that will not happen generally because of other design constraints, we are having the w by L and the bias current in the second stage also comparable to the first stage.

So, we can you know try to save some power dissipation by allowing lower bias current in the second stage, because it is not so noise critical. So, because I really take the advantage of the 3 relaxation in achieving some advantage in the second stage, by having more relaxed considered w by L and bias current. So, we are mostly focusing on the first stage for this determination of 1 upon f noise or minimization of the 1 upon f noise through the technique (Refer Time: 07:11) we are going to discuss next. So, technique that is commonly used for mitigating the effect of is 1 upon f noise chopper stabilization where we have an input signal which is which may be lying at very low frequencies.

So, for example, in our case as we have said the content of the signal may be peaking at close to you know few tens of hertz, and it can have content going all the way 2.5 hertz. So, it can be having some content very close to dc also and therefore, if I look at the complex frequency spectrum it will look like this you have the positive and negative frequency component, in the complex frequency domain coming in and. So, this is the overall signal spectrum centered around ω equal to 0 and I under this condition I also have at present the 1 upon f noise which is which can be very sharply overlapping with this even if you are designing it very carefully trying to push 1 upon f noise further and further we said that up to 10 hertz it may be feasible, but beyond that it becomes difficult.

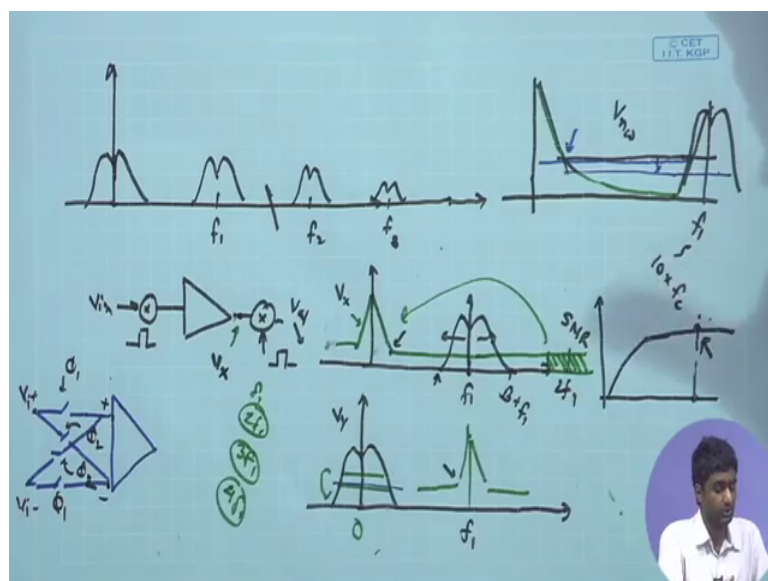
So, definitely we would like to say our signals from this increasing 1 upon f noise which can significantly corrupt or completely destroy our signal content at least those which is closer to lower frequency closer to dc. And to do that the technique uses chopping where we multiply the input signal coming to the amplifier with a higher frequency clock

signal. So, schematically you can represent it as a multiplication operation, where you are having the input signal getting multiplied by plus minus 1 sorry plus minus 1.

And as a result the overall frequency spectrum of the input signal will be getting shifted by the frequency harmonics of the square pulses. So, we know that the square pulse is going to have harmonics at the fundamental frequency of this square, and also the higher harmonics. So, I can represent this as $A_1 \cos \omega_1 t$ plus $A_2 \cos \omega_2 t$ and so on in ωt and so on. So, if we can expand it in the form of its Fourier series and we can look at the coefficients, and when you multiply this entire quantity by the input signal call it V_{int} which is having some spectrum. So, this entire frequency spectrum of V_{int} will be shifted to these higher harmonics and the fundamental harmonics of the square pulse.

So, if I assume that this is V_{int} is having some frequency content, all these frequency content ranging from say 0 to a certain frequency call it ω bandwidth will be shifted to this ω_1 and the higher harmonics of that. And therefore, I can represent my shifted signals as the magnitudes will be you know reduced as because of coefficients of the expansion will be diminishing as you go towards higher frequency. So, let me you know draw it a little bit let me this is supposed to be you know, let me draw it a fresh I just drew it equal magnitude.

(Refer Slide Time: 10:53).



So, the shifted one should be having lower magnitude. So, you had the original signal over here.

So, signal shifted to f_1 , f_2 having for the lower magnitude and so on. So, this is the spectrum we are going to get after the multiplication of the signal with the square pulse, and then after the amplifier we can once again go back with the reverse process, we can once again multiplied by the same frequency. And if the amplifier is having its bandwidth which is you know limited it will definitely reject the higher frequencies harmonic coming into picture we know that ultimately our amplifier is going to have some band limitation and we make sure that it is you know sufficiently lower than f_2 . So, we can ignore the higher harmonic coming into picture and assume that they will be diminished we can also have a dedicated low pass filter which is anyway going to suppress this.

So, in order to completely eliminate this in some cases (Refer Time: 12:08) may put a dedicated low pass filters stage if the cutoff provided by this amplifier is not sufficiently low or it is not guaranteed to be low and sharp enough, we can also incorporate a low pass filter over here before we go for the anti chopping process. So, at this stage basically what we are expecting is we are left with only the f_1 component that component of signal shifted to f_1 frequency and also we have add this point the 1 upon f noise still sitting at the low value.

So, I am drawing the signal V_x over here. So, this is let me call it V_x , the node V_x is having the 1 upon f noise spectrum still over here because just at the output of the amplifier the 1 upon f noise spectrum will be as given by the original amplifier; however, the signal has been shifted towards higher frequency because of multiplication with f_1 , and the higher harmonics have been rejected because of the low pass filter characteristics of the amplifier or presence of a dedicated low pass filter just after the amplifier. And now once again if I multiply this signal back with the same frequency, once again you will have this entire spectrum of the signal sitting at f_1 shifting back to the lower frequency or the ω equal to 0 frequency. So, once again if I multiply this with the square pulse the final signal that we get over here is once again going to come back to ω equal to 0, because the signal centered around ω_1 multiplied y th.

Student: (Refer Time: 13:55).

$\cos(\omega_1 t)$ once again is going to result in the dc component, and signals in the vicinity of ω_1 accordingly get shifted towards the frequencies in the vicinity of $\omega = 0$. So, we get back our desired signal.

However if I talk about the $1/f$ noise spectrum what happens to that after the point let me call this V_y . So, what happens to the $1/f$ noise spectrum add V_y . So, before the anti chopping switch so it is called the anti chopping switch; so this is the chopping switch. So, here we did the chopping we multiplied this frequency with this chopper which is plus minus operation, and after that we are having the anti chopping where we are again multiply the signal with the same frequency and shifting the signal back to the original spectrum, and if I look at the $1/f$ noise spectrum; however, that was sitting over here at the base band or low frequency it was going much sharp, going much higher at lower frequencies.

But now I have basically shifted this $1/f$ noise to the f_1 after the anti chopping operation; because for the $1/f$ noise is over here this is acting like a chopping operation. Therefore, this gets shifted to f_1 and my desired signal is back at lower frequency. So, basically I have been able to separate out my $1/f$ noise component with the desired frequency component, and hence mitigate the effect of this you know sharply increasing $1/f$ noise component at the low frequency, which was interfering with my data. Now if I assume that the signal has been sufficiently magnified. So, you also have this magnitude.

Which is you know a times the input magnitude which is going to be significantly higher and therefore, the $1/f$ noise or the thermal noise of the subsequent series may not be so, significant as compared to the signal over here. So, this is the one of the ways in which we can mitigate the effect of $1/f$ noise. Now if you look at there are this is the ideal picture there are of course, some issues related with this $1/f$ noise cancellation chopping as well, and that is going to help us in determining how to choose these frequencies that is the chopping frequencies and what are the trade offs in chopping the chopping frequencies appropriately.

So, let us first look at the choice of chopping frequency, what should be the chopping frequency. So, one of the criteria that we always have is this $1/f$ noise corner and we would like our signal to be sufficiently higher than this $1/f$ noise corner. So, that

it is not affecting our signal. So, definitely the obvious answer at the first hand will be that it should be sufficiently higher than this corner frequency. So, that after the anti chopping process the signal is sufficiently higher than this $1/f$ noise.

And again when I am turning it back it is the derive signal is coming back and the $1/f$ noise spectrum shifted to a much higher frequency given by the chopping frequency f_1 . So, in general the choice of the f_1 is some at least 3 to 4 times this corner frequency. So, if your corner frequency is 10 hertz I would like to keep this f_1 at least 4 or 5 times that f the corner frequency. So, say for limit is 10 times so that you can have an order of magnitude difference between the corner frequency and the center frequency of the shifted signal and of course, it depends for the bandwidth also. So, here we are assuming is that the bandwidth of the signal is sufficiently.

Lower than f_1 if it is comparable then once again you will have to take the limit on the lower side and say that this f_1 minus the bandwidth of the signal should be sufficiently higher than the corner frequency.

But if I assume that the f_1 is sufficiently higher than the signal bandwidth then we can ignore this bandwidth as compared to f_1 , and just make sure that f_1 is sufficiently higher than the corner frequency. Also ideally since this is you know $1/f$ noise curve.

So, here we are depict depicting it with a very sharp characteristics, let there is a transition sharp transition between the $1/f$ curve and the white curve. So, we are depicting with something like this, but under actual scenario of course, this is a $1/f$ curve which is going to have you know smooth decay, and then you have the white noise which is flat overall.

So, if we go higher and higher towards for the chopping frequency definitely, the effect of this $1/f$ noise will become dim will be diminished more stronger. So, cuddly we can say that $1/f$ noise corner frequency is the deciding point. If we make sure that the f_1 to which we are shifting the spectrum is sufficiently higher, as compared to the $1/f$ corner it seems like we can get a sufficiently good input referred noise we are able to mitigate this $1/f$ noise, but if you are more greedy we want to be even better in terms of the $1/f$ noise or overall input refer noise, we would like to push the signal

as far as possible so, that even the tail effect of this $1/f$ noise is not coming up and it is not affecting the signal.

Because I remember when you are talking about high precision signal, when you are talking about 10 bit, 11 bit further higher 16bit of precision, even this tail effect of noise which is increasing your overall noise can be important to address and we would not like to have even this tail effect corrupting our signal. So, we would like to take maximum possible advantage of the chopping and try to shift the signal frequency even higher by applying a much strong and once higher chop of chopper frequency, so that my signal after chopping is sitting far away from this $1/f$ corner and also by that chopping frequency f_1 the tail effect of this $1/f$ frequency has also diminished significantly.

Or in other words suppose the white noise level is given by V_{nw} , if this $1/f$ spectrum has fallen $1/10$ times of that till this point we would be having a separate limit we will say that the contribution of this $1/f$ noise is now 10 times lower than the white noise therefore, it is not very significant now. So, if you want to be more aggressive and save as much signal integrity as possible, you would like to push this $1/f$ upon sorry you had like to push this chopper frequency as high as possible so that this trailing part of the $1/f$ noise is also not having significant effect. So, analytically it can be shown that the overall contribution of the $1/f$ noise is significantly lowered if the f_1 is an order of magnitude higher than the corner frequency.

So, if you make f_1 approximately 10 times of the f_c , the contribution of this tail of an $1/f$ noise spectrum is false significantly lower than the white noise, and then you are having a maximum or the signal to noise ratio or more saturating. So, if I plot the signal to noise ratio versus frequency, it will go on improving till this point. So, if I plot the SNR it will be very bad in the initial phase and after that it will go on improving and after a certain point it will saturate. So, I would like to go to the saturation point, beyond that if you increase the chopping frequency further and further because this has anyway died down the tail of this $1/f$ has anyway died down it will not have significant advantage.

So, if I want to increase this further this is I am not going to get significant advantage in the SNR of the circuit and therefore, I would like to stop over there. Why would like to stop over there because once again what does a larger chopping frequency require. So, if

I am trying to impose large and larger chopping frequency to push my single spectrum much away from this $1/f$ and much further away from the tail of those $1/f$. I am enforcing larger clock frequency on this 2 multipliers and along with that, I am also having a constraint on the bandwidth of this amplifier; because in absence of the chopper the bandwidth of the amplifier was just supposed to cater to the input signal, but now the bandwidth of the amplifier must cater to this shifted signal $f_1 + B$.

So, now if this is the bandwidth of the signal $f_1 + B$ is the required bandwidth of the amplifier therefore, the amplifier now need to cater to this higher speed or faster signal and hence its bandwidth must be so much high and we know that if the bandwidth is supposed to be higher, we are going to have again constraints conflicting constraint; coming from the gain side you have the thermal noise also which are this is going to be impacted if you trying to increase the bandwidth. So, larger chopping frequency necessitates higher bandwidth of this amplifier, earlier it was operating in the baseband and the signal content was within 100 hertz. So, you would happy with even a 100 hertz bandwidth.

But now if I am operating with a few kilo hertz of chopping frequency the cutoff frequency of this amplifier has to be few kilohertz, and along with that you are going to have the constrain with the gain we are increasing the bandwidth the gain will be difficult to maintain, as a result you will have to once again take care of the precision consideration, try to maintain the gain of the required value by looking at other tradeoffs like sizing etcetera. So, for examples if you are trying to increase the cutoff frequency by say increasing the bias current that will going to reduce your r_o and hence increase the bandwidth of this circuit. At the same time it is also going to reduce your open loop gain otherwise likewise you have other scenarios as well you are having the compensation with the help of cc, there also you may need to relax the compensation capacitor value and that is going to you know exchange or tradeoff with your phase margin.

So, if we try to go for larger and larger chopping frequency, it has negative impact on the overall gain open loop gain of this amplifier that you can achieve, and once again you need to make sure that at this frequency while satisfying the bandwidth requirement it is able to meet your stability criteria, it is able to meet your phase margin. So, both of these are getting tightly coupled. The other issue that also needs to be taken care of is the you know optimization of the white noise and the $1/f$ noise together.

So, the white noise can also be pushed down if you use appropriate sizing constraint the white noise can also be push down further and further, so that your overall noise integrated over the signal bandwidth is lowered. For example, after the anti chopping operation when you are pushing the signal back at this frequency, they are once again the 1 upon f noise is not coming into picture, but the white noise indeed is coming into picture, and that is once again aligned with your signal content. Not only this if you see after the anti chopping process you also have the higher harmonics of this clock signal coming at this point right. So, you have not only f_1 , but the higher harmonic of f_1 multiplying this 1 upon f noise spectrum therefore, this the white noise that was present at all the higher frequencies because it is you know continuous and it is going to be present at even higher frequencies.

So, it is also going to have you know spectrum close to say $2f_1$ and $3f_1$ and so on and now when you are multiplying this $2f_1$ component with this f_1 , definitely this the noise white noise component in this interval is also going to get shifted back and come to this level as a result you will have the white noise contribution piling up because of the higher harmonics of this chopping signal as well. So, therefore, it is important to minimize the white noise component as well it is not just (Refer Time: 26:43) 1 upon f, but the white noise floor also needs to be minimized.

So, that when you are applying this anti chopping process and bringing the you know white noise components associated or located close to this higher harmonics. So, $2f_1$, $3f_1$, $14f_1$ back to the lower frequency $\omega = 0$, you are once again increasing the white noise floor close to the signal level and that can start corrupting your data. And therefore, minimization of the white noise floor also becomes important and for that once again we have to look at the overall you know expression that we have for the white noise component, which is dependent upon the gm of the input device, is w by L of the input device and primarily if I look at the first 2 component, it is the bias current of the input device and the w of the input device that needs to be sized up. So, once again these constraint needs to be followed, you need to make sure that the white noise contribution coming from the first 2 sources they are also sufficiently diminished.

So, that when you are applying the anti chopping process, the overall level does not really go up and degrade the signal to noise ratio. In general if you are having an overall low pass filtering operations. So, that after a certain point the noise contributions are

getting diminished. So, in that case the higher harmonics of the clock signals which are anyway diminishing amplitude. So, you have f , $2f$, $3f$. So, these are the guys which are bringing my white noise back to the low frequency and superimposing on the Bc. So, of course, as we go towards higher and higher harmonics their amplitude also diminishes. So, it is a convergent series it is not going to diverge, and apart from that you also have some low pass filtering affecting the circuit which is going to diminish the components at higher frequencies.

But still this series is converging towards finite value over here we need to minimize that finite value so that we can maintain a good signal to noise ratio. So, that sizing constraint also needs to be taken care of now this effect is termed as noise folding where you are folding, the higher frequency white noise back to the baseband and which is now overlapping with your desired signal. So, this mandates lowering of white noise also to as low value as possible and we have to take care of both these together, white noise as well as the $1/f$ noise. So, in some of the simplest examples also we will be looking at this surging problems how to co optimize this combination.

So, you have the choice of $1/f$ corner frequency, you have a choice of the chopping frequency depending upon that the moment you go for higher chopping frequency, you have power dissipation increasing bandwidth requirement increasing, and then you also have to make sure that the white noise spectrum is sufficiently low so that means, your anti chopping it is not folding back sufficient noise this folded back noise is also limited. So, all those constraint is to be addressed while designing the chopping for mitigation of low frequency noise.

Student: Sir is the clock frequency clock signal is 0 to Vdd or minus Vdd to 2 plus (Refer Time: 29:59).

Clock signal can be just 0 to Vdd. So, because here I have drawn a single ended versions as I have discussed earlier also in some of the other examples, ultimately the signal is differential and you can have a switch which is applying the differential signal to the positive and negative terminals of the amplifier in turn. So, if I look at the phases this will be the phase one during phase 1 the up input signal V_{in+} and V_{in-} they are coming to say V_{in+} and V_{in-} of the amplifier, and during the phase 2 which basically is these 2 switches let me draw it phase 2 and this is also phase 2.

So, during phase 2 these 2 switches are on as a result v_i plus goes to the negative input of the amplifier V_i minus goes to the positive input amplifier, and effectively it is multiplying it by plus minus 1. So, that is the way plus minus one implementation is done it is not that the clock still has to be plus minus 1.

student: Sir you have first said you (Refer Time: 31:06) multiply with the that signal not only f_1 f_2 f_3 it has some easy component also.

In this case you do not have easy component because you are multiplying with plus minus 1. So, here the signal V_i plus and V_i minus that is at one time it is applied directly to the plus and minus signal of the or plus and minus input of the amplifier. So, this amplifier V_i plus V_i minus appears over here, plus minus and in the ϕ_2 phase if the it is the cross switches are on in the ϕ_2 phase. So, V_i plus you connected here and v_i minus you connected here, as a result if it effectively means you are multiplying the signal by plus minus 1, because in one stage it will be multiplied by the gain suppose the gain is r_2 by r_1 or c_2 by c_1 . So, in first phase ϕ_1 it is getting a gain of minus c_2 by c_1 , in the other case similar getting a gain of plus c_2 by c_1 . So, effectively that is how you are multiplying it by plus minus 1.

Student: Sir why noise spectrum also switch means here the noise spectrum is multiplied and then if it is multiply the (Refer Time: 32:00) added to the signal and then it is come out at output node (Refer Time: 32:06) you draw that after anti chopping the noise spectrum come at f_1 . So, (Refer Time: 32:13).

No. So, this noise spectrum here at the begin with the 1 upon f noise whether you know lower frequency picking at ω equal to 0 , and then you multiply it with f_1 this was the noise spectrum. At this point you are getting the noise of the amplifier 1 upon f noise picking at low frequency when this symbol (Refer Time: 32:36) gets multiplied by this chopping frequency it goes towards you know the f_1 and higher harmonics of f and the signal frequency which was sitting at f_1 comes back.

Student: (Refer Time: 32:43) we apply low pass filter (Refer Time: 32:44).

Low pass filter amplifier itself having it in built low pass filter this will suppress. So, you may not you know need a dedicated low pass filter, but amplifier itself will have or we know subsequent filtering steady anyway you have anti aliasing filter.

So, they will anyway have such a cutoff frequency; because only this amplifier bandwidth is high because you are processing the chopped signal which is that higher frequencies the amplifier bandwidth it is supposed to be high, but after that the low pass filter etcetera anti aliasing filter that we have or the subsequent amplifier stage that you will have. Even after that as I said you will need another amplifier stage which is probably going to be a variable gain amplifier. will gain need to be controlled in automated fashion. So, that itself will not require chopping and its bandwidth will be much lower this is this. So or low pass filtering will be inbuilt in the circuit stages subsequent to this also.

And beyond that you anyway have a low pass filter. So, we can close our discussion here, and in the next section mostly we are going to look into some other examples where the noise constraints will be different. we will see that in the cascode coded cascode example also we will be looking at the noise analysis, frequency analysis stability analysis and how it is very different from this case, now we have the you know steps for arriving at sizing. So, now, given a specification higher level specification of the amplifier that we have started with in the beginning using all this information of noise analysis frequency analysis stability gain requirement bandwidth requirement, using all these analysis we can arrive at transistor level design, we can estimate what should be the required transistor designs or transistor sizes for a fronted amplifier. Some of the thing that we have already studied in our earlier courses is the signal swing the input common mode range, the overall you know output common mode range. So, they also act like important parameters.

So, combining what we have studied like the noise and the.

Student: (Refer Time: 37:56).

Stability along with the other parameters that come in like the input and output signal range and some other important issues like CMRR PSRR that we have not dealt with so far, All these so many issues combined together help us determining the sizing required for the transistors. So, some features or some specifications may be important some other specifications may not be important; like if I am talking about the fronted amplifier, their input common mode range will not be very important or input signal range will not be

very important because input signal is very small in quantity. Likewise there is an important quantity called slew rate for the amplifier.

Which deals with large signal operation at the output stage if the input signal is changing fast and by a larger magnitude the amplifiers slews and output the stage transitions is determined by the bias current and the load capacitance. So, slew rate happens when the input signal is changing fast and getting amplified by large amount so that the output has to swing you know very fast, one of the input devices becomes completely off and the other one becomes completely on. So, that is extreme case of the differential amplifier the slew rate also appears as one of the important specifications for the amplifier or the op amp. So, for the fronted amplifier once again slew rate may not be so critical because the fronted amplifier the very first stage is not introducing so much of slew.

Because the ampli voltage amplified after the first stage also pretty small in magnitude. So, at the max you are having few hundreds of gain and the input magnitude is you know 10 microvolt. So, you are still within maybe few millivolts after the first stage. So, you may not so much worry about the slew rate of the first stage amplifier also whereas, noise constraint becomes very important for the first stage. So, noise is going to play a heavy role in determining the sizing of the transistors, the w bias of the transistors, bias current of the transistor likewise the chopping concentration and the bandwidth is going to be very critical for the first stage amplifier. For the subsequent stage like the variable gain amplifier which is taking the amplified signal the noise constrain will be relatively relaxed you may not be implying chopping over there.

So, bandwidth constrain in will be relaxed, but it will be amplifying the signal to a large magnitude and therefore, the slew rate and the output signal swing can be important, input signal swing may not still may not be so critical. If you go deeper into the chain the filter, they are receiving a fully process or magnified signal which is at least maybe a few tens of millivolt, 100 millivolt and therefore, there the input signal range will also become very critical. So, depending upon where you are in the stage noise or swing one of these 2 will be more critical; likewise the other parameters like you know the input signal range and output common mode range, the bandwidth of the circuit and some other specification like CMRR PSRR they will also become important.

So, as you are in the earlier stage of the circuit as we said that the CMRR in PSRR there will be very crucial because of in a small mismatch between the transistor pair can lead to propagation of any noise in the supply to the differential sequence. So, any common mode noise which is appearing from the Vdd or the ground sources, they can completely overwhelm your differential signal that you are having at the output. So, these are another the important specification that we need to take care of. So, we can see that there is so many specifications, and based on those we need to arrive at the transistor sizing and you know block level implementations while meeting our target specs at different blocks for different stages in our whole signal precision chain.

And whatever we do here whatever baseline analysis we do here applies to any other general application or any other architecture that we are building. So, here we are discussing a baseline design, going down from the highest level specification down to you know all the different kinds of analysis and finally, arriving at the bottom line transistor level design. Whatever we do here applies in a similar fashion to other topologies the concept segment very much similar. So, probably we will take another parallel example where some ampli other amplifier topologies will be taking up and the similar concepts will be applied to show you another variation or another test of similar analysis or similar approaches. So, that we are comfortable with (Refer Time: 39:04) applying the similar strategy for any other design that you may take up.