Analog Circuits and Systems through SPICE Simulation
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Lecture - 23
Effect Of Zero's

Welcome back. Let us resume our discussion on the zeros and look at the circuit techniques to.

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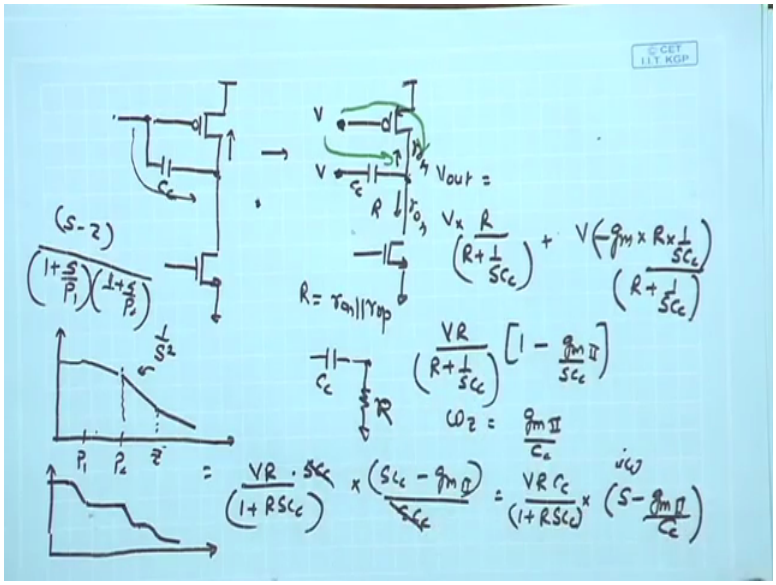

Mitigate the effect of that zero. So, as we have seen the origin of this problem we are having the zero because of this dual path from the input to the output. So, the origin of the problem is that we are having a signal path from the output of the first stage going to the output of the second stage, through this dual path one is through this capacitor and another one through this MOSFET and their phase are falling opposite at certain frequency and exactly canceling out at the zero frequency and that is what is the resulting in this term in the numerator. So, if you can eliminate one of these two paths, then we can get rid of this problem. That is one strategy one possible scheme used to compensate this kind of circuit and in order to do that we can think of inserting some component over here which can block the second path.

So, basically we want to eliminate the signal transmission from the input to the output through one of the path of course, this is not that path because this is the amplification part we do not want to disturb this path, but this is an undesirable path through which the signal is propagating from the input of the second stage the output of the second stage, and if you can block that then we can succeed in our stabilization.

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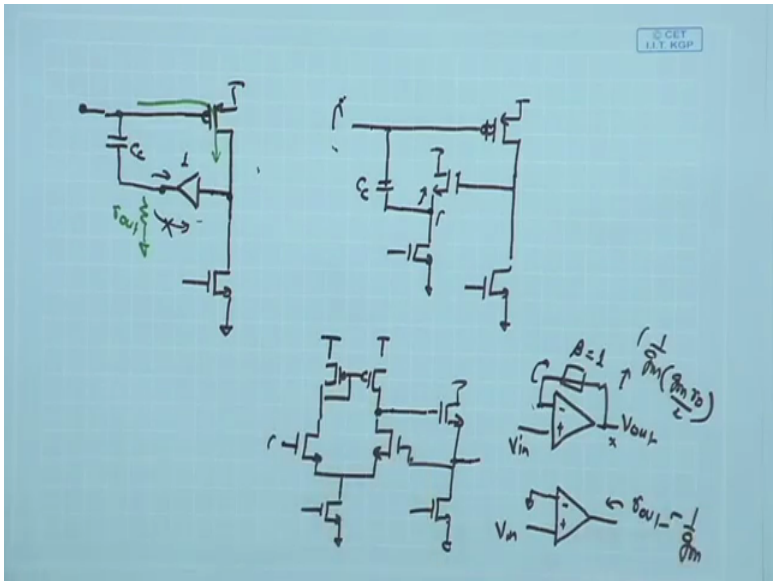

So, in order to do that we can insert a buffer may be a unity gain buffer with input at the final output and the output connected to the cc. So, this is once again my second stage I have inserted a unity gain buffer between the output and the input and this is coming from the output of the first thing I am not drawing that over here if I look at the overall functionality, because of this buffer it is a unit action buffer you can think of it as a voltage follower or even a simple common drain amplifier with gain close to unity.

So, in that case the common drain buffer or a unity gain buffer is going to transmit signal from the input to the output, but it does not allow passage of any signal from the output to the input therefore, it is going to block any signal transmission from the input to the output side therefore, the overall signal transmission now becomes only is now has only single path you have basically blocked the second path. Now does it still have the miller effect coming into picture yes because the gain is remaining same all you need for the miller effect and the miller compensation that the gain between or gain within the signal or voltage level at the other end of the capacitor with respect to the first end should be

sufficiently high, and that is not changing much because of this unity gain capacitor sorry unity, gain unity gain amplifier because the gain from the output to this point is one therefore, the miller effect remains intact.

Therefore, this is able to compensate the overall two stage response by still exploiting the miller effect and getting the cc multiplied by large number, at the same time it is also blocking the second path and hence helping us in achieving the overall a cancellation of the zero. Now in order to implement this particular zero, what are the in orders to implement this particular amplifier? As you said the simplest strategy involved is to use a common drain amplifier.

So, we can think of inserting a common drain amplifier. So, in that case our circuit sorry will look like you can have another bias point over here and this particular point goes to cc. So, this is one particular scheme where the overall output impedance of this stage is given by one upon gm of this transistor, which can be made to be relatively low, but once again when you are trying to incorporate this a stage and trying to make the gm lower it is you going to add additional power consumption in this particular branch, because it will need sufficient bias current to have a large gm.

So, that the output impedance of this stage is sufficiently low and it is acting like a (Refer Time: 04:55) common drain buffer. In this analysis if we assume that the overall output impedance of this buffer is very small, then we do not have an any additional pole coming into picture because if I assume that the output port of this amplifier is having almost 0 impedance, then basically the overall a resistance the equivalent resistance seen by this cc at this particular point terminal is almost close to 0, as a result it does not lead to any additional pole. But if the impedance is not sufficiently small it if it is relatively higher or comparable to the arrow of the MOSFET, in that case it can create problems and once again it can lead to additional poles coming over here. Because you can imagine that ultimately this point it is going to provide some r out of this common drain buffer or the unity gain buffer, and if this r out is very small it does not lead to adding additional pole, but you are not ensuring this to be very small.

Then once again it will introduce additional pole and then further complicate your analysis. Now you know application where you have power constraint like in our case we are looking for a front end amplifier or a biomedical application you having many

channels and therefore, bias current is an important factor, I do not want to burn a lot of bias current in this stage to reduce the r out. One of the other options is that you increase the w buyer of this MOSFET so that you can have a much smaller gm just by scaling the w by l because gm depends upon both the products used on the w by l times id.

So, that is another option, but that also has its limit because ultimately you will end up increasing the area of this MOSFET and as a result the channel area will increase, we know that we are apart from the power we also have a serial constraint on area in this particular application because we are going to have many many such channels or catering to different electrodes and we do not want to make any of the component too large to meet any of our design specification.

So, both from the point of view of power as well as area having this particular scheme can create issues it can valet our area constraint per channel or power constraints per channel also. Alternate method can be that you add a voltage follower over here, which can be constructed with the help of a negative feedback amplifier resistively low gain negative feedback amplifier without having too much constraint of gain or linearity.

So, we can construct a voltage follower using a simple single stage amplifier and all the better if we apply another common drain stage after this, then you have a then you basically have a positive output over here with respect to that if you increase this particular signal the output goes high and the panel open goes high and the negative output over here and therefore, I can connects these two you can have the negative feedback over here and as a result we know that this particular circuit the overall impedance for a voltage follower is going to be small.

So, this is what you are trying to implement you have the V in over here and we are trying to have a V out and we know that this particular combination is a shunt series combination, you are having shunted the sorry series shunt combination wherever series combination at the output and shunt at the series at the input in shunt at the output. So, basically you are sampling the output voltage and applying it at the negative terminal. So, it is in series with the input signal.

So, at the input side you have series combination, output we are just probing the voltage with a shunt connection therefore, and the beta factor we say it is unity for the voltage follower configuration, and in order to find out the open loop impedance and hence the

closed loop impedance you know that we can just put an open circuit over here because looking from the input port of the feedback network, I have a series connection at the output point. So, I can open circuit it and looking at the output port of the feedback network, the other terminal is shunt circuit.

So, I can just short circuit it or put in and ac ground this is the equivalent open loop circuit corresponding to the voltage follower and now I know the output impedance for this particular stage, if I am applying a common drain r out becomes approximately equal to one upon gm of the second stage, which is the common drain stage and beta is one and whatever is the gain of the overall to state is our overall open loop gain therefore, my closed loop gain or close the output impedance this case we know this going to be the open loop output impedance, which is 1 upon gm divided by 1 plus a beta, beta is 1 and the a is basically the a of this overall stage which is of the order of gm ro by 2.

So, we can get a very small impedance if we are using a voltage follower buffer constituted of this differential amplifier, and the common drain stage and remember here the response or the frequency response bandwidth of this particular stage should be within the or larger than the bandwidth of the overall differential amplifier. Because the signal over here should be able to follow the main input signal, otherwise you will not get the commiserate measure multiplication. So, this signal should be able to follow the input as well.

So, we cannot afford to make this buffer having lower bandwidth as compared to the main amplifier. For the common mode feedback we discussed a condition where we are only looking for the dc biasing part and so, therefore, even if we make the common mode feedback circuit very slow if we make the error amplifier of the common mode feedback very a low bandwidth it does not hurt the overall differential response, but here since this is the part of the differential operation we need this particular buffer amplifier also to have sufficient bandwidth close to the main amplifier. And one of the good point over here is that we do not need a very precise feedback factor and hence a very high gain for this particular buffer all we need is a sufficiently low a sufficiently low input output impedance, and the for that we need to just have sufficient gain.

So, that the overall output impedance looking into the output terminal of this buffer is sufficiently lower as compared to the impedances provided by the output stages of our

amplifier. So, if the output stage is providing impedance of say ro, ro by 2, the output impedance of this buffer if we are able to make it sufficiently lower than that as evident from this expression, we are happy about it. We do not need to necessarily make this gm ro too high to have any precise gain or closed loop feedback operation, that is not the purpose of this circuit the purpose of the circuit is just to have sufficiently low output impedance at this point, while providing almost unity gain and to do that we can relax the gain requirement over here.

So, rather than targeting a gm ro of few 100s as we do for the normal amplifier here we can go for few 10s and still get sufficiently low output impedance because it is going to divide the one upon gm by that few tens further and going to reduce the output impedance over here.

So, by this method we will be able to relax the gain requirement of this stage and therefore, we can trade off with the bandwidth with the similar amount of bass current or maybe a fraction of bass current use for the main amplifier, we can achieve similar bandwidth at the cost of lower gain, and still achieve a lower put impedance and a good buffer functionality for this particular unit so that the effect of zero is getting eliminated. So, this is one particular technique which we can employ in our design to use to arrive at the cancellation or elimination of zero.

Now, let us look at the second one, before we go any question on this par? So, let us a look at another common technique through which we can also cancel out the effect of the 0 by modifying this compensation path.

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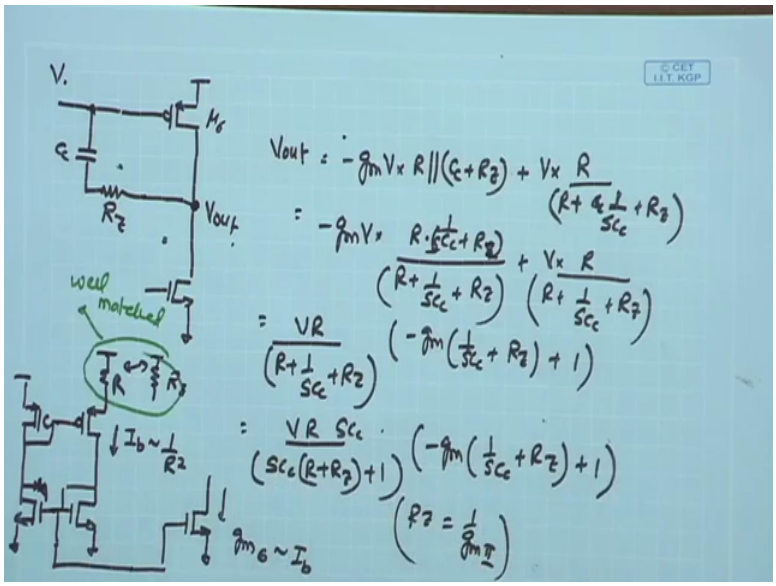

And that basically involves insertion of a nulling register in series with the cc. So, once again I have the second stage, I have just inserted another nulling register Rz in series with cc and therefore, I once again need to analyze the expression for v out in terms of the v in over here, and to do that once again we will revisit my previous analysis where I had used two parallel paths and arrived at the expression for the output in terms of the viewing.

So, I am going to repeat that only thing is I have inserted an Rz in series with the cc. So, here once again I can write down equation for V out as the superposition of the two parts. So, let us take the first part. So, this would be minus gm times V times the overall parallel combination of the small signal resistance at this point and the impedance provided by this path. So, the overall small signal impedance at this point provided by the PMOS and NMOS once again I am calling it say R and R in parallel with the series combination of cc and R z. So, R in parallel combination with cc plus Rz; this is the first patch gain and the second part which is again going to take into consideration the part through cc and Rz.

So, there once again while considering the second path we are going to assume that the circuit is that ac ground we do not have any signal applied over here and the signal is propagating only through this path and as a result I have the voltage division coming between the cc Rz combination and the effective are at this point.

So, once again I have the voltage division between R at this point and the combination of cc sorry one upon s cc plus Rz. So, we can try to solve this and look at the overall expression 1 upon Scc plus I am sorry this plus Rz plus V times R upon R plus 1 upon S cc plus Rz and I can once again take out some factors as common. So, V R and R and you have gm 1 upon S cc plus Rz plus 1 coming over here. So, this is the you know overall expression we can see and once again I can simplify it a little bit further and you have the other term as it is coming over here.

Now looking at the above expression, if I want to eliminate this zero coming in the numerator for that if I make this R is it equal to gm; so suppose in this expression if I set r is it equal to gm then this will cancel out with this factor 1 and you will be left with only the one upon Scc term over here, which will again we canceled out with this Scc term coming over here. So, if I set Rz equal to 1 upon gm. So, this gm is basically to gm the second stage.

So, I should call it gm two. If I setR is equal to 1 upon gm 2, then I can basically cancel out this factor I can eliminate the effect of this factor. So, in that case the only term will be left in the numerator is 1 upon Scc which is getting cancelled once again over here. So, this is another way by in something this nulling resistor Rz and setting its value equal to 1 upon g into I can effectively eliminate the effect of the 0 coming with all of this path and hence have a much stable response.

Now the problem here is the value of r that to be chosen and how robust this combination can be. So, we know that this Rz is the passive element which is which can be relatively well defined with plus minus 10 percent accuracy; however, gm is not a very well defined quantity it can vary significantly more widely. So, you can have plus minus 50 percent or even 100 percent change in the gm. So, if you are in simulations you are setting up this value of gm to be 10 to the power of you know minus 4, in that part then you may get a value which is 100 percent you know 2 x or 50 percent of that.

So, you can have a wide range in the values of gm that you get over here after fabrication and therefore, if you are trying to set this Rz equal to one upon gm to in fabrication in simulation, it is not necessary that after fabrication also you will get exact matching values are that equal to 1 upon gm 2 and hence you will be able to cancel out the 0. So, we need to make sure using some techniques that the matching between this Rz and the

gm 2 is pretty accurate and independent of process and temperature. So, to that extent we can try to define the overall gm of this MOSFET with the help of another by seen a scheme, where the gm of this itself becomes proportional to this Rz. So, if we make sure that the gm of this particular device is proportional to Rz then once again we can have a good matching between these two.

So, that is what we are going to see one particular method using which we can make the gm of the PMOS proportional to Rz very briefly. So, that incorporates a current reference circuit that we have not implemented yet in our design, we will briefly visit that and try to see that how it can help us in establishing a gm which is controlled by the Rz or is you know proportional to the other. So, that the cancellation can be much more robust so, to do that the scheme employed is that we use a we can use a PMOS current reference will be looking into this circuit in a little bit more detail and in this particular sorry in this particular circuit if this is an r value which is being used this is not a connection. So, in this particular circuit if this is the R value we can show that the by seeing current that we get out of this I bias is proportional to 1 upon R square

So that solution requires equating the current through this NMOS and PMOS and solving for the solving for the value of the current. So, we will be using this reference circuit later and we will be looking at the detail analysis of this particular block, and in this particular circuit the bias current provided by the reference branch is proportional to 1 upon R square, and if we can apply this bias current for this output transistor M 6 we can make sure that the bias current flowing in M 6 is also proportional to one upon r square and we know that the gm of the M 6 is going to be proportional to ib.

Therefore, gm of M 6 can be made proportional to ib and through that we can have a well defined matching between Rz and M 6. All we need to do is that this Rz needs to be matched with this R that we are putting in the reference generation circuit and as we have discussed earlier matching up to passive component very much feasible in integrated circuit. So, if you are trying to match to R values or to see values with a passive component they can be very well matched.

So, I can have these two resistance well matched as a result the Rz that we are having in the compensation branch, it is determining the bias current of the M 6 and the M 6 g and therefore, is proportional to Rz, and by appropriate sizing we can ensure that the

matching between Rz and the gm is very well controlled and it is much less dependent upon process and temperature and through that this cancellation can be made effective over a wide range of temperature and process variations and through that we can ensure that the overall zero cancellation is achieved across process variation. So, this is another scheme that can be employed for the overall elimination of the zero in the circuit, any question before we proceed further on the two scheme that we discuss for zero elimination.

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Rz in general we are having it is in the.

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Shunt path once again and it is in the second stage. So, if you look at the oral amplifier the noise dominated by the first stage and this is appearing at the second stage so that basically suppresses its effect on the overall output noise. So, and moreover it is providing a something similar to a shunt feedback just like we have for the main amplifiers there also we have discussed that if the feedback resistor Rz or Rf that we had in the op amp, that is having a shunt consideration the current mix by that at the previous stages relatively small as a result it is not going to have significant impact. And once again we will revisit that noise analysis while we discuss the transistor level noise analysis, and they also we will try to once again justify a little bit more detail analysis that the R vid appearing in the shunt-shunt feedback does not significantly corrupt the input signal or does not significantly add to the noise of the amplifier.

So, here also V c ultimately this is a shunt-shunt configuration output the sensing using a shunt connection V out is being sense. So, shunt and at the input side you are again mixing current. So, it is although it is the entire sachem voltage a voltage converter, feedback whenever the out feedback signal is mixed at the same terminal as the input quantity we have a shunt at the input also. So, you again we have a scheme which is similar to what we had in the op amp and we use that large Rs to bias the input nodes something similar over here. So, in the company in the simulation exercise also you can try out both these methods and try to see the effect of zero on the overall phase response. So, I will try to frame a problem where you will be able to observe the 0 little bit more prominently and then you may we asked to use one of these two methods to cancel the 0

and get a better phase margin. So, this two stage op amp is again once very versatile block that you may be required to use that different stage in the overall design.

So, you have a frontend amplifier you have the second stage amplifier which is going to be probably a programmable gain amplifier beyond that you have filters you may have adcs. So, this two stage op amp can be pretty handy in building all these different blocks fronted amplifier the filters even in the adc if you are doing certain topologies you may be using this kind of amplifier therefore, we are spending some more time in looking at the analysis. So, so far we have seen the dc biasing point we have look at the frequency response stability etcetera and the other path that is supposed to be addresses in wide analysis which is also going to play an important role in sizing of these transistors in our amplifier.

So, the next part we are going to look at is going to be noise analysis of this two stage amplifier, and as I just pointed out the noise analysis essentially boils down to the low noise design of the first stage because that is the most crucial stage, if you are having a high gain amplifier we are targeting say 10 to power of 4 10 to power of 5 gain from the open loop, there we assume that the first stage is having at least few 100s of gain.

So, the noise contribution of the first stage is going to be dominate. So, all we have to do in noise minimization is to make sure that the noise of the first pair there is the differential pair is minimized by appropriate sizing considerations. So, that is what we are going to look at next and determine the sizing considerations to minimize the noise contribution of the differential pair.

Once this is complete, then we can go towards transistor level design and try to arrive at the transistor sizes analytically considering high level drain specification that we had for the amplifier. So, whatever we are doing here the frequency response of the noise analysis ultimately similar concepts will be applicable elsewhere also, even if you are using other amplifier topologies like a one of the target this to look at folded cascode topologies, where we do not have this problem of zero, we do not need to have miller compensation there we have another scheme which is called dominant pole compensation which is inherently stable does not give the 0 in the overall response.

So, we will be looking at an alternate apology also, but the overall concepts remain similar you have to look at the frequency compensation, you have to make sure that you

are visiting a for every degree phase margin by inserting capacitances at proper point and make sure that whatever compensation etcetera you are doing it is robust enough it is not you know failing at different processing temperature.

So, that is another important point apart from that whatever we do in the noise analysis part or dc biasing point the similar concept apply in other circuit topologies also. So, folded is another very handy structure which can be employed at in building different functional blocks. So, there also we will be looking at similar analysis. So, once we have gone through these steps probably, we can apply similar things to the polaroid cascode structure that we will be taking up for analysis after this, and start our the discussion on noise analysis of the two stage amplifier.