Analog Circuits and Systems through SPICE Simulation
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Lecture - 22
Miller Compensation Of 2-Stage OP AMP

Hello and welcome to today's session. We are going to continue with our frequency response for the differential operation and we are going to look into the stability analysis the application of miller composition as we did for the common mode case.

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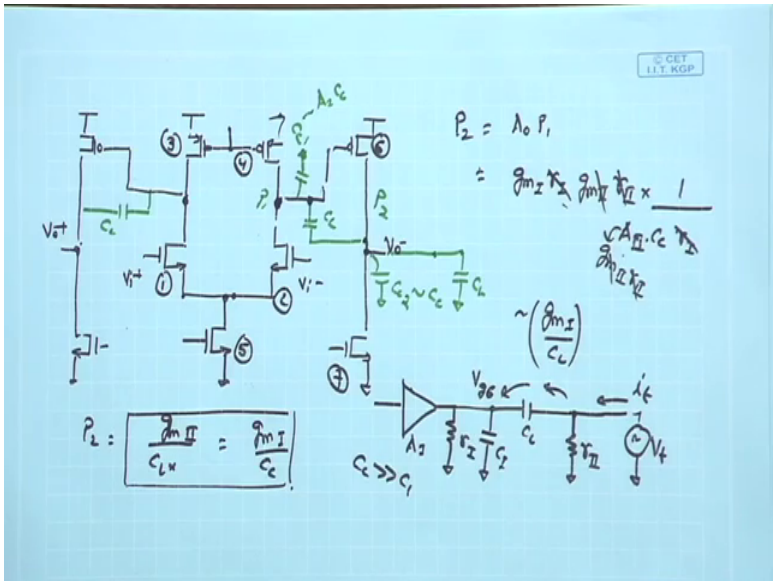

So, let us look at the frequency response of the fully differential operation for which I am drawing the entire 2 stage amplifier again and here we have the input and the output. So, we have already identified the critical poles in the circuit we mentioned that the load terminals of the first stage are going to produce or going to our relatively high impedance. Therefore, you have ro over here ro by 2 impedance coming over here as a result this is a high impedance node this is going to give us the first critical pole. And likewise in the output node once again the overall impedance is ro by 2 this is the second critical node for which need to figure out the poles.

So, for the AC half circuit we are going to deal with only the differential half circuit where you have a AC ground at the common source point of the differential pair therefore, we are left with our common source amplifier with PMOS active load, NMOS

input device. And second stage is anyway a common source stage where you have a PMOS as the input device and NMOS as the load device. And here we know that the overall differential gain that we are looking at is gmro by 2 whole square. So, this is the information we discussed last time.

And once again looking at the 2 stage topology we have we have to arrive at a proper compensation scheme just like we did for the common mode case here also we can take the help of a compensation capacitor so that one of the nodes is pushed towards very low frequency. And we get good phase margin and to do that we can exploit the gain of the second stage and put a compensation capacitor between the output of the first stage and output of the second stage.

So, let us put compensation capacitors between the output of the first stage and the second stage and we know that as the result of this will produce an equivalent capacitance C 1 dash I can call it or C c 1 which is the equivalent component resulting from the C c at the first node and that is going to be A 2 times C c approximately where A 2 is the gain of the second stage. And at the output we are going to get C c I can call it C c 2 which is the equivalent capacitance resulting at the second node or the final output because of C c 2 and which is approximately going to be C c only because this is going to be C c times 1 minus 1 upon a where a is large and therefore, its approximately C c.

So, this is the condition we have and apart from that we can have an additional load capacitance which is because of the subsequent stage the next stage coming. So, you can have an additional load capacitance C L also. So, for example, if this particular stage is driving another amplifier which is having another capacity feedback and it is having a large input capacitance of few picofarads to just give you a larger gain that can act like the load capacitance of this stage. So, that is coming from the next stage.

So, and in general that C L can be sufficiently larger than the other parasitic components at this node. So, that will be given by the input capacitance effective input capacitance provided by the next stage. Likewise since we have a fully differential operation you have the same thing on this side as well. So, I am focusing on one side. So, same thing because of symmetric operation you will get done the other side as well.

Now, here what are the relations we need to follow for obtaining the overall 45 degree phase margin? Just like in the case of our common mode operation we are going to have

similar analysis here and our target would be to make the second pole or the non dominant pole A naught times the dominant pole. So, the lower frequency pole as we said that is going to be pushed towards low frequency and we want the second pole there is a non dominant pole let us call it P 2, we want P 2 to be, we want P 2 to be A naught, A naught times P 1 where A naught is the low frequency gain of the 2 stage that is A 1 times A 2 and for that first of all we need to look at what is the P 1 and what is A naught.

So, for A naught I can write it down as gm 1 gm 1 means the gain the gm of the first stage times r 1 that is the total output resistance of the first stage that is just r op parallel ro n. So, if I say the total output resistance at this node that is r op parallel ro n for the differential operation remember for the differential operation this is at AC ground. So, in order to find out P 1 I need to find out the r equivalent and C equivalent at this particular node and the r equivalent is basically ro of the PMOS coming between this node and AC ground and likewise ro of NMOS come in between the output node and another AC ground.

So, therefore, it will be ron parallel rop and that is what I am mentioning as r 1 that is the small signal output resistance of the first stage effectively and gm 1 is the gm transconductance the first stage. So, gm 1 corresponds to the transconductance of the input pair. So, here the subscript denotes the stage the first stage gm 1 r 1 and then you have the second stage the low frequency gain. Second stage once again I can write it down as gm 2 r 2, where gm 2 be correspond to the gm of this transistor and r 2 will be the overall small signal resistance at this stage which is basically r o P parallel ro n once again at this particular stage.

So, this is the A naught that is the overall low frequency gain from the input to the output remember while calculating the low frequency gain we do not consider the other parasitic couples components parasitic capacitances and their frequency effects and then we also need to find out the P 1. So, for the P 1 we know that the overall capacitance at this node has been modified as A 2, A 2 times C c which is basically nothing used, but gm 2 times r 2 and then you have the overall small signal resistance still given by the r 1. So, this is your P 1. So, here we can get r 1 cancelled and you have A 2 which is basically the thing is, but gm 2 times r 2. So, this is your A 2 and therefore, these 2 factors also get cancelled and therefore, you are left with gm 1 upon C c. So, what I want to do is I want

to make the P 2 the I want to make the P 2 equal to gm 1 upon C c because is the relation that I want to have.

Now we also need to look at the second pole what is the expression for the second pole that we are going to get, but for that we need to look at the resulting small signal resistance and capacitance at this node. Now, if I assume that this C L which is coming close the next stage maybe in this case the next identifier or filter. So, assuming that C L is sufficiently greater than all other parasitic capacitance at this stage we can assume that the total parasitic capacitance C equivalent at the second stage is dominantly C L, assuming that to be true I can write down the C equivalent as C L at this point.

Now, the other question is; what is the r equivalent at this point that is? What is the small signal resistance at this point? So, if I look at low frequencies at low frequencies definitely for writing the gain we have used the for overall r equivalent at this point equal to the ro of p parallel ro of n that is giving us ro by 2. But if you are looking at frequencies much beyond P 1 there are certain effects coming call of this C c the impedance of the C c going low which is going to degrade the overall small signal impedance at this node and let us see how does it give us an advantage in terms of compensation of the overall amplifier response.

So, in order to look at the overall impedance at this node over all possible impedance at this node at frequency is much higher than the first pole P 1. We can draw the equivalent circuit I am going to draw a equivalent circuit for this particular second stage where I can model the second stage, the first stage over here by its equivalent output impedance you can call it ro 1 or r 1 and at this node I have some equivalent capacitance coming over here between this particular node and the ac ground because of all other components.

So, I am retaining the C c and I am saying that at in the actual amplifier if I look at the actual first stage this is the first stage giving me A 1. You have certain output resistance, so I can model its equivalent output resistance as say r 1 and along with that you have some capacitance C 1 which is because of the parasitic capacitances of the MOSFETs NMOS and the PMOS.

And then you have the C c which is connected from the output of the first stage to the output of the second stage. So, here I have the C c connecting the output of the second stage from that of the first stage and likewise at this particular point I also have the total r

the small signal resistance of the second stage I can call this say r 2. So, at this particular point I am modelling these 2 MOSFETs, they take of these 2 MOSFETs as r 2. So, that is the small signal resistance of the NMOS and PMOS combined r 2.

And now my purpose is to just find out what is the overall small signal resistance looking into the output node at frequencies much higher than P 1. So, for that I would like to inject some test voltage over here V t and try to observe the I t what is the small signal current that is how we find out the overall impedance small signal impedance looking into a particular node. Effectively what I am doing is I am just putting a small signal voltage over here at this node and trying to find out the resulting I t and for that I am modelling this overall 2 stages as the equivalent resistance and capacitances at those stage.

For example, here I have the second stage and modelling it as the r 2 which is the r up parallel r down of this stage, C c is connecting the output of the second stage from the output of the first stage and the first stage once again modelled by the equivalent parasitic capacitance C 1 at this stage and the r 1 the total small signal resistance coming at this stage because of the amplifier.

So, here I have not applied in miller effect I have not broken C c I am just looking at the exact behaviour how is it going to behave at this very high frequencies. The point to be noted here is that the C c is much larger than the parasitic capacitances provided by the first stage. So, C c is much larger than C 1 and we are assuming that we are at sufficiently higher frequencies. So, we have crossed the first pole P 1 and we are sufficiently higher than that. As a result the one upon omega C 1 the impedance of this component is dropping as compared to r 1. So, if I make that assumption then I would assume that the parallel combination over here is dominated by the impedance of this parasitic capacitances one upon omega C 1. So, that is the assumption I am making because I am at relatively high frequency.

So, in that case what I can say is the overall voltage coming over here I can call it the Vg of if I call this 6, M 6 because this is every number is 1 2 3 4 5 and 6 let us call it M 6. So, the total voltage over here V g 6 there is a small signal voltage coming over here because of light signal V t over here and if I assume that the overall impedance in this parallel branch is dominated by the C 1 which is the parasitic capacitance at this node my

V g 6 over here will be given by the ratio of these 2 capacitances the voltage division provided by these 2 capacitances. And because my C c is much larger than C 1 because of the parasitic voltage division we have the impedance of this one much smaller than the impedance of this as a result V g 6 is going to closely follow V t and therefore, this node is going to very closely follow V t.

But, but we are trying to say is that at lower frequencies the vg 6 starts following the output signal over here very closely another is what we are effectively having is there is a the 2 nodes are effectively getting short circuit from the point of view of AC. So, effective impedance in between these 2 node is degrading and effectively is these 2 nodes get shorted the M 6 over here, behaves or starts behaving like a diode connected MOSFET whose impedance looking into the drain will be approximately 1 upon gm 6 or in other words following our earlier nomenclature gm 2 that is the gm of the second stage.

So, the conclusion out of this is that we are trying to we are having a reduced effective impedance at the second stage because of this bypassing effect provided by C c at high frequency which basically is going to push the second pole at much higher frequency. Rather than having an overall impedance over here given by ro by 2 we are having an effective impedance at high frequency given by just 1 upon gm 6 which is the small signal impedance provided by M 6 when it is getting effectively short circuited and the gate of the drain of the MOSFET M 6 is getting effectively short circuited.

So, the P 2 expression if I have to write down that will be given by one upon the effective small signal capacitance here and assuming that that is dominated by C L I have the overall impedance over here given by 1 upon gm 6. So, it basically goes up and I have gms 6 or basically gm 2 that is the transconductance of the second stage as we have defined. So, in order to achieve 45 degree phase margin we want to make this equal to the gain bandwidth product that we are just arrived at this is our gm 1 upon C c. So, this is the relation we would like to obtain in order to have whatever degree phase margin in this circuit.

So, as we have said if you are going for single loop the same capacitor can compensate the common mode as well as the differential operation. So, the common mode also same capacitances will be coming into picture when you will consider the loop if you are

having a single you know form of that loop. So, that also has is discussing the class. If you have separate loops then of course, the 2 loops have to be composite it separately, if it is a single loop then we will see that even the error amplifier is the common mode feedback is not going to have significant you know it is the pole of that amplifiers also going to lying at very high frequencies.

So, as we have discussed that if you are having a single loop in that case just to reduce the overall loop gain we keep the gain of the error amplifier is pretty small by adding entire connected load for both the, you know range and in that case the dominant poles are coming only from the first 2 stages of the amplifier and the error amplifier does not contribute significantly to the pole.

So, in that case we need to compensate the P 1 only that is the main dominant pole for the differential response as well as the common mode response. So, we will revisit that once we finish this we will complete the common MOSFET back circuit also and try to you know make sure that both the loops are getting satisfied, both the loops are getting compensated. Any other question?

Student: What was happening in that putting of (Refer Time: 17:59).

So, that was just to isolate the common mode from the differential. So, here also we will see that ultimately to tackle some other issues we may need to put a buffer.

Student: (Refer Time: 18:09) r 1 is the second stage may not be (Refer Time: 18:11).

That is when you are using separate loops. So, if you are using separate loops for the first stage and the second stage for the common mode feedback then that is the result, but if you are using single loop then you have you know the same capacitances compositing both of them. So, we can go towards the other issue which comes up with this C c and that is the case of zero. So, we have ignored all throughout the zeros coming up in the depression of the fire or the operation of the fire circuits and that can they can also play very crucial role in determining the overall stability they can affect your stability in a negative manner.

So, let us look at the prospects of zero how does it arrive in this circuit and then what is its effect on the overall phase response and then how to resolve that effect using some appropriate you know components to be added in the feedback loop.

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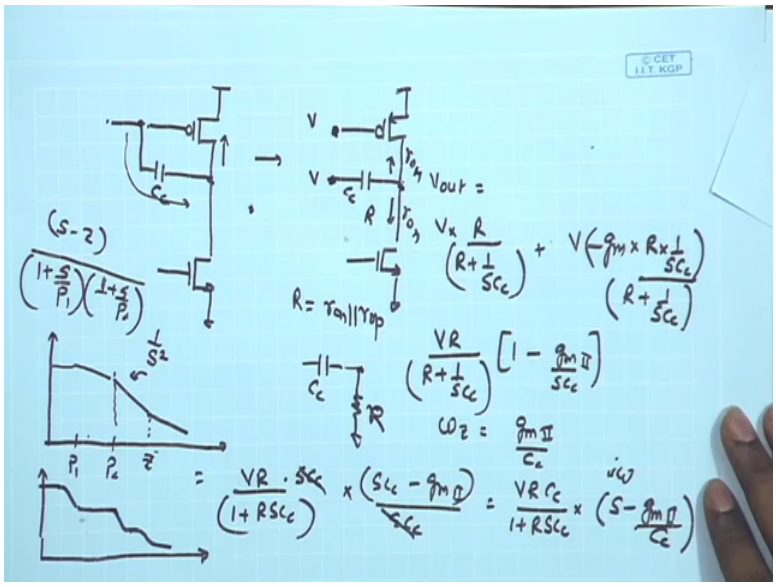

So, here if I look at the second stage, you are having the C c between the input of the second stage and output for compensation and result we have 2 different signals paths one coming from the input to the output through the C c and another one coming from the drain of the MOSFET. So, if I for example, if I isolate these 2 if I isolate these 2 resume these are 2 independent signals being applied at the input of the second stage.

So, suppose with although they are same signal, but I am just disconnecting them and assuming that they are 2 different signals. So, from the input of the PMOS we have one path we can find this overall output voltage as a superposition of these 2 signals - one coming from the input of the MOSFET to the output and you have an inverting it if I it is get the effect of V applied at the gate of the MOSFET to the output you have an inverting it whereas if I take the effect of this particular V on the output you have some overall voltage division provided by this capacitor and the overall impedance over here which can be relatively in phase of the applied signal over here.

So, if at some frequencies the signals provided by these 2 paths at this particular point have exact cancellation because of having a bulk degree phase shift over here and relatively you know positive phase over here these 2 signals can combined in a

respective expression and as a particular frequency if the cancel out each other then you have a 0. Because the overall signals the overall small signal coming over here from these 2 signal paths the inverting one and the non inverting one will be 0 and that is going to give us the frequencies of the 0 in this circuit.

So far we have ignored the zeros and that happens because we are taking approximate analysis we are assuming miller effect and getting down the capacitances are different nodes. So, we are ignoring the signal propagation through these capacitances at higher frequencies. And remember than the concept of miller effect that we use has inherent approximation that the same gain the low frequency gain is valid at higher frequency that which we are applying those capacitances also this is also not true. Because when we applying the research and think the low frequency gain that is valid for the past band or low frequencies below the dominant pole of the circuit as we go towards higher and higher frequency the gain also reduces which we do not take into consideration by applying our approximate analysis using miller effect.

So, if we look at this particular combination I can write down the expression for the output signal over here as a superposition of these two. So, I can write down V out as V times the capacitor division between the voltage division between these capacitor and the overall impedance over here. So, I am going to represent the impedance of this MOSFET say as R. So, suppose a small signal resistance provided by this MOSFET NMOS is R which we know is R over 2. So, here if I look at the or you can a we can assume that the total impedance total small signal resistance provided at this node by the combination of this PMOS and NMOS is R. So, you have rop looking upward and ron looking downward. So, the small signal resistance R and assuming is combination of ron parallel rop.

So, effectively if I am looking at the voltage division this particular of voltage is applied to a voltage divider form of this capacitor C c and R, also at the R. So, this is V out the expression of the out because of this particular signal is just going to be V into R upon R plus 1 upon S C c and for that, for by considering this you have to consider that the other V is set to 0 because we are taking superposition. So, when we are applying a V over here we assume that the gate is not on any signal. So, this is going to be AC ground and then the other MOSFET provides only the small signal resistance ro 4 and the NMOS ro n.

So, basically we are having the expression of our output because of a light signal over here likewise we can take the signal at the gate of this M there is a PMOS and then find out the expression of the output voltage with respect to this signal. And while doing that similarly we will assume that the other signal over here is set to 0. So, in that case I have V which is applied at the gate of this PMOS we are going to get minus gm minus gm times the overall small signal resistance over here and that is going to be equal to R parallel this one upon SC c.

So, minus gm times R parallel 1 upon SC c right because if I am looking this looking at this circuit as a common source amplifier where input is the M 6 this PMOS device at the load I have this overall small signal resistance ron parallel rop which is our R and if this is set to AC ground while analyzing the effect of this signal this 1 upon SC c also appears in parallel with ron and rop.

Let me read it ron and rop, and as a result I can write down the overall impedance minus gm times R parallel 1 upon SC c sorry. So, let me just complete this R plus 1 upon SC c. So, this is the overall expression that you get because of the combination of these 2 signals at the MOSFET gate and at the input terminal of this capacitor. And then I can take out R upon R plus 1 upon SC c and I have 1 minus gm times 1 upon SC c coming.

So from here we can see; what is the value of the 0 that we were expecting. So, let me call this gm 2 because ultimately this is a gm the second stage, so following our previous notation I should write it gm 2. And as a result I have the omega 0 given by gm 2 upon C c because at that frequency this term will be cancelling out and you will get an overall gain approaching 0 this is the 0 frequency that we are going to have.

Now, in the overall response if I look at the overall response I have the first stage which is giving us an inverting gain. So, from there we have inverting gain coming into picture and an overall 180 degree phase shift coming from there and we have this second stage once again giving us 0 term coming over here. So, if I incorporate the gain of the first stage I already have a 180 degree phase shift because of the first stage and then we have a second term over here. Let me simplify this little bit further and arrive at relatively simplified expression. So, you have SC c minus gm 2 upon SC c. So, this is an overall expression we are obtaining and then I can take out C c from here.

Now, if we look at frequencies which are much higher than omega much higher than omega 0 at those frequencies we have the S term being dominant, so this will lead to effectively increase in the magnitude of the gain. But if we look at the overall bode plot we of course, have the other 2 poles assuming that the 2 poles are coming at higher frequencies sorry at these are the lower frequencies as compared to the 0 we already have a gain decaying width minus 40 dB per decade slope and just justify that yes this is 0 which is a sufficiently higher frequency we see that the overall impedance 1 upon gm coming at this node is sufficiently small as a result is 0, 0 can be expected to lying at a relatively high frequency as compared to the pole P 1 and P 2 that we had in our original amplifier.

So, in the compensated amplifier also because the P 1 and P 2 are defined by the relatively high impedance nodes and the capacitance values which are sufficiently larger. We can assume that this particular 0 is at very high frequencies as compared to the dominant pole and if we assume that it is also higher than the sufficient second pole we are having a 40 dB per decade slope before this 0 comes because the earlier 2 poles are going to contribute overall 40 dB per decade decay in the gain before this 0 approach here.

So, I assume that that is true. So, the overall bode plot. You have the P 1 and P 2 suppose coming at the relatively lower frequencies. So, after P 1 you had minus 20 dB per decade slope and an after P 2 you have minus 40 dB per decade slope and then you encounter this 0 in the numerator expression. And after this we can say that once you cross the 0 this omega term become dominant you can ignore the second term as a result this is going to cancel out with the other 2 terms that you get till this point. So, till this point the expression of the overall gain was dependent upon omega square, but after the 0 you get another omega in the numerator right because of the 2 poles remember you have 1 plus S upon P 1, 1 plus S upon P 2 in the numerator and then now you are having S minus Z term coming over here.

So, if you are if the S is much larger than Z and also the S is much larger than P 1 P 2 then the overall expression that you get is S upon S upon P 1 times S upon P 2 because in the new denominator you can ignore this ones and in the numerator you can ignore this Z once your S is much greater than this 0 frequency. As a result you get once again minus 20 dB per decade slope.

So, slope goes back to minus 20 db. So, you started it minus 20 dB after the second pole you got to minus 40 dB and then after the 0 you are again back to minus 20 dB per decade and likewise if I look at the phase response what is the effect of the 0 on the overall phase response.

Now, we have an overall negative sign coming because of the previous stage also and you are having an iota omega term coming at this stage. So, it is going to if I look at, if I incorporate the previous (Refer Time: 31:11) sign. Once again you are having an additional phase shift of 90 degree coming because of this particular pole after you cross the Z. Another result once again the phase becomes all the more negative and the magnitude is going to increase.

So, as a result we are having and overall phase which was which will basically approach once you had agree much faster because of the 0 because it is going to make it all the more negative. So, you are having a further phase degradation and if this also degrading the slope. So, the slope of the decay of the gain has been reduced and the space is degrading further, as a result the possibility of encountering instability can be enhanced because the rate of decay of the gain has been reduced at the same time the rate of decay of the phase is getting increased. As a result this particular 0 can reduce the phase margin and for that we need to address this issue and we need to make certain modification in the circuit, so that the 0 can be eliminated.

So, let us get back to this point and look at the circuit solutions to you know eliminate this 0 in our amplifier through couple of circuit schemes.

Student: (Refer Time: 32:31) sir in the expression that you have found out for the 0 (Refer Time: 32:36) form of 1 plus R SC c is the denominator (Refer Time: 32:39).

Yes.

Student: So, if you are saying S is that 0 is coming from higher frequency. So, cannot we assume that in the denominator and srcc term will also going to come that expression that (Refer Time: 32:51).

In this r is you know much lower frequency, here if I look at the, so what do you mean by it is going to come in. So, can you elaborate?

Student: (Refer Time: 33:04) ask the expression that will be (Refer Time: 33:05) S minus (Refer Time: 33:06) S by t minus (Refer Time: 33:08) be a dominant omega srcc (Refer Time: 33:11).

In the denominator.

Student: Yeah.

So, that is if I look at S upon P over here. So, that P is at a you know much lower frequency because this R L going to be much smaller than this gm. So, you have the other poles like if I look at the; so you also have another expression. So, if I look at the R and so if I assume that it comes at a frequency which is much lower than this gm even then you get a overall you know reduction in slope and if I compare what are the what is the value of this. So, if you look at R and C c, R is the overall output impedance coming at this point and C c is the equivalent the C c value that you have a obtained and if I look at the other expressions which are coming because of the poles at the 2 nodes over here and here.

So, we have the pole because of the second node going to much higher frequency because of the reducing impedance of C c, so that term has not been you know taking care over here. So, here we are ignoring the other circuit combinations because you have you know high impedance node coming over here and we following our arguments in the earlier discussion we analyzed that this impedance is going to go lower here that assumption has not been taken. So, here just to show the effect of the 0 and without considering the degrading impedance over here and the drain and gate getting short circuited. So, those things have not been incorporated over here.

So, this is just to you know usually the first order equations just to show that how the 0 is appearing without considering the other effect where C c connecting the drain and gate is effectively getting short circuited and it is reducing the impedance which is pushing that pole to high frequency. So, if you do exact expression, like if you write down the transfer function without considering any miller effect and find out the exact direction for V out and V in then you will get the expressions for the original poles and zeros at different nodes without having any approximation involved. And there again you can find out the expression of 0 coming in the numerator along with the terms in the denominator

factored them out and get the expression for the exact poles and there you can take approximation and arrive at a more you know exact value of these poles.

So, here while considering the effect of 0 just to show that the mechanism is; what is the mechanism of original of the zeros, we are using this model while ignoring its connection with the previous stage and the impedance is provided by the previous stage. So, this is once again just to do a hand regulation and show overview of quick analysis. Exact analysis is lot more tedious and it will lead to a second order or third order expression in the denominator if I find out the expression of V out versus V in using S domain analysis. So, that leads to exact expression for poles and zeros where you are not doing it in isolation there is a second stage and in the first stage that is more complete.

Student: (Refer Time: 36:34) greater than Z (Refer Time: 36:37) main difference will become like (Refer Time: 36:40) plus 90 degree (Refer Time: 36:41).

No. So, here you have minus sign is also incorporated. So, if you look at the previous stage you have a negative sign coming because of the previous stage and you are having the iota omega coming over here. So, if I look at the signal from here you have overall negative sign coming from the you know previous stage and multiplied by that it will give you an expression which is minus gm by C c minus gm. So, that has already that is already giving you negative sign. So, this is basically.

Student: (Refer Time: 37:23).

Zero for C c minus S. So, it will give inverted. So, second there is an approximate analysis there we have not considered an interaction of the previous stage with this stage I will just assuming you know that you have a signal applied over here from an ideal source and we are considering only the 0 coming at this point to this path and not considering the effect of the impedance provided the previous state.

So, that is an approximation involved here just to isolate this analysis and show you the origin of 0. So, resume our discussion on this 0 and look at the circuit’s techniques which can be applied to remove the 0 or cancel it with some other terms in the denominator.