Analog Circuits and Systems through SPICE Simulation
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Lecture - 21
Frequency Response Of Differential Feedback (Contd.)

Welcome back.

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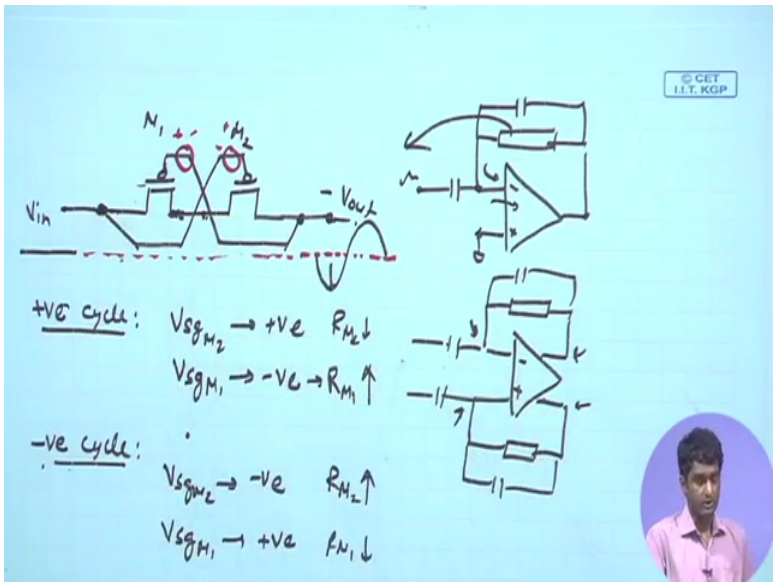

As we mentioned we are going to look into some options for tuning this high value resistor that we just discussed and the main motivation is that we want to have some option to compensate for the process and temperature variations.

So, we will see in simulation exercise also we have options of doing temperature and process simulations we can run temperatures and different corner simulation to see how much if the resistance varying over given range of temperature and in general integrate circuits can be exposed to a wide range of temperature even if it is for a specific application like a neural interface. In this case and likewise process point of view also we can have significant shifts in the V t it can be time dependent shift as well which can shift the characteristics.

So, we want to have some kind of tuning options which can be used to do calibrate these values either automatically or one time the preferred way maybe to have automated

calibration. So, that once we have deployed the chip for its normal operation there also you can have some mechanisms for sensing it and then again using the tuning option for adjusting the values. So, we will not discuss all those we will just discuss how we can implement one possible scheme for tuning.

So, the basic mechanism involved in tuning is that we want to intentionally add a kind of battery over here with the help of which we can adjust the resistance level that we are going to have. For example, if we ensure a significant voltage drop between the V out and the gate. Likewise, if we ensure some significant voltage drop between the V in and the gate of the m 2 the transistor which is getting on will be getting or more strongly and likewise the transistor which is getting off will not be staying of that strongly. So, basically if I in certain additional voltage over here such that the transistor staying off has a additional V sg drop that can help us in reducing the overall resistance across the switch that is one way through which we can control the overall resistance provided by this device.

So, let us just look at one possibility; how can we create such a battery and put it in series with this MOSFET so that the overall resistance can be reduced and we can try to simulate that example also in that you see how we can obtain such a control in the device. So, one possible way of implementing such a transistor level battery is to use a tuneable current load.

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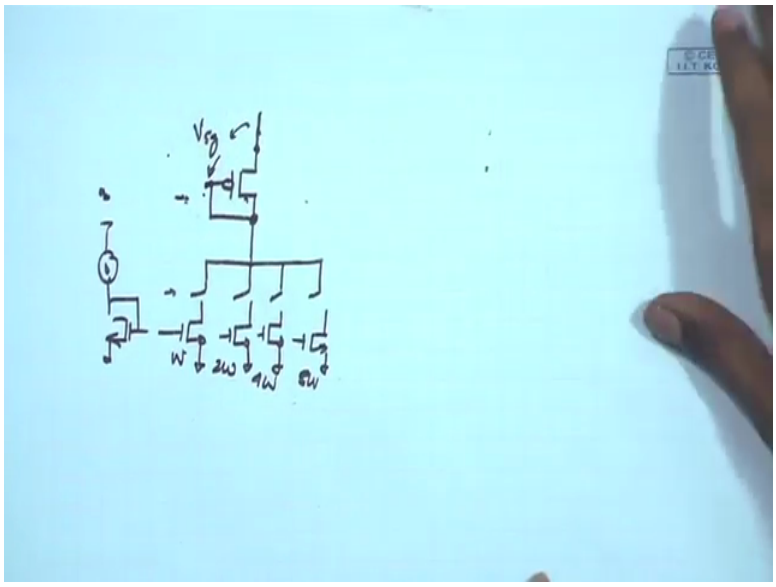

So, here I have drawn a structure which is generally termed as a pseudo NMOs gate. So, this kind of scheme can be used for implementing digital logic, but here we are using this particular structure to implement a desired voltage drop between the source of this PMOS and the gate of this PMOS and we are going to use these 2 terminals as effective as effective battery which will be the voltage developed across the source and gate of this PMOS can be used an effective battery basically we are going to connect this particular source terminal for example, at the output point and the gate terminal will be connected to the gate of the MOSFET.

So, that as compared to the output point we are having a V sg drop between this point and the gate of the MOSFET likewise for the other side also we can do the same we can connect the source terminal of this particular circuit at this point and the gate of this PMOS can be connected over the gate of m 2. So, that as compared to the input point we are having an effective potential drop between the input and the gate. So, that the potentials arriving at the gate are slightly lower as compared to the potential at this point and the output point that will basically help us in shifting the resistance towards lower values, because the effective gate potential will be lowered as compared to what we have at the V in and V out. So, the strategy will be that we will try to make the resistance for highest possible value and then have an option for tuning this voltage.

So, that we can reduce it intentionally so, the baseline transistor series transistor they will try to make it offer very high resistance values while keeping the option for pulling it down. So, by adjusting these potentials we can try to pull it down.

So, let us look at how by tuning some of these switches drawn over here we can tune the V sg. So, as we know if we have these transistors operating in sub threshold region suppose these are transistors are implementing some kind of current source mirroring a very small current. So, we can ensure mirroring of very small current of the order of say sub nanoamperes such that the total current even summed up with all these 4 transistors is very small flowing through this PMOS.

As a result the V sg developed of for this PMOS will be logarithmically dependent upon the current, because we know that if the total current is very small the V sg will be logarithmically dependent upon the sub threshold current. Or in other words the sub threshold current flowing through the MOSFET depends exponentially on the V sg of the

MOSFET. As a result if we are controlling the switches and we are making these transistors binary weighted w 2 w 4 w and 8 w we can program the total current flowing through this bank in a linear fashion and as a result the V sg can also be controlled in a logarithmic fashion.

So, if we are adjusting these switches. So, depending upon which switches you are turning on based on a binary 4 bit word we can control the total amount of current flowing through the PMOS another result the V sg also gets controlled. And hence, this logarithmically control V sg is going to once again control the resistance almost you know linear fashion you are going to have a linear range of resistance which you can tune by using the switches over there. So, this is one way in which you can insert a effective battery between these terminals and the gate and hence control this battery by controlling this tuning options it is switches over here this in turn controls the effective resistance coming between this V out and V in terminal.

So, we will see in simulations also that incorporate these are kind of tuning option can help us in obtaining a wide range of resistors values through the use of this control switches. So, this is just another example how to address the practical issues in silicon how to address the variability and time dependent drifts in the resistance that we are trying to create for our circuit any question. So, we can proceed towards the next analysis which is a frequency response for the differential case we have just looked at the DC biasing and we try to arrive at a possible scheme where we are not violating the frequency response, we are not violating the noise constraints we are also ensuring robust operation by incorporating tuning options.

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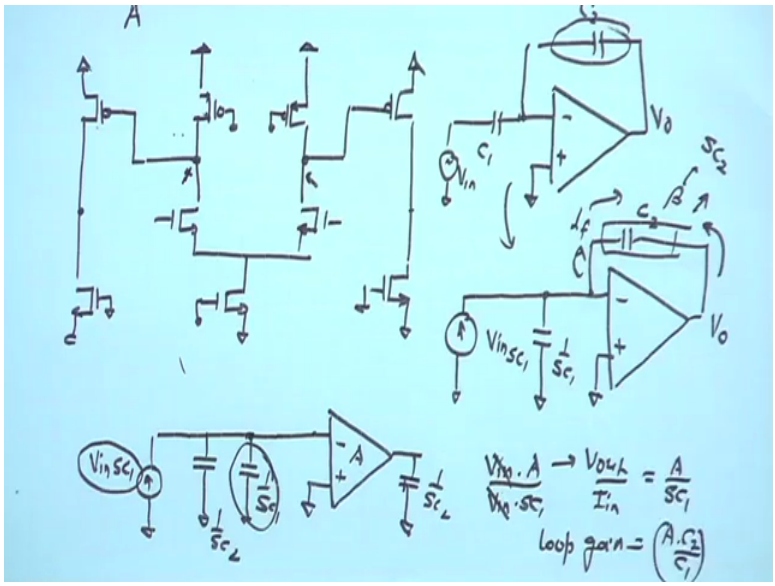

Now, next we are going to look at the differential frequency response once again coming back to our differential amplifier circuit for the fully differential operation considering the common mode to be DC we are ignoring the common mode circuit and . So, we are back to our fully differentials circuit and for overall differential gain we know that from the input to the output we have gm r o whole square gain. And we also need to find out the critical poles in the circuit which are going to be at the first output nodes first stage, because here we have equivalent it is given by r o by 2.

Remember for the differential mode operation this point will be easy ground for the differential pair as a result these are also acting like the common source amplifier with current source load. As a result the impedance over here for the differential operation will be just r o by 2 r up r will r down both of them r o and assuming both of them are closed or similar r o by 2 like whether the output point anyway they are acting like a common source amplifiers with current source load as a result the overall impedance over here is also going to be r o by 2. And we also we can find out the overall capacitances connected at this point.

So, we can look at the overall parasitic capacitances coming at these 2 points and that is that is going to give me the final parasitic r c value and hence from there we can calculate the overall poles for this transistor level circuit. So, we also looked at the feedback operation that we are applying over here. So, we need to look at the block level

also that how those feedback elements can come into picture to determine the overall loop gain. So, this is giving you the open loop gain of the stand alone amplifier we need to incorporate the loop gain curve because of the feedback operation.

So, let us go back to the block level description of our feedback amplifier again I am reverting to the single ended topology just for simplicity of the analysis and let me call this c 1 c 2 and you have the input signal over here I am ignoring the large r for the AC operation. Now here we have seen we have argued that this is a shunt-shunt topology because you are mixing the feedback signal in shunt with the input signal. Therefore, it must be current mixing. And therefore, I need to convert this input signal into an equivalent current source.

Now, here we have c 1 effectively providing the z 1 and therefore, if we apply the venin then we try to convert this into an equivalent current source I need to use this c 1 as the corresponding source impedance or other one upon S c 1 as the corresponding source impedance. And therefore, the resulting current will be V in upon z 1. That means, V in times S c 1 is our resulting current source I will make my current source as V in times S c 1 and I will also put the impedance over here as one upon S c 1 this is the input impedance and then I have the c 2 forming the feedback connection.

Now, for the feedback circuit if I look at the feedback configuration this is shunt-shunt and for opening the loop for a shunt-shunt configuration this is my feedback network this is the feedback element which is sensing the output voltage V out and providing the feedback current. So, let me draw one more step let me complete one more step and then open the loop. So, here this c 2 is sensing the V o and is providing us the feedback current I f that what we have seen earlier also. And therefore, we need to figure out the open loop circuit considering this shunt-shunt configuration.

Now, in order to do that this is our feedback network looking from the input port of the feedback network remember this is the input port of the feedback network because it is sensing the output voltage over here the other terminal of the feedback network is having shunt connection therefore, I will open circuited short circuited while opening the c 2 therefore, the in the equivalent open loop amplifier I have one upon S c 1 I have.

The V in times S c 1 while opening this feedback loop looking from the output side this was shunt connection for the shunt connection we need to short circuited therefore, I will

put an impedance one upon S c 2 over here from output to the ground. So, whenever we are opening the loop for a shunt-shunt configuration looking into the input port of the feedback network other terminal is shunt and therefore, we put a ground over there.

So, we have one upon S c 2 coming over here likewise looking into the output port of the feedback network this is the output port of the feedback network where you are having the I f going into the feedback network the other end is once again shunt connection we are sensing the output voltage another result we while looking into the output port we put another ground over here another result we get one upon S c 2 as the equivalent load impedance coming because the feedback network effectively we are arriving at an at the open loop equivalent circuit and we are incorporating the loading effect of the feedback network on the main amplifier.

Now, here if we look at this resulting open loop equivalent circuit at the input port we have combination of one upon S c 1 and one upon S c 2 if you look at the source for the source this is acting like a parallel combination and which one is larger in order to get larger gain, but we have seen is we have giving one upon the c 1 was supposed to be larger therefore, in the impedance if you look at it the overall capacitance or overall impedance over here the one upon S c 1 being larger is going to produce smaller impedance whereas, one upon S c 2 is going to produce lower impedance.

So, in terms of impedances if I look at the a complex impedance coming because of these 2 capacitor the c 1 is dominating and therefore, we will assume this to be the dominant component this may not play an important role with respect to c 1 and therefore, if we look at the overall voltage signal developed at this point for the open loop we need to find out the overall A beta for that we first of all need to figure out the output voltage over here and from there we need to find out what is the feedback current that is the overall operation right.

So, the A that is the open loop gain basically the current to voltage gain multiplied by the feedback factor which is the voltage to current conversion factor obtained by this feedback network that is known to us. So, what is the voltage of current conversion factor that is already known what is that this is a voltage what is the I f produced by this feedback network by sensing this voltage.

That is just V o upon the z of this impedance and that is just S c two. So, our beta is known that is just S c 2. Remember you want to find out the feedback factor for the shunt-shunt case we need to put a ground at the output port of the feedback network apply a voltage signal over here and then see what is the resulting current.

Why do we put a ground at the shunt connection? Because remember this is acting like a voltage to current converter, So, this feedback network is sensing voltage and providing you current as a result we are trying to estimate the gain basically voltage to current conversion gain or voltage to current conversion factor for this voltage to current converter element. And whenever we are trying to categorize a voltage to current converter let us call it above it to current converting amplifier we need to put a short circuit at the output, because that is the best case for the voltage to current converter when you have 0 load at the output.

Likewise if you are finding out the voltage to voltage gain or a voltage to voltage amplifier or a voltage to voltage converter the best case for a voltage a voltage converter is open circuit when the out voltage amplifier is not loaded by any external load the overall gain is maximized. Therefore, for assessing the overall voltage to voltage conversion factor we would open circuit the output port of the voltage to voltage converter. And likewise while assessing the conversion factor for a voltage to current converter likes this feedback factor we would short circuit the output node. So, that the feedback; FAC feedback network is not loaded by the amplifier.

So, we are trying to factorize this feedback network that given a voltage signal over here what is the corresponding current provided by this feedback network. So, what is the voltage to current conversion factor for this feedback network for the shunt-shunt configuration? So, for that while applying a output voltage at this input terminal of the feedback network the other terminal will be grounded and we will try to see what is the resulting current going through this feedback network and therefore, we ground it and look at the current and we get the factor S c 2.

So, that is the beta and the remaining job is to get the a from here overall current to voltage gain from here and for that we have to also note that the current by definition in this case is V in times S c 1 this is the current that we have defined. So, this is the current we know that the voltage as we are saying this is the dominant impedance one upon S c 1

the smaller one another result the voltage at this point which is going to be V in S c 1 gets cancelled with another c 1 that is not going to come into picture and then you have the overall gain which is just given by the A of this amplifier.

So, this amplifier is having some overall gain we have just seen what is that gain of this amplifier overall that is g m r o by 2 the whole square that is the A of this amplifier because this inherently this amplifier is the voltage to voltage amplifier. So, the gain from this to point to the output is anyway the A of this amplify that you are using. So, that gives us V in times A as the final voltage over here this is the final voltage this is the V out right. So, what is?

This is the V out we need to find out V out upon I in therefore, what is V out upon I in is V in S c 1 therefore, the V out upon I in that is the open loop gain of our current to voltage amplifier is A upon S c 1 this is clear, because effectively we are modelling this as a. Current to voltage amplifier we are treating this as a current source. So, we are looking at the output voltage output voltage is V in S c 1 multiplied by one upon S c 1 that is V in only V in times A because this is a our amplifier.

So, V in is the signal appearing here times A that gives us V in times A voltage over here, but that is a voltage I want to get the voltage to current gain of this overall amplifier our current by definition in this case is V in S c 1 we have arrived at the equivalent current source by the venin equivalent derivation. So, this is the V in S c 1. So, by divided and we get V out upon I in which is a upon S c 1 that is the open loop voltage to current gain of our shunts-shunts amplifier and we need to multiply beta with this.

So, in order to get the loop gain which is I would say let us just name this loop gain is equal to this times beta that we have already found out that is going to give me A times c 2 upon c one. So, this is the overall loop gain of the amplifier therefore, A times c 2 upon c 1 where my definitely my c 2 is smaller than c 1 in order to get larger gain. So, my overall loop gain is definitely smaller I have A times c 2 upon c 1 in order to get a 100 gain I would keep c 2 to be you know 100 times smaller than c 1 in order to get a 50 gain I will keep this hundred times smaller than 50 times smaller than c one. So, as come to the open loop gain my loop gain is definitely smaller and that will raise concerns regarding the precision and accuracy that you want.

So, here which is the loop gain factor is smaller we know that in order to get a good precision we need to have the loop gain that is you are A beta of the overall amplifier sufficiently larger than one if you want say 7 bit precision we have discussed in the very beginning the precision requirements. So, if you are going for 7 bit precision; that means, we want this overall loop gain A upon 1 plus A beta.

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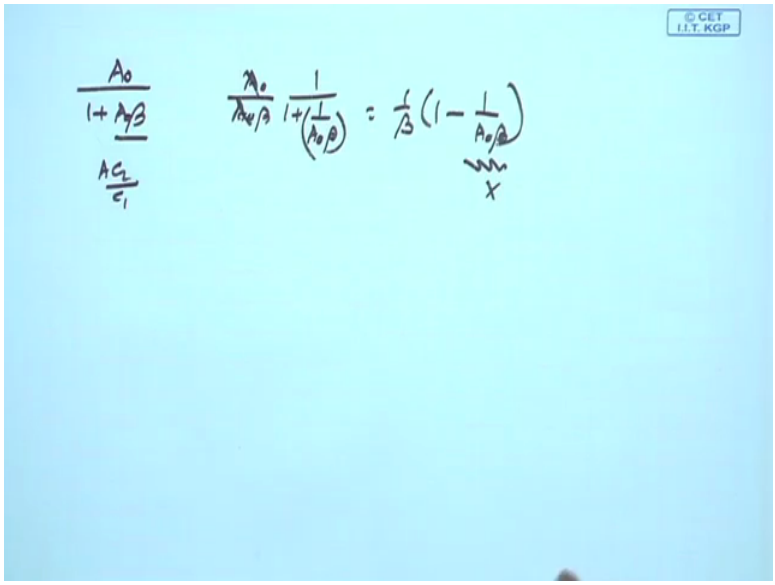

So, A beta is what we have just found out which is the loop gain given by A times c 2 upon c 1 let me call this do not mix this number. So, the A is the open loop gain. So, let me call this A naught; A naught and beta A naught beta. So, this A is the amplifiers gain. So, let us not mix these 2 quantities.

So, I am just considering the general case of a feedback amplifier that a naught beta is the loop gain we have just found out and in that case it is in our case it is A times c 2 upon c 1 where a is the gain of our fully differential amplifier 2 stage and c 2 upon c 1 is giving as the ratio of the capacitors now this to be much greater than 1 for theven representation we would like this to be at least hundred times greater than one why because if I take out these factors a naught beta we are basically left with one upon one upon a naught beta and if a naught beta is much greater than one this is a small quantity one upon one plus x I can jump it up. So, this becomes one upon beta one minus one upon a naught beta

And in order to get a good precision I would not like to depend upon the second term I would like to be my gain would like to be determined by only beta and not by the second term because this term is you know highly parameter dependent process dependent that can change from time to time can change from device to device.

So, this is not a very precise component. So, I do not want to depend on this and therefore, in order to get one percent precision I would like this quantity to be less than point 0 0 one and that is the reason I would like to have a naught beta much greater than you know hundred. So, at least a value of hundred will be required to obtain a 7 bit precision or one percent precision, but we have seen is one bit precision means 7 bit accuracy for the digital domain, because if you are having 7 bit means you are trying to have or trying to have one twenty 7 different levels in the data close to you know hundred. So, you want to record data bit hundred levels of precision.

So, therefore, you do not want even one percent of corruption in the data otherwise higher 7 or even higher number of bits in the data is meaningless. So, in order to have one bit a one percent precision or close to 7 bit accuracy I would like this quantity to be sufficiently higher than hundred at least around hundred. So, that one upon a naught beta is less than 0.001; 0.01 sorry and that would mandate that this A naught is accordingly much larger.

So, the beta is chosen as one of one hundred to get a close loop gain of around 100 that would imply a naught at least and the power of four. So, the close the open loop gain a naught of my differential amplifier that I am sitting is looking at will be at least 10 power of 4 or higher. So, that is the limitation which would be coming because in this case my overall loop gain is diminished by this factor of c 2 upon c 1 larger I try to get c 2 upon c 1 lower will be the A naught beta and in order to get larger a naught beta I would like to have larger A for this pull the differential amplifier that is one constraint we need to be aware of.

So, now we have obtained expression for the loop gain A naught beta and next we make to look at the overall poles in our frequency response. So, in the open loop amplifier we need to look at the critical nodes and we have earlier also we have discussed that in this overall circuit we have the critical nodes coming at the output of the first differential stage and output of the second differential stage and likewise we can look at the r equals

these 2 points and find out the poles and we will follow the similar analysis will be looking at the overall frequency response coming from the 2 pole system and trying to look at the miller compensation for getting a an improved phase margin and from there we will look at another concept of 0 how the application of miller compensation creates additional problems introduces 0s in the circuit and then briefly we will discuss a couple of ways to address that issue and ensure overall stability for the differential feedback loop so;

Student: Sir, what is the typical value of open loop A?

A naught can be a can be very large which depends upon your design. So, if you look at one eighty nanometer technology you can go to values of A which are even 10 to power of 7 10 to the power of 7 also possible, but for that you may need to use special techniques. So, there are some ways in which you can have very large gain without relying only on r o.

So, we will study some techniques like gain boosting where rather than relying only on r o you can incorporate some additional components in form of amplifiers only in the main amplifier to boost the gain to very high values. So, high values are possible, but it adds more complexity if you want through keep your design simple and if your precision requirements are relax then probably 10 to the power of 4 10 to the power of five is achievable with you know without adding more complexity, but we will study some additional techniques also through which you can enhance the gain by order of magnitude and go to 10 to the power of 7 gain also any other questions in.

I hope the feedback operation is clear how we are opening the loop and looking at the amplifier as a current to voltage converter then finding out the current to voltage gain and then multiplying it with the feedback factor beta to get the overall closed loop overall a beta that is open loop response that part should be clear only thing that we have to take note of is that we are using this amplifier overall as a now voltage to voltage amplifiers, but the feedback topology the shunts-shunts.

So, we are transforming the input signal into or input source into an equivalent current source and then doing the rest of the analysis. After that if you assume that this is the given source and this is the topology from here this overall derivation should not be a

problem only thing is initial steps involved in transforming this input signal as a voltage to and personal as a current.