Analog Circuits and Systems through SPICE Simulation
Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture - 20
Frequency Response Of Differential Feedback

Welcome back. We are going to start from where we left the fully differential operation and the DC biasing and stability analysis for the fully differential operation.

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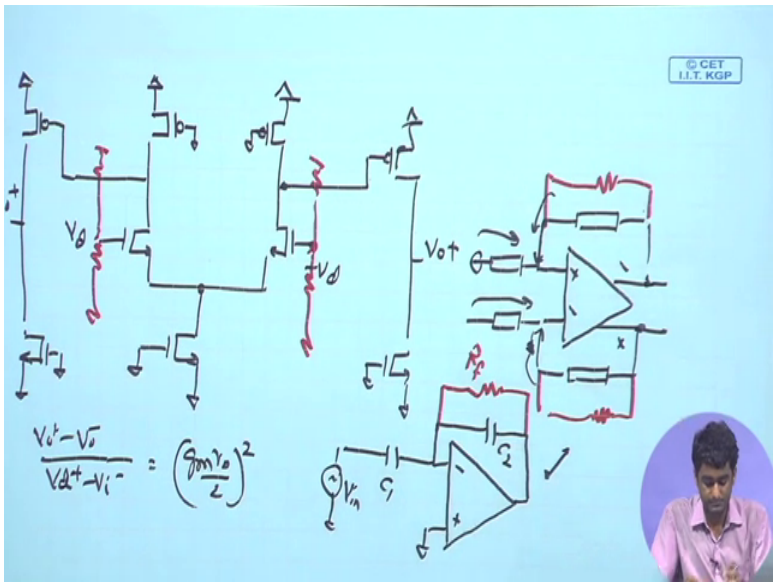

So, here summarizing what we started with, we look at the common mode feedback and we did the stability analysis for that and our assumption is that the common mode feedback loop is having very low bandwidth it is not propagating any significant signal content. As a result we are assuming that the voltage provided over here by the common mode error amplifier is almost constant it is just a DC bias.

And therefore, we are putting in AC ground over here in the AC equivalent circuit even if there is a significant common mode at the input the differential amplifier also ensures that the common mode at the output is sufficiently small, so the common mode signal anyway will be small. But apart from that the bandwidth of the error amplifier can be made to be intentionally very small so that it does not propagate any significant component of the common mode signal as a result you will just have a DC bias point.

So, that is the reason by we have put an AC ground over here assuming that this is relatively constant DC potential provided by the common mode feedback circuit. And we have the differential signal V d minus V d at the input and we just wrote down the expression for the overall gain for this particular amplifier from the differential input to the differential output V o plus minus V o minus upon V i plus minus V i minus so that is having gm ro by 2 whole square. And we need to look at 2 things what is the first analysis of the close loop stability for that we need to look at the feedback operation and the stability analysis for this feedback operation and second thing we also need to check the DC bias, just like we did for the common mode feedback.

So, let us start with the DC bias and look at how to establish an appropriate DC bias point at the input nodes of this fully differential amplifier. So, remember that using the common mode feedback we are assuming that we have already set the output DC bias for to an appropriate value and also the DC bias at the output of the first stage have been set to an appropriate value a desired value.

Now the next question is how do we set the input DC bias. So, if we recall some of the very commons steps that you might have taken in an under that with lab to bias differential amplifier or a common source amplifier this using a voltage divider. So, for differential amplifier possibly we can think of using a voltage divider, you can connect and voltage divider to get an appropriate DC bias point that you want over here and then you can use the capture a feedback as we have discussed in the beginning.

But once again what is the problem with such bias? The biggest problem will be the noise contributed by these resistors, because ultimately these resistors are going to give you an input referred noise which is going to come directly at the input port and it is going to interfere with your amplifiers operation and therefore, direct resistive biasing may not be a good option. Likewise it will also degrade the input impedance so here putting the resistive divider, so degrade the input impedance rather than the signal coming at the gate to the capacitor you are now having low pass filter form with this with the help of this resistor.

So, it is good to affect your frequency response input impedance and noise and therefore, using these resistive dividers is may not be a very good option. Apart from that this will also wait some of the static power because if you are having a voltage divider unless you

are having very large resistances is mega ohms range it may bunch few micro amperes of power and that can also lead to wastage. So, rather than using voltage dividers at the input port we are going to take help of already established DC bias point at the output to bias my input nodes and for that we are going to use resistors in parallel with our feedback element.

Let us see how does this help and how does this not violate our other constraint. So, we have to choose appropriate values of this R and make sure that it is helping which is establishing the appropriate DC bias point at the input terminal of our differential amplifier without violating the frequency response or the noise constraint of our overall amplifier. So, the in a very beginning we have said that we do not want to use resistive feedback we do not want to use R 1, R 2 and one of the main reason is that it can lead to lot of noise because R 1 whatever noise is being contributed by R 1 that will get amplified by the amplifier and it can increase the input the overall output noise of the amplifier and also the equivalent input referred noise as a result will be bad. So, that was a starting point why we chose the capacitive feedback.

Now in this case we are saying that we are again going to take help of these resistors in the feedback network to establish an appropriate DC bias point at the input. So, let us see how does that help us in first of all establishing DC bias without positive noise constraint and then look at the frequency response criteria. So, for the analysis I will look at the single ended version because that is simpler to analyze and visualize as well. So, I will stick to the single ended version where I am having the C 1 C 2 for the feedback realization and I am having a feedback resistor Rf for the DC bias. You are having the input signal applied here V in you can call it C 1 you can call it C 2. So, and just going to use the single ended version for analysis results remain valid for the differential case also.

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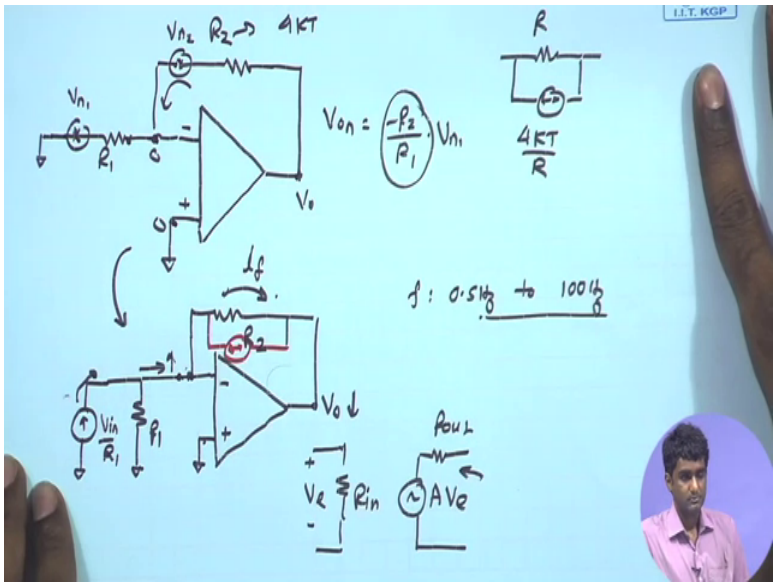

Now, if we look at the overall operation of this inverting amplifier and consider the role of Rf we can visualize the role of Rf by is a constructing a feedback network even resistor. So, let us see if I have the resistive elements in the feedback what are the roles or what are the contribution of these 2 resistors R 2 and R 1 in the overall noise of the output amplifier over here. So, we can analyze the overall output noise by taking superposition of that noise contributed by these 2 resistors. So, first of all let us see what is going to happen with R 1. So, R 1 has its equivalent noise I can represent it in form of a noise voltage V n 1 suppose we do not have any signal we are just considering the contribution of the noise of these resistors and trying to see how does it translate to the final output.

So, first I will consider the effect of V n 1 and we can see that V n with in nothing is, but it is behaving like an input signal which will ultimately get multiplied by this gain factor R 2 upon R 1 because this is in AC ground or the DC potential this will also be AC ground therefore, you have V n 1 upon R 1 signal coming in and that current goes into R 2 and therefore, you have this 0 plus 0 minus V n 1 upon R 1 times R 2 voltage coming over here. So, von output noise which is going to be minus R 2 upon R 1 times V n 1 therefore, it gets multiplied by the gain factor that you have chosen if you are choosing a gain factor of say 50 or 100 we can see that the R 1 vice will also you know get magnified. Whereas, if I look at R 2, R 2 if I am looking at the overall noise contribution setting V n 1 0 and just considering V n 2 V n 2 appears as it is. So, if I consider this to

be 0 and then look at only V n 2 that does not get amplified by this circuit so that remains as it is and therefore, you know the noise contribution by this feedback resistor will not be you know amplified as compared to the signal, signal is getting amplified by the factor R 2 by R 1, but the noise contributed by the feedback resistant that is the resistor R 2 that is not getting amplified.

So, this amplifier will amplify the input signal and V n 1 by the amplifier gain, but not the noise contributed by R 2 therefore, the signal to noise ratio would not be slaughtered significantly by the noise contributed by R 2 also if we look at the feedback configuration we can visualize what is the role of R 2. So, as we said this particular feedback is acting like a shunt-shunt feedback, you have an output signal which is voltage V o which is being sensed by this feedback element R 2 and it is producing an effective signal I write now I am not thing whether it is the current signal or a voltage signal it is producing an effective signal which is going into the input node and it is getting mixed with the same node where the input signal is coming.

So, whenever there is a combination of feedback signal and the input signal at the same terminal there is a shunt connection and we know that it is going to be a current mixing because current mixing happens at the same node you have to subtract voltage then it happens at different node. So, if the feedback signal is coming at the complementary node as compared to the applied input signal then it is series feedback the input quantity is you know subtracting from the feedback quantity because the feedback terminal or the feedback signal respect to the complimentary terminal.

But, here we see that the feedback signal respect to the same terminal as the input signal therefore, the input quantity has to be treated as current and as a result if I look at the role of R 2 it is basically providing a current feedback at the input point. In order to treat or analyze this feedback amplifier we need to analyze this as a shunt-shunt amplifier and need to analyze a given input source also as a current source.

So, even though we are using this amplifier topology as a voltage to voltage amplifier, but the mechanism is of a shunt-shunt amplifier therefore, if I look at an applied input source over here V in we would like to first convert it into its equivalent Thevenin current source. So, let us assume that we are having a input signal V in. So, I can represent that as an equivalent current source V in upon R 1 and its equivalent source

resistance becomes R 1 right, if you are having V in in series with R 1 we can convert its it to its equivalent Thevenin equivalent current source and the corresponding source resistance R 1 then it goes into the input of our amplifier and the R 2 basically now can be seen as mixing current sensing voltage and mixing current.

Therefore, you are having voltage sensing in current mixing at the input port shunt at the output shunt at the input. And once again if you look at the polarity if the input current is increasing; that means, the voltage the negative terminal is going to increase in the amplifiers input. As a result the output voltage over here is going to reduce because it is the input is the negative terminal if this increases because of an increase in the input signal current the voltage over here is going to reduce as a result the current flowing from this input point to the output is also going to increase that is the I feedback flowing through R 2 is also going to increase.

So, if the input current is assumed to be increasing we see that the If also increases increasing input current increases the voltage over here whatever is the over input impedance this input current increasing resulting increasing input voltage that will result in reduction in the output voltage because it is a negative terminal 0 minus this voltage increasing will lead to reduction in the output voltage. And as a result will have the increase in If that is the feedback current flowing from the negative terminal of the amplifier to the output as a result we say that the feedback current is increasing as the input current is increasing.

Therefore, subtracting from the input current in effect if it is an op-amp base on CMOS circuit we can assume that the input current going into the regular terminal almost 0 therefore, the I in is almost similar to If whatever is the input current provided by the source into the amplifier if I assume that this resistance can be clubbed with the source whatever is the input current provided by this particular source entirely goes into If. That is the current feedback operation we can visualize. As a result if I need to look at the overall contribution of R 2 I need to look at its equivalent current contributed as a noise.

So, we know that if I have to look at the noise voltage of R 2 it is 4 KT are; however, if we look at the equivalent current I can represent the equivalent current noise of a resistor. Once again by taking the Thevenin equivalent and writing it as 480 upon R and as a result the noise current contributed by R 2 also reduces as the value of R 2 is increased.

So, they have a very large R 2 in the feedback the noise current contributed by R 2 in the feedback will be reduced as compared with the feedback current. And as a result we can say that a larger value of R 2 effectively is going to diminish the contribution of noise current contributed by the feedback element to the input point therefore, the current mixing will not been input so much by the noise current contributed by R 2.

So, looking at this feedback topology we can assume that the R 2 if you are making it large even then because of this current mixing topology it will not going to corrupt the input signal over here, it is not going to significantly corrupt the feedback current coming through the resistive path. As a result what we can conclude from here is that because of the current mixing topology current feedback terminal over here a large twice of R 2 does not corrupt the feedback signal coming from the actual a capacitive feedback and therefore, is not going to significantly corrupt my output signal in the overall closed loop feedback operation .

So now let us see; what is the role of this R 2 in frequency response. So, we have just looked at the overall noise response we also need to take care that it is not interfering with the specification of frequency response that we have started with. So, we has looked into the high level specification and depending upon the signal V, estimated that our signal content is going to be in the range 0.5 hertz all the way to around 100 hertz and putting this R in parallel bit see in the feedback path should not interfere with this we should still be able to satisfy this condition. Let us see whether that is getting sacrificed if yours then what is the value of R 2 needed in order to meet these criteria.

Student: (Refer Time: 16:29) voltage across R 1 is 0, so can we remove the R 1.

You know ultimately this current this is inherently a voltage to voltage amplifier this op-amp is a voltage to voltage amplifier. So, in order to amplify signal giving the voltage over here, so this current ultimately produces a voltage that produces a amplified voltage over here, but overall this configuration is shunt-shunt. So, this op-amp along with the resistive feedback is producing or is implementing current to voltage amplifier.

So, we have seen in the feedback discussion that the op-amp can be used to built any of the four topologies of feedback it can be shunt-shunt, shunt-series, series-series, series-shunt. So, it can be used to implement current to voltage amplifier also although inherently this triangle that is op-amp is basically taking a voltage at the input input DC

in the voltage at the output. So, if you model an op-amp it is modeled as the R in at the input point and you are having some output resistance R out and you are having A times the V e where V e is the voltage across its input parallel. So, this will be the model for in op-amp because ultimately it is amplifying the voltage appearing across the 2 input terminal it has some effective output resistance. So, this is how the model an op-amp, but I can implement any one of the four topologies of the feedback using op-amp and in that case the overall amplifier has to be modeled corresponding to the topology.

So, here I can model this amplifier as a current to voltage amplifier for that the in factories amplifier. So, I can ask you to find out the overall 2 port network model of this amplifier as a current to voltage amplifier, you should be able to do that you should be able to find out the equivalent input you know resistance the current to voltage gain and output resistance if I have to customize this as a current to voltage amplifier. So, although using this op-amp to build my circuit, but effectively topology by this is current to voltage amplifier. Any other question, we proceed towards the frequency response.

So, for the frequency response once again I have to go back and add my original feedback components that are my capacitors. So, let us do that.

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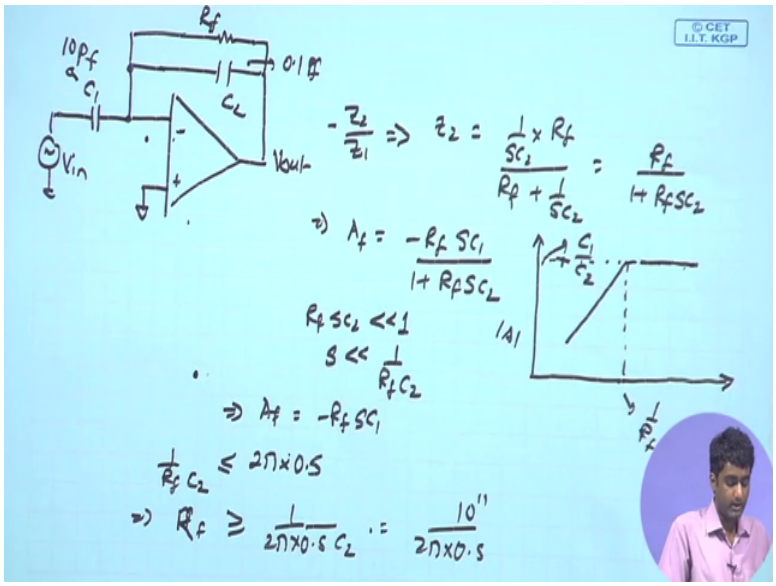

Once again I am using only the single ended version just to keep the analysis simpler, call it C 2 this is the overall circuit and here we know that overall response will be given by Z 2 upon Z once. So, I can just write it down as Z 2 upon Z 1 minus sign which is

where Z 2 is parallel combination of Rf and C 2. So, I can find out Z 2 first which is 1 upon SC 2 parallel Rf upon Rf plus 1 upon SC 2 and this is going to result in Rf upon 1 plus Rf SC 2 and therefore, the gain is the closed loop gain is minus Z 2 point Z 1. So, Rf Z 1 is 1 upon SC 1. So, you have SC 1 upon 1 plus Rf SC 2.

So, what kind of transfer function do we see here because of the Rf you are going to plot this as a function of frequency what is the standard also I get. At very high frequencies the Rf SC 2 term in going to be much larger than 1, as a result I can ignore this one with respect to this Rf SC 2 and therefore, what is the as a function?

Student: (Refer Time: 20:40).

A going to be my required the desired gain C 1 upon C 2 minus some or design just taking the mod of that. So, this is your mod A, so at high frequency I get C 1 upon C 2; however, if I go towards lower and lower frequencies where S or where Rf SC 2 is becoming much smaller than 1 or S will becoming much smaller than Rf C 2, 1 upon Rf C 2, the 1 the Rf SC 2 term will be you node with respect to 1 in that case and for that scenario A f will just become minus Rf SC 1; that means, if I look at the modulus or the magnitude of the gain it will be dropping towards lower frequency as why good words lower and lower omega the gain will also become lower and lower.

So, what is the sequence thing beyond which it is happening? It will be the 1 upon Rf C 2 beyond that you are having the drop because of the high pass operation because of the whole coming over here. So, we are having an overall high pass transfer function resulting from this Rf and C 2 combination. And we have just regard that in order to allow our neural signal to pass through amplifier you must make sure that this capacitance is higher than 0.5 hertz. So, I must make sure that or lower than lower than greater than or equal to 1 upon Rf C 2 that must be smaller than or equal to must be smaller than or equal to our minimum signal frequency which we have said 2 pi times 0.5 hertz, and that would implying that Rf must be greater than sorry Rf must be greater than one upon 2 pi 0.5 times C 2.

Now, let us see what is the possible value of C 2 that we get from here? So, we have seen that the C 1 C 2 values how I given to be, how are they going to be determined and how are they going to be constrained. So, in order to get larger gain we would like to has C 1 larger and C 2 small and suppose we target again of say 50 to 100 from a single stage in

that case C 2 is hundred times smaller than C 1 and bulbpark number the maximum values of capacitor that you would have in a single channel suppose it is ten picofarad is also on a higher side in general it can be further smaller.

But suppose we are choosing C 1 to be 10 picofarad and as a result C 2 is around 0.1 picofarad we have stressed numbers. So, in that case C 2 is 100 femtofarad and once again we have to make sure that this C 2 the smallest value of C 2 that we choose is sufficiently higher than the parasitic capacitance of the MOSFETs in the operation amplifier otherwise you will not get a precise scheme. So, that will be the lower limit on C 2 if you want to just recall that.

Now, in that case I have to make sure that Rf is greater than or equal to 2 pi 0.5 times to the power of minus 11, so basically a huge number. So, this is something close to or higher than then power of (Refer Time: 24:12) attend and this words 10 Giga ohm range therefore, Rf must be greater than 10 Giga ohm it is a huge number and therefore, we have to see whether it is at all practical to implement such a huge number using passive resistance. The answer would be no definitely because passive resistance at the max they can achieve values of around a mega ohm, few mega ohm is feasible, but beyond that achieving such large values of Rf will be very you know difficult, this value is definitely impossible using passive resistance. So, rather than using passive resistance people have explored other techniques which using transistors we can implement such large values of Rf we will look at techniques where transistors operating in sub threshold region very close to the off condition can be used to implement such values of Rf. Rather than relying on passive resistors we will be looking at how to implement such large resistor value effectively large resistor values using transistors.

You just look at one particular example and try to see how such a high impedance value can be obtained from a combination of resistors transistor, any question do I proceed. So, here we have just looked at the frequency limitation and trying to make sure that the Rf value that you are choosing is in line with our frequency specification bandwidth specification of the amplifier and then we arrived at this huge value. And then we have to look at the circuit implementation how do we really go ahead and implement these using transistors.

And another point that we noted was that you have large Rf value if you look at the equivalent feedback contributed by Rf that will be small. So, we are looking at the equivalent noise contribution or noise current contribution. So, if you are implement taken using large you are using such a sub threshold using transistors to implement such an Rf the overall noise current will also be small because of the does not upon R dependence of the noise current.

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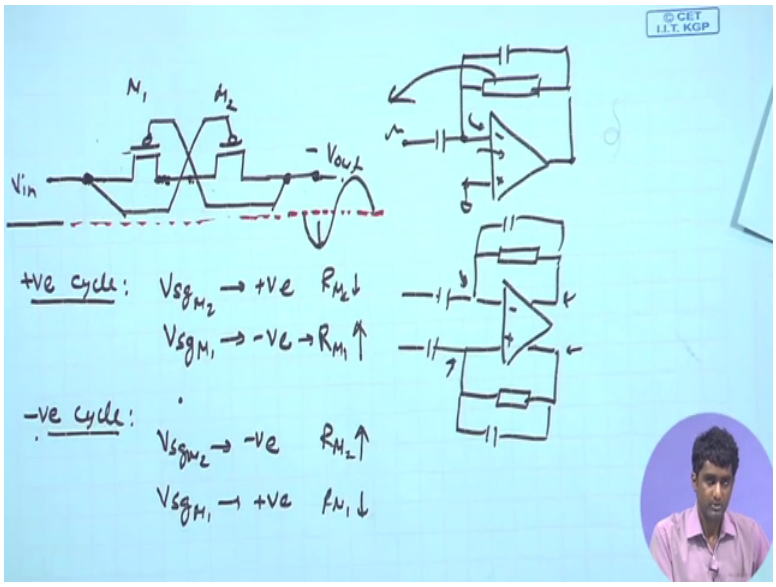


So, now let us look at the transistor level implementation of Rf and that you see what are the non idealities that mean to adjust. Any question before I proceed towards science to a analog implementation ok.

So, one of the implementations used in literature is a series combination of 2 MOSFETs I am using p MOSFETs where you can wherever I am drawing the dots they are having connectivity, where they are no dots means no connectivity they are just crossing points. So, the input signal is over here this is the input terminal of the amplifier. So, basically you can say the negative terminal of the amplifier or positive terminal of the amplifier and this is the input signal, the input point is connected to the gate of this particular PMOS, the input terminal of the amplifiers connected to the second PMOS here you do not have any connection.

Now if you look at our negative feedback configuration if we are having such in such a resistor realized between these 2 points and of course, we have this capacitor feedback.

So, basically we are building this large resistor using this series connected transistors and we also need to check what is the voltage conditions across these 2 terminals that are where you are going to have. Now at the input point we have some AC signal coming and it is capacitor coupling. So, we do have some input manute, input signal coming at this point and this point we have just established we are trying to establish a DC bias with the help of this large resistors. So, assume that you have a good DC bias established we know that the input of the in gates of the MOSFET devices which are forming the input terminal they do not sink in any current. So, there will be 0 current going into the input terminal. So, under DC condition we can assume that whatever is output DC potential the same DC potential will be available over here right because ultimately you have the negative and the positive terminal of the amplifier going into the gate of the MOSFETs of the differential amplifier as we have seen and they do sync any current.

So, if you talk about absolute DC values whatever is that DC value present at the output will be same as the DC value present over here. So, despite having very large resistor DC point to be even if there is a very small manute nanoamperes picoamperes of current flowing through this in long term in few seconds at least it will make sure that the DC potential as these 2 points are coming to be same. And that is a basic mechanism through which despite using very large resistor we get almost the required DC point over here same as the DC point which is available at the output.

For the fully differential case we know that we have established appropriate DC points at the differential output. So, in our fully differential amplifier we have differential output both of them are set to a required DC point, there is a common mode DC voltage and with the help of this resistor large resistor connected between the 2 outputs and the inputs we are ensuring that we are able to establish the same DC point at the input as well. So, you having minus plus and both sides were connecting the inputs with the corresponding outputs and of course, along with that you have the capacitor as well. So, on both the sides we are ensuring that the input DC points are equal to the output DC point which is said to the common mode voltage.

So, the output terminal the right terminal of this series connected transistor is connected to the output point of the amplifier which is going to have amplified signal level has compared to the input signal and here we have the left end of the transistors connected over the negative and the positive terminal which are acting as AC ground you do not

have much of a signal over here. So, as a result what we can say is you are going to have sufficiently larger signal at this point whereas, the other end is going to be relatively stable is not going to have much fluctuation over here.

So, we have to see what happens when the signal at the other end is going up and down with respect to the DC potential. Remember DC point to be what we are assuming is that the DC potential at this 2 point and the input points are same therefore, the DC level at the output point is also similar to the DC level at the input point. So, the DC levels are same because this resistive feedback has ensured that the DC point here and here is remaining same whereas, the signal is much higher you have a amplified signal at the output point as result with respect to the left terminal the right terminal going to have a sufficiently large signal swing. So, as the signal changes we can see how the effective resistance of this series connected transistor pair changes.

So, let us look at the say positive cycle when the signal is going high what is the condition of each of these transistors they call them M 1 and M 2 . So, when the signal is going positive we can see that the gate potential of M 1 is increasing whereas, the gate potential of M 2 is relatively constant. We know that MOSFET is a bi directional device, so the definition of source and drain depends upon the relative potential across the 2 terminals.

So, for a PMOS transistor whichever terminal is having higher potential higher ups look potential that is the source. So, for both these MOSFETs because this is for the positive cycle this is the higher potential this is the lower potential as a result the midpoint is also expected to be definitely higher potential than the V in. So, when the signal is going up this point as well as this point is higher than the V in.

Now, if I look at the condition of M 2, for M 2 therefore, since this is at the higher potential. So, this is the source terminals for M 2 and the gate of M 2 is V in and therefore, the V sg is becoming positive. So, for the positive cycle the V sg of M 2 is positive whereas, if I look at the condition of M 1 for M 1 also this is your source terminal because ultimately this is a higher potential this is a lower potential midpoint of that it may not be exactly the midway, but it is supposed to be higher potential than this one.

So, this is going to be the higher potential to the source terminal this is definitely lower than the potential over here whereas, the gate potential is higher. So, although the source potential is higher than the drain potential, but the gate potential is even higher than the source potential and therefore, the V sg of M 2 becoming more and more negative. So, V sg of M 1 is becoming negative. And therefore, the resistance of M 1 will be you can say R M 1 will be going up very strongly whereas, R of M 2 is going down.

This is a series combination so ultimately the overall resistance that is R M 1 plus R M 2. If the R M 1 is strongly going up and becoming relative is remaining relatively off because V sg is becoming more negative therefore, this is going to dominate the overall resistance between the 2 terminals and therefore, the effective resistance between the 2 terminals V in and the output point is going to be very high determined by the off resistance of M 1, is it clear. So, this is trying to keep this overall resistance very high despite the signal going up.

What happens to the negative cycle? So, negative cycle also we are going to just have the reverse condition by symmetry we will see when the signal goes down little bit, now for both the MOSFETs this is at a higher terminal higher potential as a result for M 1 this becomes a source for M 2 this is going to be higher potential than the other one because this is higher than the other extreme for the negative cycle.

So, for the negative cycle this is the source of M 1 this is the source of M 2, this midpoint is source of M 2 the V in becomes the source of M 1. Under that condition what we see is for M 1 the V sg M 1 is becoming slightly positive because V in is higher than the V out over here. So, this is basically your V out. So, V in is higher than the V out under the negative cycle, as a result the gate potential of M 1 is reading lower than the source potential therefore, it will try to get on it may not necessarily get on because it is I am not saying that the gate potential is lower or the V sg is greater than mod V t of the PMOS, but still the V sg is positive.

So, although it will be still is sub threshold region, region it is not completely on, but definitely it resistance will be reducing as the signal is going down. So, as the signal goes down down and down as compared to the DC line the gate potential of M 1 is reducing with respect to the input potential and therefore, the V sg is reducing therefore, the impedance of M 1 is reducing.

If I assume that this is in sub threshold region the resistance of M 1 will be reducing exponentially because we know that in sub threshold region the resistance of the transistor current for the transistor is exponentially dependent upon V sg therefore, as the V sg is becoming more and more positive the impedance of M 1 will be reducing exponentially.

Now if you look at M 2 to another hand once again we have the reverse condition the gate of M 2 is V in which is at higher potential as compared to the source because this is a source of M 2 which is going to be this is the lower than the V in because the voltage division you are definitely getting this point which is lower than V in. And as the input signal or the output signal becoming more and more negative we are going to have the overall potential over here becoming all the more lower because this is getting on therefore, this will try to connect these 2 points more closely as a result this potential will follow more closely V in therefore, this becomes closer to V in.

Because if you look at the simple voltage division because this resistance is much smaller now as compared to this therefore, this point will be closer to V in. As a result this potential is also you know getting as compared to the gate potential you are having 0 or negative V sg for M 2 and therefore, once again the V sg of M 2 in this case is negative and therefore, the R M 2 will be you know increasing exponentially R M 1 is reducing exponentially.

So, what we can see is that in the negative cycle once again the reverse (Refer Time: 38:28) resistance of M 2 becomes much higher and M 1 become must lower the series combination is going to be determined by well much larger one and therefore, the overall impedance over across the V in and V out become space height for the positive as well as negative cycle. And for the sub threshold operation since the impedances are going to be much smaller we are having a negative V sg for another MOSFET we can ensure much higher impedance provided by these MOSFETs.

So, even when the V sg is off the device will have some minimum leakage flowing through the drain and source. So, there is always an nonzero leakage current between the drain and the source that is what is going to give us a very large impedance value a very large resistance value and throughout the cycle whether the signal is going positive or negative we are ensuring that the impedance provided by the overall series combination

is corresponding to the off state impedance of the transistor and hence is would staying very high.

So, by appropriately choosing the channel length for example, we can also try to push the impedance higher and it has been shown that this kind of combination can be can help us in achieving resistance all the way of putting power 14 and power 15 here our target is 10 to power of 12. Definitely that is also achievable using appropriate device dimensions. The problem in this particular case if you are operating a sub threshold region we are not sure how to size these resistance values will be. So, here we are relying on assumption that this feedback component will be able to meet our bandwidth requirement Rf, we have trying to choose is such that it is not suppressing our desired signal content. If you are relying on sub threshold operation of the transistor to the empl to realize such large value of Rf it is going to be highly sensitive to temperature and process variation, sub threshold region because of exponential dependence of transistor currents on threshold voltage variation or temperature variation.

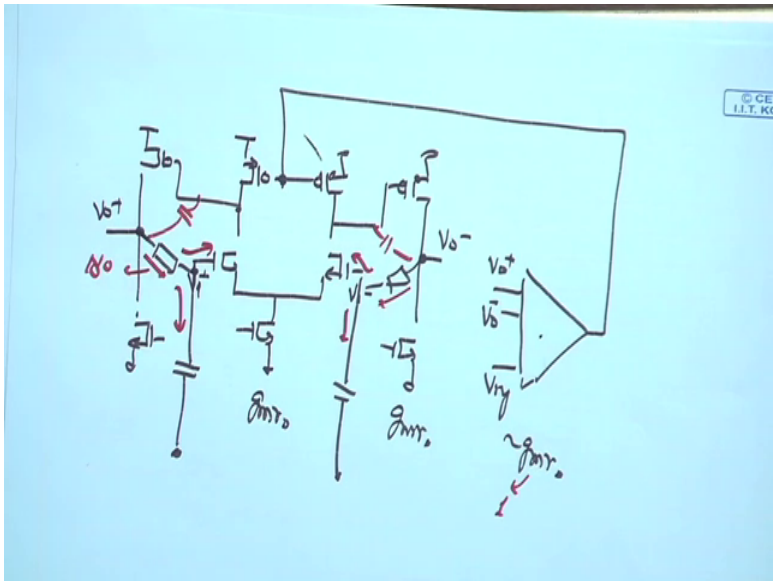
It can have very sharp or very strong dependence on temperature on process and as a result it will not be very well defined very well controlled in simulation you will be getting some value, but the actual implementation can give you the drastically a different value. And therefore, we may end up blocking our desired single component as well because this Rfc 2 can end up lying much lower in the expected value or it can happen the reverse say it can end up lying much higher than the expected values.

So, that is not a very well controlled values it can very factor of tens or even higher. So, it will be good to have some kind of tuning option or calibration. So, that this large value of resistor is calibrated or tuned as per requirement. So, we need to have some post silicon calibration or tuning options so that it is controllable or adjustable in the silicon we are having the option of tuning and matching it to the derived value because a simulation you may be expecting some values, but in the silicon you can end up having very different value because of a small change in the V t or over the time or so the resistance can change you know exponentially because of the sub threshold operation.

And hence, you can end up having very different R value and hence a very different frequency spectrum on the lower side of for our amplifier which is not desirable. Therefore, we will see that how to incorporate some tuning option in this circuit, circuit

with me both are the differential amplifier, if I am connecting my output DC point fixed with the help of the common mode feedback there is fixed.

(Refer Slide Time: 42:06)



And the input is just having some connection with the external electrode with the high power capacitor. So, there is no DC path to the capacitor, there is no DC path to the transistor and therefore, if you connect some very large resistor between the output to the this point the transistor is not a perfect insulator you are having some leakage current through that even if it is off it is providing a very large resistance. And as a result it will ensure that whatever DC point is obtained over here the same almost same DC point is obtained over here because there is in a steady state there is no current flowing into the gate of the MOSFET, there is no DC current flowing into this capacitor.

So, if the total current flowing here is 0 in steady state that must make sure that this DC potential is same whether DC potential here, this is clear.

Student: Sir, in AC it will be what?

Ac because.

Student: Output voltage scan you input scan (Refer Time: 43:17).

No. So, for the DC response once again because we are having very large R value and at the input side you are having an impedance which is much smaller than the R. So, if you

take superposition because the output signal there will be hardly an impact on the input side. Even if I just assume that you are applying some output signal over here what is its impact on the input. So, we can see that you are having some input impedance over here which is just having mega ohm. So, just we have seen that the electrode impedance that is approximately around mega ohm. So, here you are having around 10 to power of 10 or 10 to the power of 11 and here you are having mega. So, it is 1 mega, so still it is much larger. Therefore, if I am applying if I assume that let us see that is apply some output signal over here and what is its effect on the input that is not going to be so much, very manual.

Student: Sir, you told that is the resistance can change over time. So, if this condition satisfied at them data frequency is proper then if it is increase then raise to scan it be problematic, if it is decrease then it is have some issue if it is increased.

Increased then it has issue because it is going towards low frequency also and then you can have you know more artifacts coming into picture. So, we also want to suppress low frequency artifact. So, we have discussed the issues of dynamic offset. So, if you are lowering the cutoff frequency it will pass those low frequency artifacts also. So, we do not want to you know invite the low frequency artifact sitting at 0.1 hertz or something we want to block that. So, lowers set also it can create problem.

Student: Sir, what it is (Refer Time: 45:04).

(Refer Time: 45:07) is not enough definitely. So, as we have discussed we want to incorporate filtering operation in the main amplifier itself using some additional feedback operation. So, that also will be seeing that. I guess in some of the simulation exercises also we have seen how to incorporate a feedback loop which can take care of that additional low frequency component. So, it can incorporate some filtering operation in the main front and amplified itself and give you a high order filtering effectively, it is a concept of servo loop as we have discussed the similar thing will become.

Student: (Refer Time: 45:41).

No, this MOSFET noise is dependent upon the overall output the thermal noise of the MOSFET inverter mod of noise of the MOSFET, we have the modulate according to the MOSFET parameters. So, for our thermal noise of the MOSFET if you look at it, so here

anyway having very small gm 4 KT gamma gm will be the thermal noise current of the MOSFET. So, if you are using sub threshold region MOSFET gm anyway going to be very small the world current flowing with the MOSFET dividing a very small. So, the thermal current which is proportional to 4 KT gamma gm will also be very small therefore, it will not interfere with the feedback current provide by the capacitors too much.