Analog Circuits and Systems through SPICE Simulation
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Lecture - 19
DC Biasing Of Input Node

Welcome back. So, let us assume our discussion with which we started.

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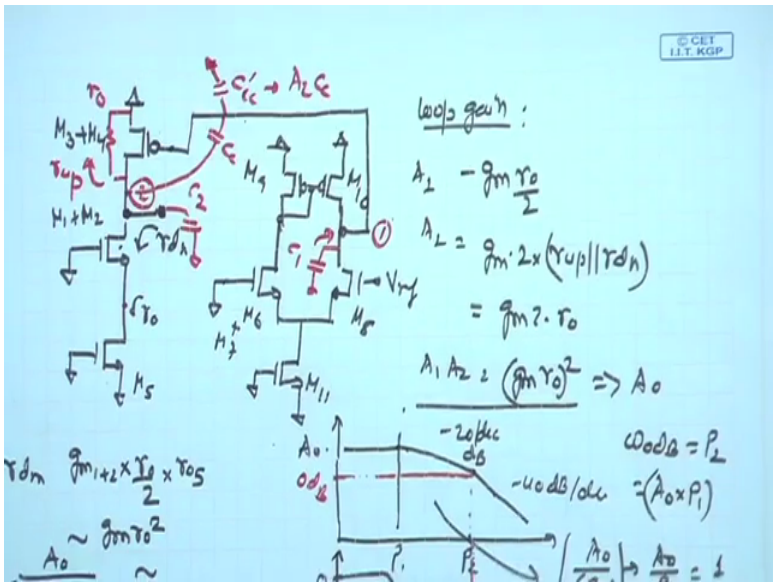

So, here we looked at the composition of the common mode feedback loop, where we try to put a compensation capacitor between the node 1 and node 2 and that resulted in a larger capacitance or larger equivalent capacitance between this point in AC ground by a multiplication factor A 2 which is the gain of this particular stage. And in that case the capacitance consummated at this point I can call this the additional capacitance coming because of the cc dash will be close to cc.

So this C2 is the equivalent capacitance coming because of the other transistors parasitics as well, but because you place cc this node will also experience another capacitive component which is close to cc, because the reverse factor or reverse similar factor from this point this point will be close to unity. So, still you are adding up little bit of capacitance at this node as well and that can interfere with your differential operation as well. Because remember when we talk about the overall capacitance between this point and the node over here node 2 over here in the actual circuit, in the actual differential

circuit this node is a differential node it is not a single node type together we do not have a you know resistor with the help of which we are taking a central tap, this is the part of the differential circuit.

So in the actual circuit this cc will have to be concave between the common pmos point and the two differential node separately as per this scheme.

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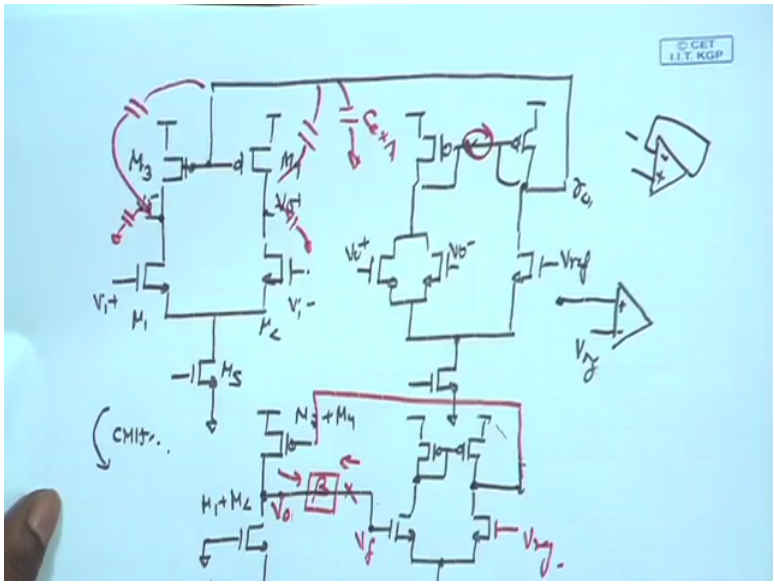

And that would mean that both these differential nodes where we are putting this cc and here. So, this is resulting in an effective capacitance over here, the gcc times the a of you know the common mode gain of this stage, from this input point to the output point whatever common mode or you know you should call it a common mode gain, but it is basically the gain of the common mode half circuit from the input point to the output. So, that is that was the A and that let to multiplication factor and resulting in a large capacitance between this point and ground over here, but apart from that we also have an equivalent capacitance contributed at this point because of the reverse multiplication factor, and that can interfere with our differential operation also because in our differential operation we are adding up some additional capacitance at this point.

So we just need to take care that whatever capacitance we are adding over here it does not add significant capacitance to the differential operation, so that the desired bandwidth is reduced for the differential operation. So, the common mode here we are assuming that the main concern is DC point. There is no significant common mode signal as such

which we are trying to cancel out, the main concern is to establish well defined common mode DC point and for that we do not need to really worry about the bandwidth of this loop or speed of the common mode feedback amplifier. We can minimize the speed of this particular amplifier, minimize the bandwidth of this amplifier by for example, reducing the bias current and increasing the channel length.

So that the ro y here is much stronger as compared to the ro of this stage that that is possible and that is also going to help us in saving some power. So, rather than burning equal amount of bias current here we can afford to sacrifice the bias current here as well because we do not really need to have good bandwidth in this stage this is just supposed to provide it a DC bias point. There may be applications where we need to track common mode signals as well in that case it may become important to keep the bandwidth of this common mode feedback close to the main amplifier. So, that it can track the common mode signal as well. So, that depends upon the requirement. So, here we are assuming that the purpose of this auxiliary amplifier is just to establish a DC point and therefore, we may not worry about the bandwidth of this amplifier or the speed of this amplifier it can be much slower as compared to the main amplifier.

So we should just take care that the additional capacitance that is coming at this differential node that is not limiting the bandwidth of the main amplifier further. We will see that for the overall differential operation, anyway we will be using composition capacitor for the differential operation also and that invention does limit the open loop bandwidth of the main amplifier, but since we are proposing to put capacitance over here we should also take care that does not limit the bandwidth over here. And if we say want to avoid any effect altogether on the differential node we can put buffers over here.

So be the capacitors can be put after buffer. So, if for example, if you have a after these nodes if you employ say buffers, rather than directly connect to the output node.

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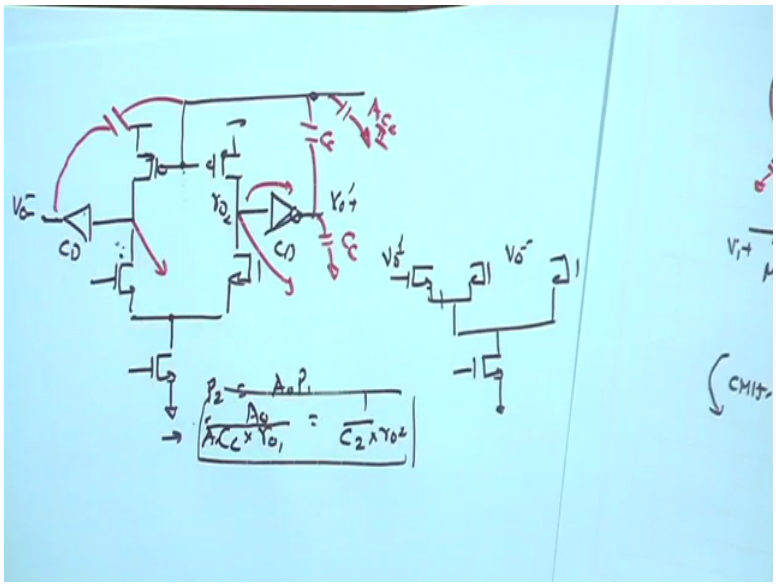

And alternate scheme where you can have buffers may sorry may be common drain buffers which has a relatively small output impedance and you are having the these are common drain buffer which can facilitate relatively low output impedance gain remains close to be unity from this point to this point; and if you are putting the gap between the output of the error amplifier and this point, it is not going to interfere with my actual differential node from which I am taking the differential signal.

So these remain intact these are not loaded because of the additional capacitor that we are putting; and the common drain stage since the impedance output impedance of the common drain stages (Refer Time: 06:17) smaller, even if you are ending up having an additional capacitance because of this cc approximately it is going to be cc, and we know that this is going to be approximately A times cc because of the gain factor A 2 times cc to be more accurate. So, this point A (Refer Time: 06:32) time cc, but after the common drain assuming that this gain is close to unity for the common drain, the component you get over here is only cc and along with that the output because of the common drain is relatively small, so that does not really interfere with the overall open loop response of our error amplifier.

So after that you have your normal error amplifier operation where the two outputs V 0 plus dash, and V 0 minus dash now will be going V 0 plus dash and V 0 minus dash this is your error amplifier that you had earlier. So, in that case the overall the cc has been

decoupled from the output node, that is not influencing the differential node except its be just influencing the common mode node over here and even if this node happens to have a larger capacitance, we do not really worry about the speed of this common mode because this is just a DC bias point.

So it is not important concern as of in this particular application where we are just concerned with establishing a DC bias with the help of common mode feedback. So, this is another point to be noted. And another benefit of doing, this if you see this node the capacitance is now independent of cc. So, you have some parasitic capacitance over here which is present because of the transistors or maybe some additional capacitors that you may have added for the differential mode that is independent of the cc. So, here we can still make sure that this A times cc times the ro of the differential pair is you know sufficiently larger or you know the criteria that P 2 is A 0 time P 1 is being make and for that I need to make sure that the P 2; the P 2 or the dominant pole that you are trying to make this is a times cc times the ro 1 if I call this node the ro 1, overall impedance over here ro 1 so need to make sure that a times cc times ro 1, 1upon that is going to be equal to A 0 times P 1.

So or in other words I want to make the dominant pole the P 1 and A 0 times that should be equal to the P 2 which is the total capacitance at the second pole that is C 2 times ro 2. So, in this case the C 2 and cc are decoupled. So, I can control C 2 and cc separately. So, for the first node since we have employed this cc, we have an overall capacitance a time cc coming at the first pole and then you have the ro 1 coming over here at the first stage. So, at the first stage we have assumed the total impedance over here is ro 1 and then A times cc is the total capacitance coming over here.

So, that gives me the A times cc times ro 1 that is the lower frequency pole have pushed that pole towards lower frequency, and what we are seeing here is that the second pole that is the pole at the output point that is decoupled with cc. If you are putting the buffer that is not interacting with cc as a result whatever parasitic capacitance C 2 that you have over here, that is not influenced by the compensation and then C 2 times ro 2 which is the overall impedance at this node becomes the pole over there and then I can try to set the value of cc such that this condition is met.

So then achieving a for where do we phase margin will be a lot more visible. So, buffer can help us decoupled the differential operation from the common mode compensation that we are trying to achieve for the common mode feedback loop. So, any question before we proceed further.

Student: (Refer Time: 11:07).

No the higher frequency pole if we look at our discussion over here, it because of the large cc value coming effectively the impedance at this node at higher frequency basically reduces it does not remain exactly ro it goes down effectively close to you know one upon gm of the low transistors let us discuss that we will look at that with respect to the differential operation also it will become more clear I will try to show that at high frequency at the omega is approaching high frequency, how the pole at this particular point gets shifted towards higher frequency. That is because the effective bypass operation provided by the cc.

So, at low frequencies or P 1 assuming that the P 1 the dominant pole is at much lower frequency than the P 2 they are the overall impedance provide by cc between these two points is still sufficiently large, but how when we are going towards P 2 much higher frequency, the impedance provided by cc between this point and the output node degrades and because of the one upon omega cc factor it almost start bearing like a short circuit, as a result you have a diode connected impedance coming over here and that impedance because pushes the second pole towards higher frequency.

So we will discuss that effect little bit more detail when we look at the differential operation. If you decouple that using buffer then that factor will not come into picture; however, if you have the capture is culture between this common gate point and output then of course, that will come in effect, but you know that will also degrade you differential gain and we can create problems with you differential operation also therefore, it will be better to decouple the differential operation from the common mode feedback. So, if you are trying to stabilize the common mode feedback it will be better to avoid its interaction interference with the differential operation that is why I have just implied this buffer and try to separate out the effect of cc on from the differential operation.

So here it will not be achieve, but you connect it directly over here then it will come into picture let us look at that when we go for the differential operation and the compensation for the differential screen, where you will be anyway connecting the cap sit of with from the output of the first stage will output of the second stage and there you will see that the impedance reduction because the cc will be coming into picture because of which the P 2 will be pushed towards higher frequency. So, let us look at over that.

Student: sir how (Refer Time: 13:46).

Gain is same right. So, formula if you need a gain from this point, to this point similar effect for this this is a unity gain close to unity gain the common drain stage that does not you know degrade your gain too much. So, therefore, the gain remain same from this point to this point because you have a common gain or not and the this point is not suffering so much because this is output impedance is low even if you get a cc is not having any significant degradation in the pole whereas, this point because output impedance from the previous stage is high m and apart from that I am putting a large cap over here a time cc, you are ending up having a large time constant over here.

Student: Sir DC point and (Refer Time: 14:27) change in this course.

What?

Student: Because where the common (Refer Time: 14:35) was DC point will.

Will you have to make sure that the DC bias point of the common drain stage is sufficient for driving the input over here. So, in general this DC first point of the first stage will not be very low will be relatively high. So, for example, if you have A 2 stage amplifier after that yesterday, we did common source amplifier we put two common source amplifier over here. So, in the simulation exercises of so we will look at that the DC bias point over here for achieving best possible swing at the output will be relatively high will be close to you know the vg of this MOSFET.

So and after that if you have a common drain it will have another Vgs drop, you have to make sure that of course, that Vgs drop is not too high such that the gate voltage over here becomes too low. So, you have to make sure that the levels are consistent we can use you know you can use the buffer, where you can have a common drain with basis of

NMOS and another common drain based on PMOS and you can cancel the level shifts also. So, the buffers can be considered in several ways common drain is one option you can also have a voltage follower kind of configuration build with just a single stage differential amplifier because if you are using a buffer there the target is not to every precise gain therefore, I can just use a differential amplifier with current mirror load in negative feedback configuration and construct a good buffer out of that as well this can also be done.

So in this case you do not worry so much about the DC shift as well, and if you are using common drain in that case you can use if you want to cancel the DC shift, you can basically use a NMOS stage common drain PMOS stage common drain that will also cancel out the shift there are several ways. You can construct this one is the surface, but and moreover this is single stage right. So, if you are using a just single differential amplifier with current mirror load, this is basically a single stage differential amplifier. So, inherently it will not be. So, unstable this energy stable because of just being a single stage amplifier it also has multiple pole, but these guys are at higher frequency that connected load this point it will be at higher frequency.

So you can construct a good buffer sufficiently good buffer just using the single stage. Because when we are using these buffers we do not want very precise one gain unity gain is you just be approximately able to follow. So, we can use single stage also to produce a buffer using differential amplifier.

Student: (Refer Time: 17:07) from here we get the output (Refer Time: 17:11).

Of course, now also in this case we are not using the buffer to feed to the next stage. So, the output is going from the differential output only. So, this is just to decouple the common mode feedback from the differential operation. So, output goes from the differential before buffer, but that this if we will see that in the differential case also in some scenario will have to do is buffer. So, I just in this particular example the buffer is just used to separate out the differential node from the common mode compensation and the signal actually is going from this point to the next stage any other question.

Student: (Refer Time: 17:50).

Yes let us a A 2 time cc

Student: (Refer Time: 17:59).

A 2 is that any other question now as we have discuss yesterday we can apply the common mode feedback separately for the two loops also or you can combine the entire loop and apply a single common mode feedback. So, if I go for the combined common mode feedback then the scenario is slightly different.

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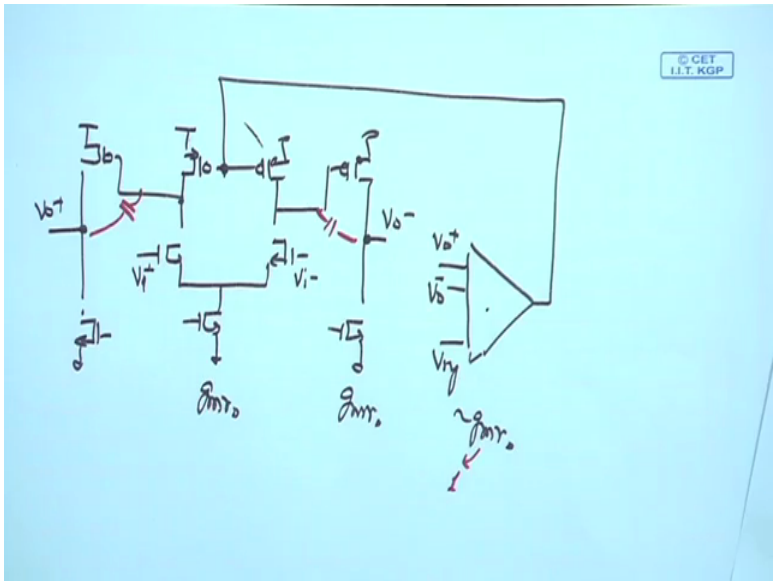

So, for example, if I apply a common mode feedback for the two loops combined together that is one option, in this case the V 0 plus Vi plus and Vi minus and you have V 0 plus and V 0 minus. So, in this case the error amplifier if I draw it you have the two inputs which are taking up V 0 plus and V 0 minus and the third one is just the Vref and then the output goes back to my PMOS load.

So this is a single loop common mode feedback where we are relying on only one error amplifier which is rejecting the final output and giving the bias point over here. In this case if you want to stabilize this circuit look at the open loop analysis then of course, we see that the overall loop gain will be the gain of the differential amplifier, again in the common mode these two stages will be combined together. So, you will have basically two stages of common source amplifier detective load. So, if I strip to the previous previous topology of the error amplifier this is going to give me a gain of the order of gmro in the loop gain the is also going to give me gmro and the common source is also going to give me gmro.

So overall there will be gmro cube whole loop gain, as a result this is much larger as compared to the previous case where we where you are having feedback in the same loop and this can further lead to instability. So, whenever you have larger gain in the loop it can make the system lot more unstable. So, in that case if you want to be safer we can get rid of this current mirror load and rather use diode connected load. So, in that case basically we can reduce the load of our error amplifier, and then we will eliminate this interconnection and then just go for diode connected load both sides.

So in that case what will happen the gain of this stage will become just close to unity because for a diode connected load we know that the gain from input to the output gm 1 upon gm 2 another result the resulting this stamp with diode connected load will have lower gain another result this factor from gmro it will go to close to unity, and then my overall gain will just remain gmro times gmro square. So, that will be safer because the gain will be limited and it will help us achieve stability for the common mode response once again and however, in that case since we have the overall two stages in the differential gain, it can be compensated using the differential stage itself.

So for example, if we just lie on the capacitor connected between the first stage in the second stage for example, if we put a cc over here and cc over here, which is generally done for the differential mode compensation, in the common mode also these two cc are going to come as it is and they will compensate the common mode response also. So, if you look at the common mode response if you are connecting a cc between the output of the first stage and output of the second stage in the differential amplifier, in the common mode response also the cc is going to come between the common mode half circuit of the first stage and the second common source stage right if you combine this two together in the common mode response these two will be combined together these two nodes will be combined together, as a result the this cc will come between the common mode output point of the differential pair and output point of the second stage, as a result you can have the overall composition given by just cc.

So the common mode loop can also be compensated by cc. You will see that this cc is generally use for compensating the differential operation, but in this case we can use it also to compensate the common mode loop that is one possibility and; however, and the main reason is that this is not contributing to much gain. So, this is the gain is unity. So, it is not going to degrade your phase margin too much; however, the other case when you

are using say the common mode feedback for the individual loops they are generally we will like to make sure that the overall loop gain is still large maybe gmro square, and in that case we will be using our previous scheme where we have is it will be large gain current with a load error amplifier and we will be using that loop for the output stage separately and the differential amplifier separately, and there we need to compensate the individual loops also because they are not aligned with the overall differential loop.

So in that case the individual common mode loop for the output stage and the differential amplifier they are separate. So, we will look into these examples also in simulation exercises we will be trying to analyze both the cases, when we are trying to compensate we are trying to have common mode feedback for the two stages separately using two error amplifiers, and the other option where we are having a single common mode amplifier doing the combination for the entire common mode setup for the final stage as well as the first stage. So, there are couple of tradeoffs on this related to this choice probably that will be more clear when we look at the simulation examples.

So any question we will proceed towards the stability analysis for the differential stage. So, whatever we have drawn just now we will see that this particular scheme can help us stabilize the differential mode operation also along with the common mode. So, let us look into that any question before you proceed. So, let us look at the fully differential operation now, and see how the scheme is going to help us in stabilizing the overall differential operation. So, for the differential operation I can simply put this to an AC ground, because this is going to be a DC bias point over the common mode operation.

So I am assuming that the common mode is stable and we are having an AC ground over here this is the DC bias point.

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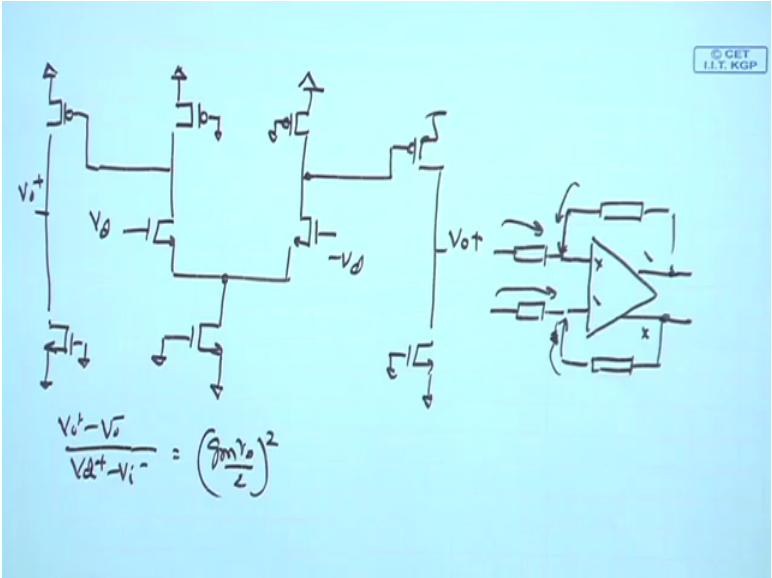

So, the for the differential half circuit I will ignore the common mode operation, and only draw the differential operation differential circuit this we have Vd and minus Vd and then you have the second common source stage. So, all the DC bias point I am putting it to AC ground and here once again we know that for the differential gain from the input to the final output is having gmro by 2 square term first it gives us gmro by 2, second stage again common source amplifier give us gmro by 2 and the result we are going to have V 0 plus minus V 0 minus upon we I should take Vd overall Vd.

So, in this case I can just write is Vi plus minus vi minus should be gm ro by 2 square. So, we do the low frequency open loop gain of this particular circuit and we also need to check the overall feedback operation that we are going to apply over here for our amplifier design. So, we need to include the additional feedback factor and then look at the stability of the closed loop. Now if you look at the feedback operation that we have started with the differential operation is having the capacity feedback where we have Z 1 Z 2 implemented using C 1 C 2 and we are taking the outputs over here.

If we now look at the feedback scheme, what is the feedback scheme being implemented over here if I assume this is plus minus and minus plus. So, we are having the output voltage being sampled by this feedback element and being combined in shunt manner with the input signal therefore, output we have voltage sampling, but at the input we are seeing that the sample quantity is being combined in shunt; that means, it is getting

mixed in shunt or in parallel with the input component. So, if I have an input signal the feedback signal is combined at the same node along with the input signal.

So if I have the signal coming from the negative terminal, it is getting combined with the signal coming at the positive terminal in a parallel fashion just like we add current. So, definitely we have a shunt connection at the input and likewise we have a shunt connection at the output because here also we are sensing the output voltage using this feedback network. So, basically this particular topology is a shunt-shunt amplifier although we are having a applied input voltage over here, but effectively the feedback topology is like that of a shunt-shunt amplifier. So, while analyzing this we have to be careful about this topology and we need to look at or arrive at the open loop amplifier considering this particular topology.

So that is something we need to take care of before we go towards the analysis of the differential operation for this given shunt-shunt amplifier that we have designed we have chosen for our front end amplifier, and along with that another important point that we also like to discuss is the DC bias. So, we have discussed the DC bias for the common mode case and we have this the main purpose of using the common mode feedback is to have a stable DC bias for the common mode; that means, the DC bias point at the first stage output and the second stage output are very stable very precisely defined and that was the purpose served by the common mode feedback. And after that we looked into the stability as well and make sure that we can have some compensation scheme.

So that the phase margin in the common mode feedback loop is sufficient likewise in the differential operation we are relying on these feedback elements to give us a well defined gain with the help of these passive elements in this case capacitor, but in this case apart from getting the gain we also need to make sure that we are having sufficient or appropriate DC bias of the input point.

So, both these factors again need to be analyzed here the stability of the feedback loop that we are applying for getting a well defined gain and apart from that in present of this feedback loop whether the DC bias point at the input is satisfied whether we are having appropriate DC bias at the input and what can be done to achieve a (Refer Time: 31:09) DC bias at the input, so both these criterion it to be examined with respect to the

differential operation also. So, we have done it for the common mode operation let us do the same for the differential operation.