Analog Circuits and Systems through SPICE Simulation
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Lecture - 15

Let us continue with the discussion from where we left.

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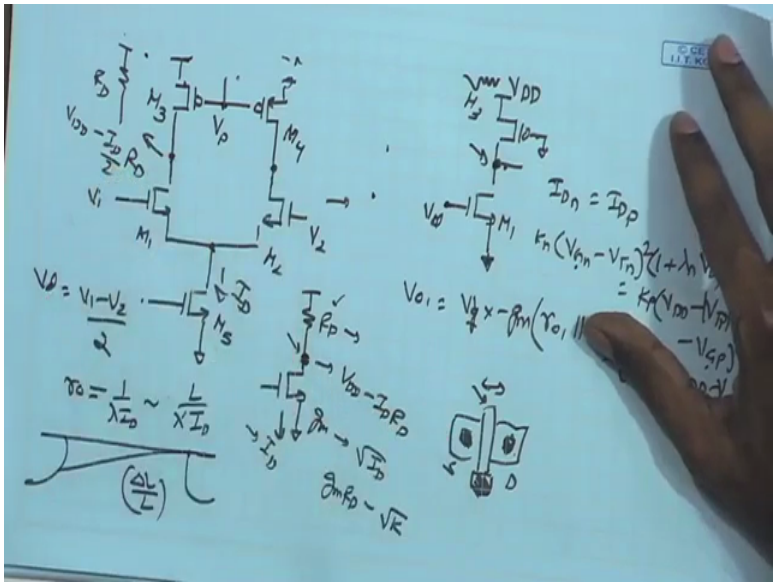

So, we are looking at the biasing problem of on active load differential amplifier we concluded that if you are looking at a DC bias point of an active load common source amplifier we know that this DC point is not very well controllable because it depends upon so many device parameters k and k p lambda and lambda p ratios. And therefore, if you have fabricating (Refer Time: 00:44) simulation you may be getting some value, but after fabrication you will be getting completely different values and for different versions or so different the copies of the same circuit the values can be very different and it cannot even guarantee that the transistors will be in saturation.

So, we need to take help of some other biasing schemes with the help of which I can ensure a proper DC biasing point over here.

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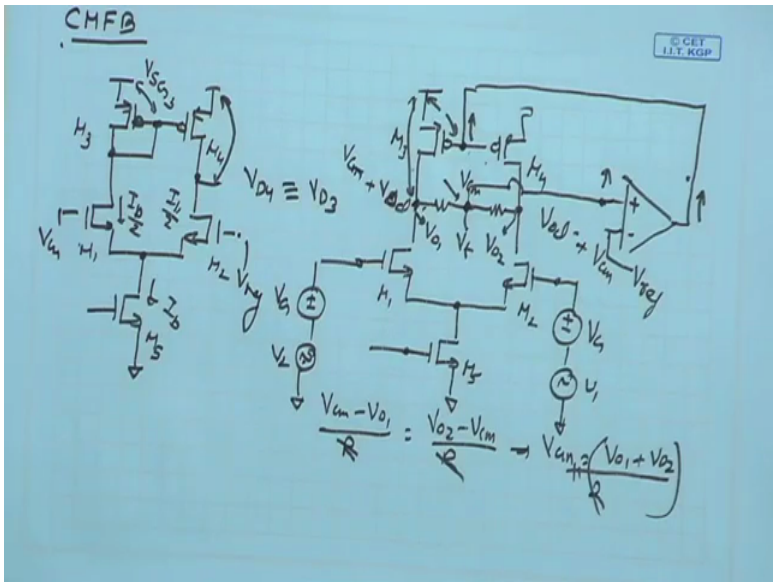

So, that technique is called common mode feedback where we take the advantage of differential amplifier with current mirror load which is having are well defined DC bias point. So, let us visit our deferential amplifier with current mirror load in order to being used as a common mode feedback unit. So, here we know that if you are pumping a DC bias current I bias into m 5 the 2 transistors are going to shrink I b by 2 provided you are having same DC bias condition for m 1 and m 2 and m 1 m 2 are well matched. And therefore, both these transistor and 3 mm 4 also going to have same I bias by 2 I b by 2 I b by 2 in both of them. And the I b by 2 flowing in m 3 is going to establish a certain VSG for the transistor which is basically going to be copied by m 4 the same VSG apply for the m 4.

Therefore, this load act like a current mirror the m 3 establishes a certain value of VSG which is enforced by the id by 2 provided by the bias current and provide by the symmetric biasing point enforced at the gates of m 1 and m 2. And now if we also look at the other terminal of the m 3 and m 4; the source terminal they are at the same potential as a result the VSG of m 3 and m 4 is at the same potential the transistors m 1 and m 2 are trying to enforce the same current into them.

Therefore, the id of m 3 and m 4 is going to be same VSG is same and therefore, the VSD also must be same that basically ensures that the VSD of m 4 is exactly same or very well matched with respect to VSD of m 3 therefore, VD of 4 must be very close to

VD of 3 ideally equal to the VD of 3 if these 2 transistors pairs are very well match. So, differential amplifiers with current mirror load a self biasing. So, it provides an output DC point it is well defined it is equal to the VSG of m 3. And therefore, we can take help of the differential amplifier with current mirror load to bias our fully differential amplifier which is not having a well defined DC bias point. So, let us look at the overall solution that we are going to apply. So, let us draw our fully deferential amplifier once again.

Call this m 1 m 2 m 3 m 4 and call this m 5. So, assume that the gate of m 5 is any bias with the help of a current mirror and I am not drawing all that. And now the first thing that we need to do is to find out or extract the common mode voltage or the common mode DC bias point for the differential amplifier output I am assuming that the input DC points are same and both the sides are well matched you may be having some signal applied to both m 1 and m 2. So, on the top of the DC bias point you may be having some signals as well. So, you having the V g of m 1 and m 2 same the DC bias same and on the top of that you may be having some V 1 and V 2 arbitrary V 1 and V 2 small signals.

And a result we know that the differential signal V 1 minus V 2 by 2 common mode signal V 1 plus V 2 by 2 and we assume that the common mode gain is poor therefore, we do not consider the common mode signal coming over here let us consider the differential signal coming over here is we call it VD; VOD plus and VOD minus. So, you will have some differential signal coming over here and if I want to get the common mode signal.

So, you are having VOD say plus the common mode level it can also have DC plus AC as I said if the common mode gain is sufficient it can also lead to some common mode signal over here. So, it may not be just a DC it can be suppose some common mode signal VCM plus VCM. So, assume that not only dc, but you also have a common mode AC signal. So, if I want to extract the common mode signal I can take a resistive divider and at this point if I assume this voltage to be V o 1 and this to be V o 2 that is we can write down the equation for this particular node.

So, if I write this as say vt what is the vt. So, for that I will solve the kcl in this direction. So, you just have kcl being solved over here. So, I will write VCM minus V o 1 upon this

R that should be equal to the V o 2 minus VCM upon R r R being equal we can say that the VCM is going to be V o 1 plus V o 2 by 2 sorry V o 1 as your 2 by 2. As a result if you are having an overall common mode and differential signal we can say that the central point over here is just going to capture the common mode signal. And that is what we want we want to set the common mode level. Now we have extracted the common mode signal out of this amplifier and we want to fix it to a desired value.

Now in the subsequent equation I am going to assume that I am not caring for the past varying common mode signal, because then the design becomes more challenging. So, assume that I can filter out any common mode small signal over here. So, in that case I will be remaining with only the common mode DC that I want. So, it will be the common mode DC level that I want to set.

So, my target is to have a proper common mode DC level. So, if you are having a differential signal over here its affect does not come over here and at this point you are good thing only V o 1 plus V o 2 by 2 which is absolutely the DC bias point or the DC common mode level at the 2 outputs now I can apply a an error amplifier over here and try to put a reference voltage V ref at the terminal and the output of this can be made to control the gate of the PIMOs and if I ensure negative feedback in this loop the negative feedbacks stabilizes the input voltage at the positive terminal close to the negative terminal or vice versa it will make sure that these 2 voltages are same.

So, if I ensure negative feedback it will make sure that the 2 voltages over here are close together and therefore, it will ensure that we see m is equal to V ref and in order to make its negative feedback I also need to make sure that the polarity of increase over here is causing the reverse action to be taken by the m 4 and m 3 which again you know tries to adjust this VCM back to the prior value. So, let us see what should be the derived polarity.

So, suppose your VCM because of some reasons is going up as compared to the reference voltage in that case I would like the feedback loop to bring this VCM or the common mode voltage back to the desired value V ref how can it happen. So, if the VCM is going up and suppose the output voltage of the amplifier also goes up; that means, in that case we are going to have this as positive this as negative. So, if the VCM goes up the positive terminal input is going up with respect to V ref as a result the output

voltage over here will go up as a result the gate voltage of these 2 PMOS transistors will also go up.

So, what should happen to the output DC voltages over here? So, if the gate voltage of these 2 MOFSETS go up remember that the DC bias point provided by m 5 is fixed the DC current flowing through m 1 and m 2. Therefore, they are you know same as I bias by 2 and therefore, the DC current flowing through m 3 and m 4 they are also same as I bias by 2 and now you are increasing the gate voltage of m 3 and m 4.

So, in order to maintain the same DC current I bias by 2 what should happen to the drain voltages it should go down because you are reducing the VSG by pulling the gate voltage up. So, VSG oh or both the PMOS is getting reduced as a result only way to maintain the same I bias by 2 current through both of them is to increase the VSD of both the MOFSETS. And therefore, it will try to pull down both the drain potentials another result the common mode voltage will come down again close to V ref.

So, we see that there is a negative feedback operation involved here if we make this connection to the positive terminal of the amplifier. So, we can call this as error amplifier which is amplifying any small difference between the actual common mode signal and the desired reference signal to which we want to set the common modes and it is controlling the gate voltage of PMOS. So, that they in turn control the DC bias point at the output.

So, using this configuration where a differential amplifier with differential input, but a single ended output is controlling the DC bias point at the gate of m 3 and m 4 which in turn are controlling the DC bias point at the 2 outputs we are able to establish a well defined DC bias point V ref at the output nodes. So, this is the basic mechanism involved in the common mode feedback.

Now we can just replace this amplifier with our differential amplifier with current mirror load where we can use these 2 input terminals of m 1 and m 2 the positive terminal of course, is going to be the gate of m 1 because if you increase the gate voltage of m 1 you know that this output goes up. So, for the differential amplifier with current mirror load this is the single ended output and therefore, with respect to the gate of m 1 we know that if you increase the gate voltage of m 1 the output over here goes high this is an non inverting terminal this is the inverting terminal. So, basically the midpoint VCM will be

connected over here V ref will be connected over here and the output of this amplifier will be fed to the gate voltage of m 3 and m 4.

So, this is the way we can realize a common mode feedback circuit where we are establishing probably DC bias for the fully differential amplifier with the help of our differential amplifier with current mirror load. So, the differential amplifier with current mirror load since it is self buyers and it is having a well defined DC point it can help the other guy having a established DC bias.

Now of course, what is the effect of this resistive voltage divider on the differential operation that also needs to be considered? So, if I look at the differential operation once again if I assume that the DC bias point the gate are same well defined differential half circuit this point will be AC ground and as a result.

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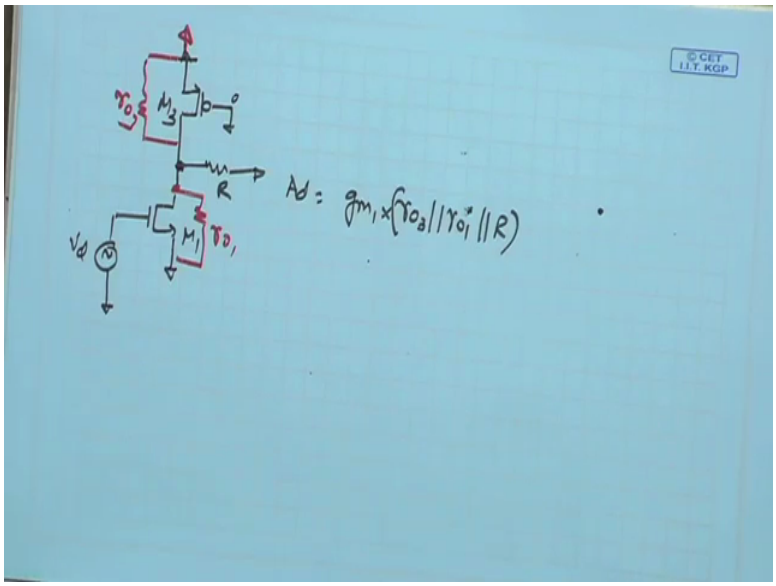

If you look at the differential operation I am going to draw the differential half circuit with the PMOS gates at AC ground you have the NMOS gate receiving VD by 2 let us keep this in the view and you are having the PMOS gate receiving VD by 2 and this is an AC ground and you are having the output signal over here if you look at the condition of R that is appearing between the output point and the VCM which is not having a differential signal. So, with respect to the differential half circuit this point will be AC ground because there is no differential signal coming over here.

So, in our differential half circuit this R will come between these individual outputs and AC ground. So, in the differential half circuit I will put this between the output and AC ground as a result for the differential half circuit our gain can be modified as a differential is equal to gm 1 ro 3 parallel ro 1 parallel R, because we know that for this equivalent differential of circuit is acting like a common source amplifier where you have the ro of the 2 MOFSETS coming into picture between the drain and the AC ground. So, you have ro 1 over here likewise you have ro 3 over here vdd is effectively in AC ground on for the motion analysis.

So, ro 3 over here basically ro 1 ro 3 and R all appear between the output point and the respective AC grounds and therefore, the overall gain is just gm one times ro 3 parallel ro parallel R and therefore, definitely if we want to maintain large open loop gain we must make sure that R is sufficiently larger as compared to ro 3 and ro 1. And now this requirement will just differently make us thing that of course, now they are going to be lot of constraints, because we are looking for lower current. So, that we can reduce about power dissipation we also want larger open loop gain that would also enforce lower bias current and that would mean very large ro 1 and ro 3.

So, the technology if you are going for bias currents of the order of 10 micro ampere ro values can easily approach hundreds of kilo ohm to one mega ohm especially when you use longer channel lengths. So, we will see that noise constrain also enforces longer channel lengths and that would make the ro 1 ro 3 pretty large and that would mean that if you really want to use the resistive divider to extract the common mode voltage the R value required over here will also be very large.

And then the expected value can range from mega ohm anywhere between mega ohm to tens of mega ohms which build once again will not be very practical for the point of view of integrated circuit design. Therefore, we can look for alternate techniques where we can avoid use of such resistive dividers and rather go for active components only in the feedback loop.

So, let us look at alternate scheme where we can avoid the use of such large passive resistors in order to determine the common mode feedback. So, let us just have a brief overview of what we are going to do. So, we are going to basically have our error amplifier itself being capable of extracting the common mode signal.

So, here we are relying on this R values to extract the common mode signal and then it respect to a simpler error amplifier. Now if we can translate or we can you know outsource this common mode extraction to our error amplifier then the job becomes simplified we may not rely on R there is a strategy we are going to use. We are going to incorporate this common mode extraction inside our error amplifier so that we do not have to rely on these large resistors in order to achieve common mode feedback.

So, let us look at that in our next module.