**Analog Circuits and Systems through SPICE Simulation**

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**Lecture – 14**

Welcome back.

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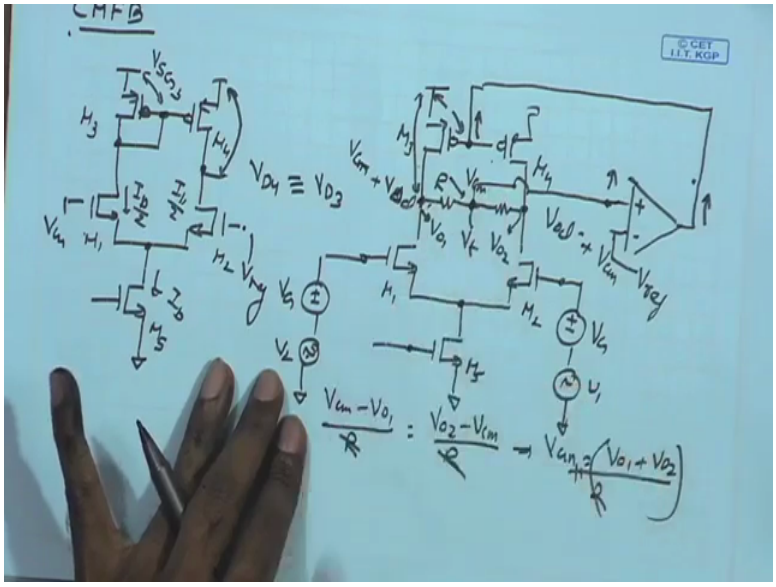


So, we are going to look into the discussion and continue our analysis on the common mode feedback, where we are going to replace the present common mode feedback scheme with a whether active common mode feedback where we will get rid of these two registers in order to extract the V CM; let us see how can we do that.

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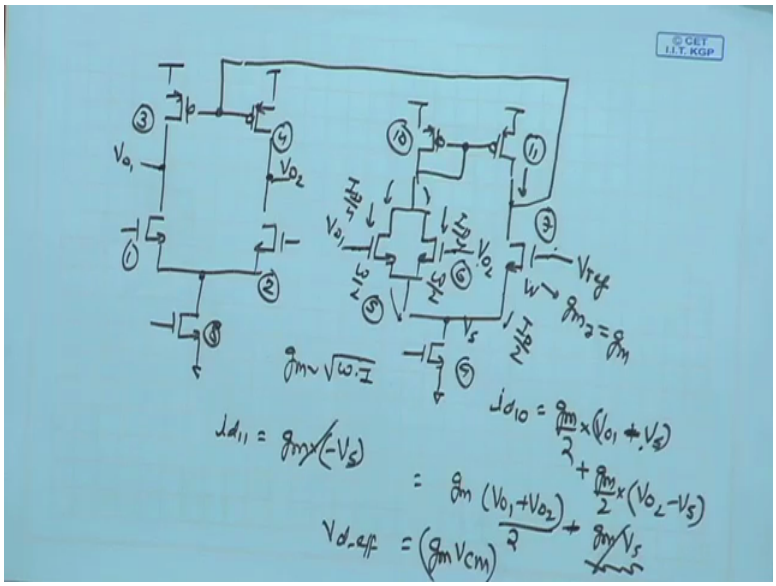


So, once again I will redraw the fully differential amplifier. And I will have a slightly modified version of our differential amplifier with current mirror load where one of the input devices has been split into two. So, this is w each of this is w by 2. And obviously, if you are having the gate biases almost at the similar value, you will also have the I D flowing in these two branches almost similar and as a result I D of these two devices will also be half of I D of this one. So, this is having I D by 2 each of these will be having I D by 4 I D by 4.

As a result what I can say is the gm of these two devices will be half of the gm of the device over here, because you know that gm is proportional to root under w and I. So, if the w of these two is half of the w of this device as well as bias current is half of course the gm is going to be half. Each of these are going to half the gm of this one. So, let me number this 1, 2, 3, 4, 5, let me call this 6 7. And now the load side I will decide upon the diode connectivity once we discuss the polarity; let us leave that for the timing.

Now, one of them will have the diode connection because this is the current mirror load how will be determined diode connection that again depends upon the negative feedback polarity. Now if we connect the two outputs over here say Vo 1 and Vo 2 to these inputs. So, what I am going to do automatically I am connecting Vo 1 over here and Vo 2 over here. So, these two outputs are brought and connected to the two input devices over here.

And that condition what can I write about the common mode are the differential current signals flowing through these two. So, if I am having the output signals over here Vo 1 and Vo 2 and if I assume that this is a source which is not necessarily at AC ground, because if the signals are not fully differential that may not be exactly at AC ground suppose there is some small signal V s coming over here this is our reference signal V ref and I want my output common mode of the differential amplifier to be set equal to the reference signal.

As a result if I look at the small signal current combination flowing from these two transistors; let me call this 11 and 10. If I look at the small signal current flowing through these two transistors provided by these two pull down devices I can sum the small signal current flowing through this two. So, I can write the id 10; id 10 is going to be equal to gm 5 which is gm by 2 if I call gm of m seven as just gm. So, the gm of m 5 is just gm by 2. So, id 10 is going to be gm by 2 times Vo 1 plus or if I assume that the source is not at AC ground. So, I should basically take Vo 1 minus V s plus another gm by 2 times Vo 2 minus V s, and therefore I can write down id 10 as gm times Vo 1 plus Vo 2 by 2, plus gm times V s rather minus gm times V s.

So, this is the extraneous component that is coming. Likewise on the other side if I see this is a DC potential this is V ref which is a constant DC; as a result there is no AC signal over here. Therefore, what is the small signal current for id 11. So, if I write the same thing for id 11 that is going to be gm times vgs vg of this is zero because the small signal value is 0 V g become 0 minus V s.

Therefore if I look at the differential current id 11 is just gm times minus V s minus gm V s, id 10 on the other hand minus gm V s plus this quantity. As a result this is the common quantity which will get subtracted which will look at the differential operation. So, I do not need to worry about this. Effectively the overall signal that is coming is equal to gm Vo 1 plus Vo 2 by 2 which is nothing else, but thus V CM.

Therefore, the effective differential signal which is coming at this differential input overall differential input is just gm V CM effective V d for the error amplified happens to be just gm V CM. So, basically this split differential pair is expecting the V CM of the first stage. So, it is helping us in obtaining the V CM in an indirect fashion. We are get

got rid of that register divider and with the help of this split pair we are able to extract the V CM.

Now, if you look at the polarity. Once again if V CM goes up means both the signals are going up or the common mode level of the first amplifier the main differential amplifier is going up; that means, the voltage over here will be going down and this potential will be going up. And we know that the up going potential is to be connected to the PMOS. Therefore, this is supposed to be my output which is supposed to be connected to the PMOS gate.

So, I will once again make the diode connection over here and connect the output of my error amplifier to the gate of m 3 and mm 4. Therefore, once again if the common mode voltage of the fully differential amplifier goes up this is the effectively the non inverting input of my error amplifier. If this common mode goes up the output over here will go up as a result the PMOS gate voltages those go up. And as we discussed in the last session it will try to bring this two levels or the common mode level over here back to the reference value which is the V ref.

So, this is once again doing the similar operation basis we are able to establish a well defined precise V ref or common mode voltage at the output of the fully differential amplifier with the help of this error amplifier.

Now, in general when we go for operational amplifier design we know that we will be needing multiple stages, we will need two stages in a given operation amplified at least to get a larger gain. And the second stage is also active load and fully differential. So, how do we incorporate common mode feedback in such a case?

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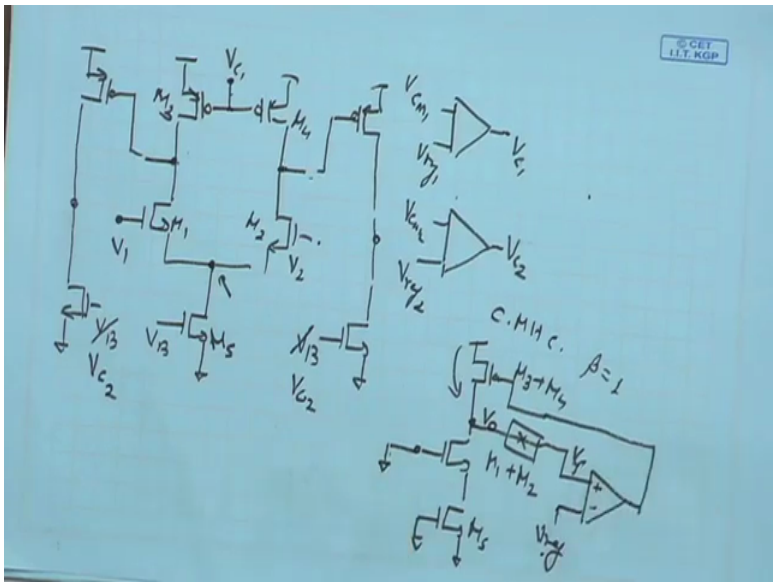


So, we can look at that scenario where we have a fully differential Op-Amp where you have two stage amplification. So, basically the output of the first page expect to a second stage which is going to be simply common source amplifier. So, all these are bias points. So, this is V B which is a fixed bias point, and your inputs are over here I am not showing the input bias point for the main amplifier.

And here in this case we have the first output which is active load which is not having a well defined DC point, and also the second output is also an active load which is also not having well defined DC point. What is the overall gain of this circuit if I will talk about a differential gain? The first stage is same as are our fully differential amplifier, therefore the gain from V 1 V 2- Vo 1 and Vo 2 over here remain same gm ro by 2.

So, the differential gain remains same, as we will assume this point to the AC ground and then this becomes the common source with amplifier with active load. And therefore, the gain expression from these two input to the output remains same. After that basically you have just another common source stage. So, these two transistors are just providing to another common source stage where these two bottom transistors are active low they are bias with the fixed DC potential they are providing active load and these two are the input devices or the input devices of a common source transistors.

Therefore, these two stages are also going to provide you similar gain factor gm ro by 2. So, this is a common source amplifier input device, the low device. And therefore, the

gain from here to the output is again gm ro by 2. And these are also active loads and therefore, we do not have a well defined DC point over here.

So, now in this particular amplifier the how can we set the DC bias point for both the stages? One option is that we sense the common mode at the final output only and then control the bias point of the PMOS transistor by the single error amplifier. Assuming that it is going to set up the cover mode level over here appropriately such that the (Refer Time: 10:50) common mode output over here is at the desired DC point. That is one option I can just sense the two outputs over here and extract the common mode corresponding to these two outputs and then generate the error signal which is going to control the bias point of the PMOS.

But a safer option would be to control these two DC point separately. That means, I would use a first error amplifier to control the DC bias point of the output of the first stage separately. So, I will say V CM of the first stage compared with V ref and then provide the control signal V c 1 and then use another one to get the V CM of the second stage call it V CM 2. And then provide and you know you can the V ref can be different V ref 2 and provide another control voltage V c 2 to control the gate voltages over here, rather than fixing them you apply another gate voltage V c 2 which is coming from the error amplifier.

So, in that case I can control the two DC bias points for the output stage and the first stage separately and safely. So, in simulation exercises as we can see that what happens if we rely on a single error amplifier and you know try to control the output DC point by just adjusting the V c 1 with the help of single error amplifier. That can be more risky case and it will be more clear when we look at the corresponding simulation example; we better to explain with that.

So, in general for more robes design people prefer having separate common mode feedback for the two stages.

Now, after going through this basic operation of common mode feedback we need to look into some of the important aspects associated with this common mode feedback loop namely stability first of all. So, whenever we had having negative feedback in the circuit it is very important that the feedback loop is stable and we are not having unwanted oscillations which can corrupt your overall operation. Therefore, once again

the stability analysis of the feedback becomes important. And for stability analysis we can first of all find out the feedback topology of this circuit look at the overall high frequency polls coming in this circuit. And then look at the considerations that we can make to ensure overall stability and the feedback loop; what kind of compensation, what kind of components are supposed to be added so that we can make sure that the overall loop is stable.

So, before we go to words stability analysis first of all we need to look at the equivalent common mode circuit, because ultimately this is a common mode feedback and therefore we need to look at the common mode half circuit for the original amplifier clubbed with the error amplifier to arrive at the overall common mode circuit for which we will be analyzing the stability. So, let us quickly look at the common mode half circuit for which stability will be analyzed.

So, we know that for a single differential amplifier stage when we arrive at the common mode half circuit, we will be basically, combining these two transistors together, combining the input devices together assuming that the input voltage is same, because if the input applied voltage is same the common mode value the output DC point will be exactly same as a result we can tie them together. So, in the common mode half circuit we simply tie these two nodes together. And as a result in the equivalent common mode half circuit I will have the two transistors M 1, M 2, and M 3, M 4 tied up together.

So, I will have this as M 3 plus M 4 and the input device will be reduced to M 1 plus M 2. For the common mode of course, we do not have this point as the AC ground. So, we will have the M 5, if I call this M 5; I will have the M 5 also coming into picture. And then the gate of M 5 is AC ground because the gate of M 5 is sc ground because the gate of M 5 is just the DC bias. So, this can be set to AC ground the common mode signal at the gate of M 1 and M 2 for the time being we are assuming it to be 0 there is no common mode signal applied. So, I can put this also put to be AC ground.

The gate of a M 3 and M 4 however is driven by my error amplifier. So, I will have the common mode output coming from the first stage which is going to the error amplifier whose output is basically controlling the gate of M 3 and M 4. So, this is the equivalent common mode half circuit and you are having the V ref over here, and the common

mode signal coming from the main differential amplifier is fed to the positive terminal of the error amplifier.

Now in this see this case we can assume the V ref to be my input port and I can see that the final voltage that is fed back to the other terminal is at the opposite polarity. So, if I assume that the V ref is an input signal which I willing to change to set up a new common mode voltage we can see that the feedback voltage that is coming over here that is at the opposite terminal. As a result we can say that there is a series feedback at the input terminal of this amplifier. Whenever the feedback signal coming from the loop is at the opposite terminal of the differential amplifier basically effectively subtract from the input signal. As a result we can say that there is an effective negative feedback coming over here.

And if I have to open the loop I can break the loop over here at this point and we can see is that the output voltage over here is being applied as it is to the feedback terminal. As a result what we can say is the V F or the feedback signal is equal to Vo. So, basically the feedback factor is 1 essentially. So, the output signal after traversing the loop from the differential amplifier going into the fully differential amplifier common mode, the output common mode is applied as it is to the positive terminal. As the result the beta factor is one. And we are sensing the output potential of the output stage here. As the result we are having a shunt connection at the output.

So, once again series at the input because we are subtracting the feedback voltage from the effective input voltage; and we are having the shunt connection at the output, because we are having of feedback network beta equal to unit t and it is just passing the output voltage as it is to the non inverting terminal of the amplifier. So, we can draw the transistor level implementation of this amplifier and then analyze this in the open loop case to obtain the stability, phase margin, etcetera using the frequency response. And then look for the stability criteria where and how to add additional components in terms of capacitors to stabilize the circuit and obtain a reliable phase margin.

So, let us look at that in the next module.