Analog Circuits and Systems through SPICE Simulation
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Lecture - 13

Welcome back. We are going to continue from where we left.

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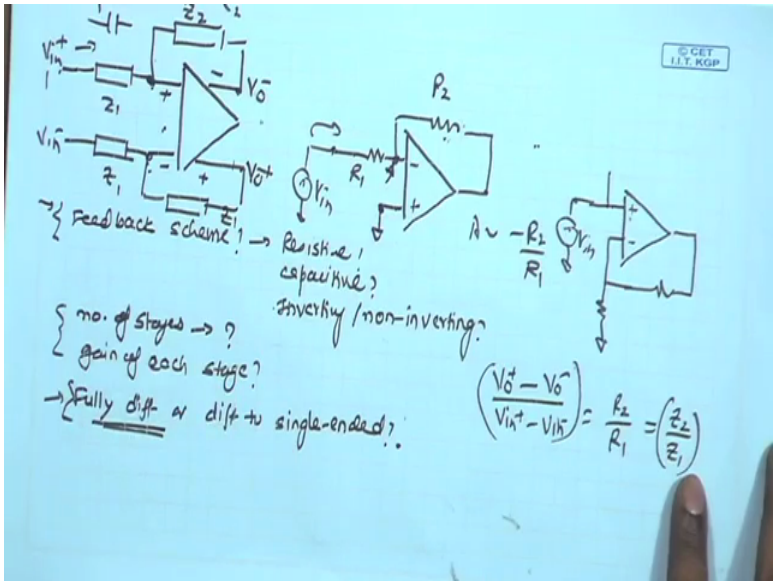

We are going to deeper into the discussion of fully differential amplifier. We are going to looking to transistors developmentation of the chip of the differential amplifier and look at the basic analysis starting from DC biasing then going towards the frequency response, stability analysis, buying analysis and so on, so that we can figure out how to achieve as derived set of matrices. So, we had seen at the topmost level we have arrive some designs and education the front end amplifier that translates to transistor level specification.

So, first we will try to see how to choose the particular topology and go for the transistor level design, and from there how to do the analysis for those particular specifications.

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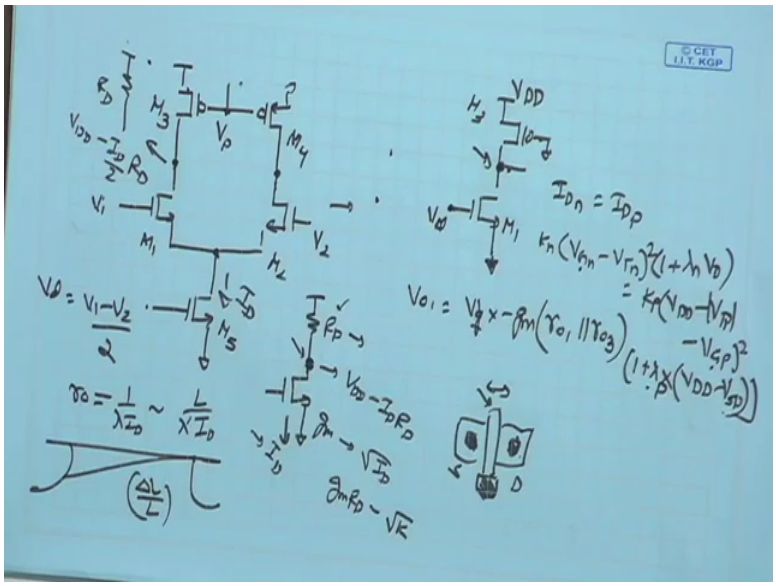

Let us get started with simple fully differential amplifier using MOSFET transistors. This is a single stage fully differential amplifier provided you have a bias point to V p you call this M 1, M 2, M 3, M 4, and M 5 and we are assuming that V p had been provided by appropriate biasing scheme and we will be discussing that very soon.

And here if we our concepts of differential amplifier operation for a fully differential signal we know that we can call this V 1 V 2 and the differential component for the signal can be identified as V 1 minus V 2 by 2 and for the differential half circuit I can represent the differential half circuit as this by putting an ac ground at the source of M 1, and M 3 gate also becomes ac ground for DC biased point and you having the v differential; what is the differential that is Vd is V 1 minus V 2 by 2.

So, you have Vd applied over here and we know that for this particular signal our output signal Vo 1 will be given by Vd times minus gm; sorry gm times the output resistance over here of resistance and over again which is ro 1 parallel ro 3. This is based on to a simple common source amplifier with an active load. And if the looking from the basics we understand what is the need of an active load. The main advantage of an active load is that you can give us large gain without compromising from that DC biased point.

So, if we want large gain with a passive load what is the criteria if you are looking for a common source amplifier with a resistive load or a differential amplifier with the resistive load in order to increase the gain there are two options either you increase the

bias current or you increase the R D and larger that use R D means larger and larger area because a passive resistance a larger amount of area. So, using a passive resistance also you can get large area. For example, the two options that I have here took for achieving a larger gain is gm and R D.

So, if I go for increase in R D for a given bias current we know that the DC biased point over here is given by V DD minus I D R D will be coming down. So, if I am fixing my bias current to I D and trying to increase the gain by increasing R D then I know that the DC biased point over here will going down and down. And I know that for symmetric swing or maximum possible swing I should bias this DC point at the output close to the midpoint of maximum and minimum allowed voltages.

So, in a circuit if we are finding out what is the maximum allowed voltage over here at this node to keep the transistors in saturation and correspondingly what is the minimal allowed voltage that gives you the range of the signal swing that you can have at this point. And a good DC bias point would be the midpoint of that.

So, if I am just going on increasing R D in a passive load registers load amplifier the DC point will be going down. Therefore, in order to maintain the same DC point the only option is that if I am increasing R D I must also reduce I D by the same amount so that the DC bias point remains close to the desired value. So, if I am increasing R D I must reduce I D by the same factor. So, that my DC bias point is not disturbed it is same as the previous desired value. In that case I know that gm is proportional to root I D.

So, if I am increasing R D factor of k and reducing I D by the same factor the gm R D product is going to go up by root k. That means you will be able to increase the overall gain by root k by increasing the R D and reducing I D by the same along why I keeping the DC bias point intact.

So, even with the passive load even get large gain and we are similar tradeoffs with other important quantity which we were bandwidth. So, just like I am increasing the R D ultimately the R D times constant at this point will become larger and larger. And in order to calculate bandwidth you can look at the R equivalent at this node if the R D is increasing if the r equivalent at this node also goes up. As a result your bandwidth which is also go to come down. So, you will do have the similar constrains, similar tradeoffs

trying to increase the gain by increasing R D you are reducing the bandwidth, but the other is important factor is the area.

So, the area of the resistor increases proportional to with the value and as a result you will end up consuming a huge amount of area if you are trying to go for larger passive resistance. So, in order to avoid that we can rather up for active loads where you can get very large value of small signal resistance provided by these MOSFETs by controlling some parameters while the bias current or the channel length. So, we know that the small signal resistance of the MOSFETs is given by 1 upon lambda I D; lambda itself is going to reduce if I am increasing the channel length.

So, I can write this as lambda dash L upon id. So, if you are having larger and larger channel length we know that some of the device. The effective delta L power channel modulation the delta L by L factor will be smaller than if you have larger L as a result a larger channel length will ensure a larger ro and smaller lambda. So, if lambda can be written as lambda dash upon L by lambda dash is independent of L. So, in order to increase ro or the small signal resistance for the MOSFET I have two options: I can reduce the I D or I can increase the L. Increasing the L does not drastically increase the area of the MOSFET, because L consumes relatively smaller footprint in the entire MOSFET.

So, if I am looking at the top view of the MOSFET this is the source, this is the drain, this small squares are the contacts that you make with the source and the drain regions and then you have the gate contact that you make with the polysilicon gate. So, the gate generally does not consume so much area channel length does not consume so much area. So, by increasing this dimension you are not you are sacrificed in too much of area. And the other strong option that I have for interesting the gain is the I D I can lower the bias current in the circuit to achieve larger gain.

So, there I can use active load I can employ smaller and smaller bias current and longer channel lengths to have are large ro and at the same time with large gain without sacrificing the area significantly. As we will see that of course, reducing the bias current can tradeoff with other important specifications: one of them of course is the bandwidth, and other one being noise as we go towards small signal analysis, frequency response and in noise analysis we will see that the bias current played an important role in

determining noise. And hence we cannot arbitrary lower the I D to increase ro, because that is one of the main reasons why we are using the differential amplifier with active load.

Now, let us ask the question regard in a DC bias point. We know that for a passive load common source amplifier or a passive load differential amplifier the DC bias point at the output is well defined, because if you are biasing the differential amplifier with a current I D bias current I D and you have a resistive load over here; both of them R D R D, I know that the DC bias point you going to be V DD minus I D R D. So, if I am replacing this by R D the DC bias point is V DD minus I D by 2 times R D if I D is the total bias current of the tail current.

And R D is the passive component and it can also bandwidth may not very precise in integrated circuit design with using proper layout techniques we can ensure that the two R D the passive R D on the two drains they are very close together. We can match two R D see in subsequent sessions, we can match two R D value very closely within 0.1 percent, but the absolute values can vary ad hoc vary even 10 percent, but still 10 percent is within limit. So, if you are trying to bias this with say a 0.5 volt it may end up being 0.55 volt or 0.45 volts till first key simple big tolerable. So, we have to keep that much margin, but still it is relatively well defined.

There are ways in which we can define the current source also pretty precisely, and we can have very well controlled kind of source. You can have a current reference as we were see in the course we can design very precise current references to appropriate techniques and we can have a very well defined current source. Once you have a precise current reference locate it somewhere in the chip you can copy that current reference using (Refer Time: 10:44) have different points. If you want more accuracy you can use cascode current source and have more accurate control on the current source.

So, current is a you can have much better control. Even if the control the current value, because when we are forming current mirrors they are also once side having the reference current, the transistors which are forming the mirrors they also can be matched to NMOS transistors or two PMOS transistors can be matched very well by appropriate layout techniques. And therefore, you can have current defined in a very accurate fashion.

So, if you are having current defined in an accurate fashion then for resistive load only the variations in absolute value of R D becomes the limiting factor on the DC bias point. But if the technology is good and the absolute variation in R D is within say plus minus 10 percent then you still have good control on the DC bias point. Whereas, if you go for the active load there we know that the output DC bias point is primarily determined by the channel length modulation factors, because here what you are trying to do you are finding to establish a DC current in M 1 with the help of the tail current source. The gate voltage of M 1 is also fixed, gate voltage of M 3 is also fixed.

And therefore, the output DC point is goes to be determined only by the force to drain voltages, because the drain current you are enforcing a certain value gate voltages you are enforcing a certain value, and therefore you are left with the V ds to determine the output DC point and the V ds in turn depends upon the channel length modulation factor. So, even if you look at this simple example of a common source amplifier with active load in order to determine the output DC point we will equate I D n into I D p and in this case we know that k n times the V gs V Gn minus V tn square should be equal to the k p times the V sg where V s is V DD minus mod V tp minus V GP square.

Now, here if we look at these quantities the V Gn is fixed V GP is fixed because the biasing point of the gate voltage of M 3 and M 1 they are being the remainder of circuits. So, we are already biasing M 3 and M 1 gates appropriately. So, the V Gn V GP become fixed V t and V tp can vary from the by significantly k n and k p can also vary. And then you have a channel in modulation factor 1 plus lambda n times the Vd is by referenced with the common source amplifier is this force ground then we have the Vd directly coming over here and then the PMOS equation I will have V SD.

So, V SD its basically V DD minus V SD. Therefore, we can see that if you want to solve for V SD ultimately is going to determined by the ratio of k n k p ratio of the lambda n and lambda p times; sorry 1 plus lambda V SD. So, I have to 1 plus lambda p times V SD. So, here you will be finding out the expression for V d which is going to determine by the lambda p lambda n ratio and also the k n k p ratio. And all these values the k n k p ratio that is the (Refer Time: 14:08) parameters of NMOS PMOS and the lambda n lambda p ratios can vary a lot from device to device. And therefore, we do not have much control on the output DC point over here.

And therefore, one of the main limitation of the active load device is that we need to make sure by appropriate biasing scheme that the output DC point is well defined. And for that will take help of a common mode feedback that will be study you in the next session. Apart from the output DC point we also need to look at the frequency response considerations. To figure out the frequency response as we said the limitation as compared to the passive load can be similar.

So, as you are trying to increase the gain; as we said we have the two parameters I D and L. So, once again reducing the I D or increasing the L both of them are going to have negative you know implication on the bandwidth enhance frequency response so that concern as it is. So, apart from the DC bias point if we consider some other aspects related to the circuit. We will see later that which is the two some very important parameters like common mode rejection ratio or power supply rejection ratio also the choice of PMOS device or PMOS active device can play an important role.

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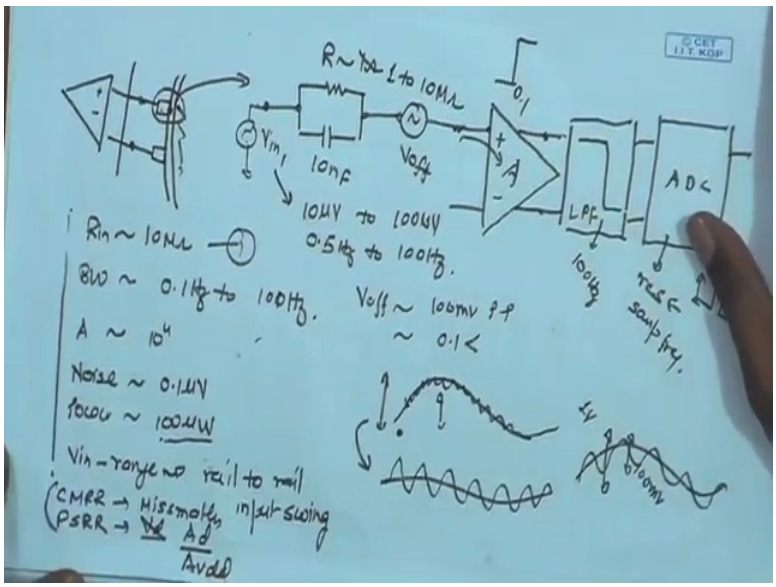

So, in our earlier specifications; we have not discussed two very important characteristics of differential front ends that is the common mode rejection ratio and power supply rejection ratio.

So, we will visit these a little later in the discussion. We know that common mode rejection ratio for differential amplifier is the gain of the ratio of differential gain and common mode gain. And good differential amplifier should have a very high common

mode rejection ratio. We have often we are using a fully differential topology and for a fully differential topology as long as the signal is remaining differential also of the chain. CMRR ideally it may not play an important role, but there are other constraints with there are other considerations with the mismatch that will also degrade CMRR even for a fully differential topology. So, we will see that in case of fully differential amplifier the CMRR is mainly degraded because of mismatches. So, this will require separate discussion.

Another important factor is PSRR- power supply rejection ratio that basically determines by the ratio of the signal gain divided by the gain from power supply noise to the output. So, we say this is the differential gain upon or let me write it as differential gain Ad upon A vdd; that means, if you imagine that the power supply itself is having some noise over here and how does that power supply noise translate to the output of the amplifier. So, that gain is the defined as A vdd. And for a good deferential operation for a clean amplifier operation I would write my A vdd to be very small even if the power supply is having some noise they should not directly translate to the output of the amplifier.

Once again the choice of load can have significant impact on the power supply noise also and we need to take into consideration PSRR. So, we will see in subsequent discussion that these two parameters CMRR PSRR also determined by the load condition. So, they are influenced by the load conditions. And I will try to arrive at the expression for PSRR and I will see if how the load the choice of load in the appropriate biasing technologies play a role in determining these two.

So, let us continue our discussion on the passive scheme and the common mode rejection ratio and the common mode feedback in the subsequent session. So, we will stop here before we start at the next module.