Analog Circuits and Systems through SPICE Simulation
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Lecture - 10
Basic Analog Design Part III (Contd.)

Good afternoon everyone and welcome to. Start with a brief introduction of differential amplifier. So, far we have covered the basic common source amplifier with active load, we have gone through the analysis, DC analysis, swing analysis frequency response and also noise analysis. Now we are going to proceed towards differential amplifier which is going to be the first stage offer op-amp or 2 stage op-amp which is going to be employed in building the low noise front end amplifier for our analog front end. So, let us start our discussion on differential amplifiers.

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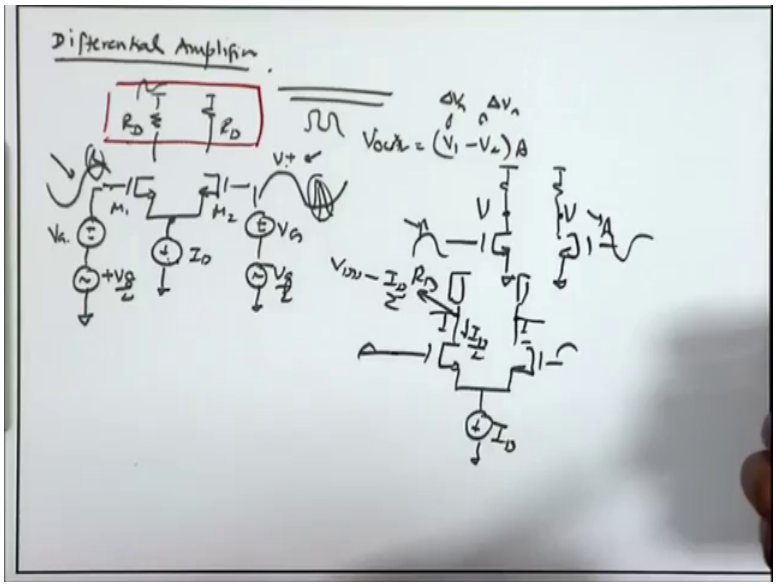

Now, for differential operation the common topology that is used we have a bias current id, which is used to supply current to 2 differential pairs M 1 and M 2 and you have load resistances. Now this load can be active load just like what we have studied earlier it can be passive load it can be P mos.

Now, all of us are aware of what are the basic advantage of differential operation right. So, differential operation ideally is able to reject any common mode disturbance on both the inputs. Say if you are having an input signal in a differential mode that is the small

signal applied on the top of the DC voltage VG if they having opposite polarity. So, this is minus VG by 2 and on this one again DC voltage VG and plus VG by 2.

So, here these 2 differential signals are going to produce corresponding differential signal as the output, any common signal mode that comes in suppose you are having at a particular time instance some disturbance, there is a kink on both sides. So, ideally a differential circuit should be able to reject this kind of common mode disturbance on the input signal that is the advantage of a differential circuit. So specially, when we are going towards s o c we are trying to integrate analog in digital together, apart from the external noise sources there are many other on chip noise source that can come into picture like along with the digital circuit, you can have some clock signal going in nearby and it can create some common mode noise if VDD can have some noise.

So, all those appear as common mode noise, and a fully differential circuit operation can reject that common mode noise. The main operation of the differential amplifier is the output should be A times V 1 minus V 2 or V plus minus V minus, let me call it V out should be A times V 1 minus V 2. Where if you are having common disturbance on both of them delta V, delta V which is a common noise V n, V n that should get cancelled.

Let us ideal operation of a common of a differential amplifier, cancelling out any common mode disturbance. Now here if we talk about the differential operation like what is the operation of this amplifier if we consider differential signal, we are applying a differential signal what happens to the output signal and what happens to the node over here why are the using current source that can be a question to start with, can we do it without the current source also. So, they are if I try to answer this, if I am directly connecting 2 common source amplifier ground, ground and then you are having the input signal may be differential and on the top of that you have some common mode disturbance coming at some point. So, this is this kink is a common mode disturbance coming at some point.

Can this circuits still give us can this circuits still give us can this circuits still reject the common mode signal over here. So, once again if I see if we do not have this current source, this common signal over here that is definitely going to increase the current in both these branches and as a result the output is going to this is going to translate to both the outputs equally, as long as a circuits are well matched. So, if I talk about this single

ended operation, if I am looking at the single ended output we are not able to reject the common mode signal whereas, if I am talking about a current source suppose I have an ideal current source tide at this node, under that condition if I am having a common mode out input.

That means, both the inputs are changing together assuming that this transistors are remaining in saturation, the currents will divide equally because V g s is same both the inputs are changing by the same amount. Therefore, the 2 currents are going to be same and therefore, depending upon what load do we have over here the 2 voltages over here are going to remain more less constant, because this currents are constant as long as this transistor in saturation and this current is constant this loads are going to this voltages are going to be constant.

Suppose you have a resistive load, the ID will be dividing equally between ID by 2 from the 2 sides and therefore, the output voltage over here is just VDD minus ID by 2 times RD. So, idea it will reject any common mode signal it will not have any fluctuation because of the common mode signal that is the main advantage of having a differential operation. So, now, how do we look at the common mode and differential operation of such circuit? So, here once again we have already seen how to implement this ID. And therefore, we are just going to replace it with our actual current source will later before that; let us do some analysis and try to find out the behavior of this common source terminal.

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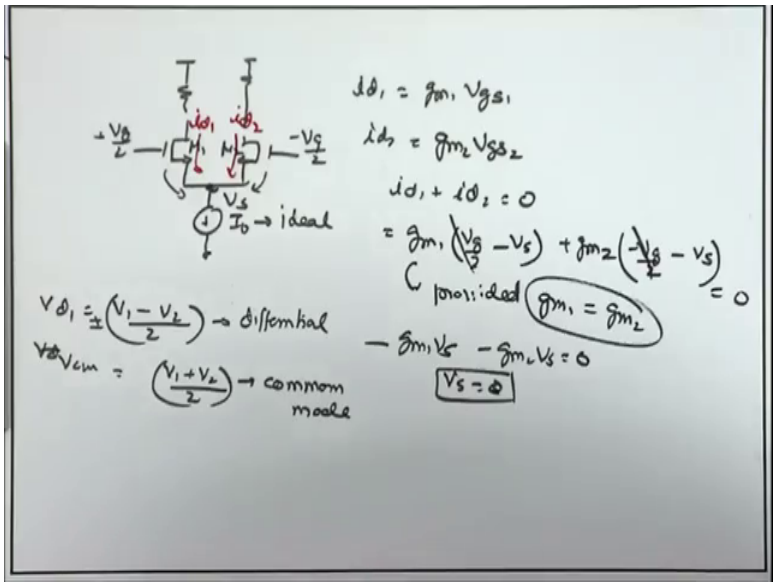

If I put the load connected here, if I assume that both the transistors are in saturation and I have a good current source close to ideal, and I am applying a differential signal say plus VG by 2 here minus VG by 2 here. Just looking at the small signal I am forgetting about the DC and just looking about the small signal plus VG by 2 here minus VG by 2 here.

So, what happens to this Vs? What can we say about the small signal at the source I am just trying to talk about the small change in Vs that may appear because of the small differential signal applied at the 2 gates of M 1 and M 2. So, if I ignore the channel length modulation of M 1 and M 2 effectively I am trying to change the VGs of M 1 I am also trying to change the VGs of M 2. And we know that when you try to change the VGs you are going to get a small signal current flowing from drain to source of M 1 which is equal to gm 1 VGs 1.

So, if I say the small signal current over here is ID 1 and the small signal current over here is ID 2 what is ID 1? If I ignore channel length modulation ID 1 can be written as n gm 1 times VGs 1, and ID 2 likewise can be written as gm 2 times VGs 2. Now the third current over here that is ID, this is ideal current source ideally it should remain constant it should not change therefore, the small signal currents ID 1 and ID 2 should add to 0. Under all conditions ID 1 plus ID 2 should add to 0, because if I just the small changes in the current I capital ID 1 and capital ID 2.

And therefore, I can write down gm 1, what is the gs one VG by 2 minus Vs plus gm 2, once again what is VG 2 that is we have assume differential signal. So, that becomes minus V g 2 minus VG by 2 minus Vs VGs 2 that should be equal to 0. If you see the first term gets cancelled minus gm 2 Vg, gm 1 VG provided gm 1 is equal to gm 2. Say this condition is met the first 2 terms get cancelled and I am just left with gm 1 Vs minus gm 2 Vs equal to 0, which implies that Vs must be equal to 0. What was that mean? That Vs is not having any small signal.

Therefore, we can say that this is now an AC ground. So, basically the joint source terminal of this 2 pairs M 1 and m twos acting like an AC ground as long as we are having gm 1 and gm 2 matched. So, once again we need good matching between these 2 n mos pairs for a good differential amplifier. So, that we can have a reliable AC ground established at this point and what if you know your signal is not fully differential, rather than VG plus plus VG by 2 minus VG by 2 we can have this at the constant terminal and you can have a input which is coming over here.

So, in that case we can decompose the input into V common mode and V differential. So, we can always write down the differential voltages V 1 minus V 2 by 2, and the differential voltage f plus minus V 1 minus V 2 by 2 and the V common mode as V 1 plus V 2 by 2. And we have to see the behavior of the circuit for the common mode voltage separately and the differential voltage separately. So, I can apply plus or VD 1 minus VD 1 that becomes a differential operation, and then I can treat the circuit for the differential mode find out what is the output signal for the differential. And second, I can also look at the behavior of the circuit to the common mode signal.

Ultimately, if I add these 2 it is just the input signal V 1 and V 2. If I am just breaking down any arbitrary signal V 1 and V 2 applied at the gate, provided their you know small signal DC voltages are quite close. So, that gm does not change important point is that the gm should be almost you know very similar that will happen if you have a DC point same

So, provided these V 1 and V 2 are small signals, I can decompose them into the differential signal and the common mode signal and then analyze the effect of this differential signal and the common mode signal separately and then add them up, because if you are talking about small signal model that is a linear model right. So,

superposition will hold true linear superposition will hold true. So, you can just unlies the effect of this differential signal separately find out the output signal resulting from the V differential signal, likewise find out the output signal resulting from the common mode signal add them 2 together and that gives me the overall response of the circuit on the signals V 1 and V 2 applied at the input terminal.

That is how we can analyze any arbitrary signal at the input. So, for the differential case one thing we have already figured out, if the if I am looking at the differential operation plus VD by 2 minus VD by 2, one thing we have already seen that the Vs is AC ground. We can for the differential mode we can always treat Vs as the AC ground, in that case I can talk about the differential half circuit right for differential half circuit I can treat the source terminal at AC ground and then my amplifier for a given VG by 2 just a common source amplifier same as before what we have done.

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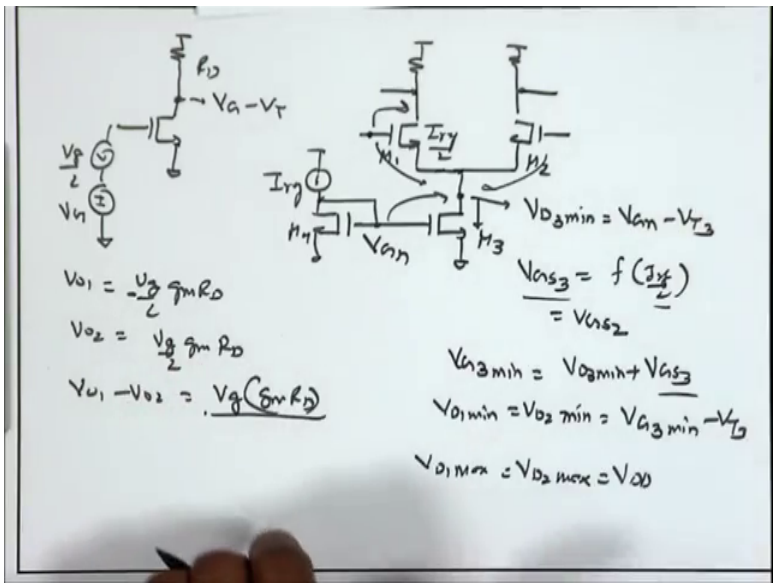

And the entire analysis whether we talk about the DC analysis, small signal analysis frequency response remain same. Something is going to differ and that is our swing analysis and we also need to address what is going to happen to our noise analysis. Is the noise analysis going to remain same or we need to have any difference.

So, for the point of view of DC once again we know that there is a bias current coming over here, you have some c gate voltage over here and the minimum drain voltage that you can have is going to be suppose if there is a DC voltage capital VG that is the DC

bias points of both the sides, and the minimum output voltage you can have is again going to be VG minus Vt, but this VG is also going to be determine by some other constrain and that is given by the constrain produced by the current source. So, for AC analysis the common point common source point is you know AC ground Vs equal to 0, but from the point of view of dc, I need to look at the capital VG which can accommodate enough drain to sources voltage for the current source.

So, if I talk about the AC analysis and try to go back and place my current source over here, the one we have already used in our common source amplifier. So, you have some I ref you are having diode connected transistor, and then you are trying to mirror this. So, this is the current source, non ideal current source you have of course, have some finite output resistance, but close to an no good current source what we have now.

And we know that corresponding to this I ref how to calculate the VGn equate the equation for current in say call it M 1 M 2 M 3 and M 4. We can equate the equation of current in MOSFET and find out the VGn it is a require to support the I ref and therefore, under that condition we know what is the minimum drain voltage that M 3 can have. So, I can say VD 3 min is going to be VGn minus VT call it VT 3. Now I know that if these are having a same ratio I have I ref by 2 flowing through each of these for the DC biasing point or DC biasing point is gate voltage is capital VG and I have IRf by 2, IRf by 2 flowing through both of them and therefore, once again I can find out the required VGs 3 which is going to be a function of I ref by 2 because we know I ref by 2 is once again VGs 3 minus VT 3 square times the kn. So, I can obtain VGs 3 as well as VGs 2 both of them are equal as long as the 2 devices are well matched.

And then for a given minimum VD 3 we can say what is going to be the minimum gate voltage that you can have over here. So, that becomes VG 3 min that is equal to VD 3 min plus VGs 3. And then for this particular DC voltage at the gate we can find out what is the VD 1 min or VD 2 min which is going to be V G 3 min minus VT 3. So, this gives us the limit on the minimum voltage or the drain voltage that I can have for M 1 and M 2; for the resistive load the maximum voltage that I can have at M 1 and M 2 drain is just VDD. So, VD1 max equal to VD 2 max is just equal to VDD. So, the upper point is not change VD 1 max and VD 2 max do not change, but VD 1 min and VD 2 min they are again slightly higher because you need to have enough VDS for M 3. The VD this node is not at DC ground, this is an AC ground from the point of view of DC you do need

some minimum drain voltage for M 3 to keep M 3 in saturation and make it behave like a good current source that is the difference comes with respect to the signal swing.

Now, in case of differential analysis we already had seen that this is a differential half circuit. So, I am if I am applying a fully differential signal that is plus VG by 2 on one gate, and minus VG by 2 on other gate this is a AC ground and therefore, the gain is going to be just VG by 2 times gm RD likewise on the other side VG by 2 times gm RD and you take the difference. So, V o 1 is V g by 2 times gm RD with a minus sign and Vo 2 likewise plus VG by 2 minus VG by 2 times minus gm RD. So, plus you are having another plus sign and therefore, the output signal which is V o 1 minus V o 2, will be just VG times gm rd. So, this is the gain we are just getting gm RD as the small signal gain Vo 1 minus Vo 2 divided by V in 1 minus V in 2.

So, the small signal analysis for the differential operation remains same; what about the small signal analysis for the common mode case. So, for the common mode case how do we deal with it? So, if I have to write if I have to draw the circuit for the common mode operation, what we are talking about is applying the same DC or same AC signal at the 2 gates. So, basically we are going to pull these 2 gate voltages up and down by same amount that is a common mode. So, under that condition we can say the source voltages are anyway common, the 2 transistors are very well matched the gate voltages are also common we are having a same gate voltages.

So, basically we are tying down the tying up th 2 gates together. V as long as the 2 MOSFETs are mashed and the 2 RDs are mashed, we expect that the drain voltages are also going to be same they are going to change by similar fashion. Therefore, we can tie them also together and we can then arrive at a equivalent common mode half circuit by tying this 2 branches together because gate voltage is same, the source voltage is same, and the drain voltage is same. But in this case defiantly we do not expect that this node is going to be AC ground right because again if I assume that this is behaving like a good current source, this is providing an ideal current, DC current this 2 VGs will remain almost same this will they will remain almost constant.

So, if I am pulling the VG up is order to keep the same VGs the source will also go up and down up and down. So, source is no longer AC ground for common mode operation; we are trying to pull up the gate voltages the source voltage will also be pulled up by

same amount so that the VGs of DC transistor remain same and so that they keep supporting a same current I Ref by 2.

So, source is no longer AC ground. So, in the common mode half circuit I need to consider the transistor M 3 also, I cannot just ignore it I cannot put an AC ground over here. Now if I talk about M 3 what is a role of M 3, how do I model m threes behavior on this circuit. Once again as long as M 3 is in saturation this is a n mos transistor with gate voltage constant, looking into the drain I have an equivalent small signal resistant provided by M 3 and that is just equal to r o 3.

So, again for small signal analysis I can replace M 3 by its equivalent small signal resistance r o 3.

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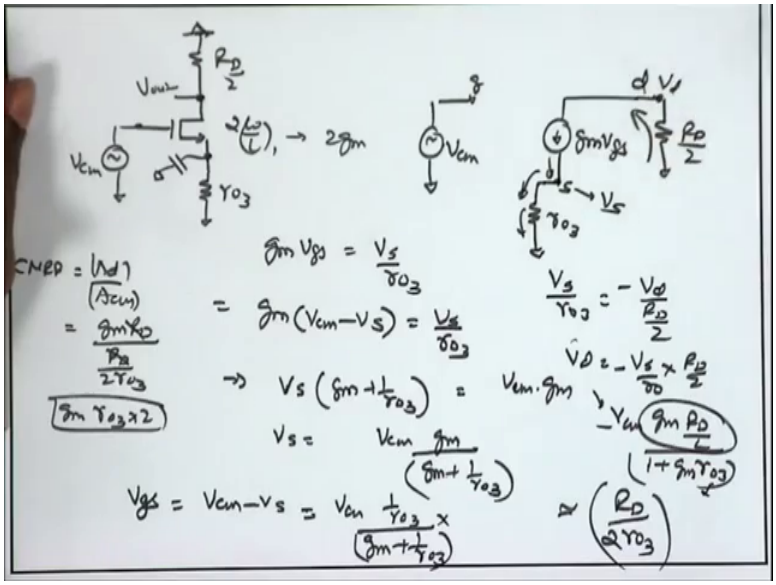

So, I can replace M 3 by r o 3, I am tying the 2 transistors M 1 and M 2 together. So, this becomes 2 times w by L of individual M 1 and M 2, I am also tying the 2 RDs together. So, this is becomes RD by 2 and therefore, this is my common mode half circuit right. So, I just tie the 2 transistors together. So, of course, if I talk about the gm now this is 2 times you know w by L I have tie 2 both the transistors together and the ID in this combined transistor is equal to I ref, initially the 2 transistors were having I ref by 2 I ref by 2 now this combined transistor of length 2 times w by L is having a total current of I ref. So, we have w by L 2 I ref twice and therefore, we are having gm which is 2 times gm of the individual transistors. So, now, I can do the small signal analysis at if you are

applying a common mode Vcm the small signal Vcm at the gate, what is the output voltage V out small signal output voltage resulting from this.

Now, this is something like a common source amplifier this common source amplifier is this source region ration resistance. Many of you might have seen it those who are you know into analog courses teaching and they search, we are very familiar with this topology common source amplifier with a source region ration resistance we just going to be quickly derive it how are we going to do this your now in a normal common source amplifier we have this source connected to AC ground, but now we do not have this as ground we have an r o 3 over here.

Again quickly derive the small signal model we have Vcm applied at the gate, this is the gate terminal we are having gm VGs as the current source between the drain and the source, between the drain and the VDD I have RD by 2 if I can call it RD by 2 I am ignoring Ro by 2 for the timing for a simplicity as compare to RD by 2 and then my analysis relatively simple I have r o 3 between the source and the AC ground. Remember RD is between the drain and VDD, for small signal VDD is also AC ground. So, RD by 2 appear between drain and the AC ground ro 3 appear between the source and the AC ground.

Now, we have this small signal equivalent circuit for this case and I can try to solve it and find out what is the relationship of VD as compare to Vcm. So, what we can say is I can write the KCL over here I can assign I can say Vgm VGs is the current coming here which is just equal to V s which is the node voltage over here upon r o 3. Whatever current comes the same current goes Vs upon ro 3 is the current flowing through ro 3 which is equal to gm VGs; where VG is Vcm Vs is the source voltage upon ro 3 and therefore, I can find out the expression for Vs gm plus 1 upon ro 3 that is equal to Vcm times gm therefore, Vs is Vcm times gm upon gm plus one upon ro 3 and therefore, VGs is going to be Vcm minus Vs right. So, I can write down VGs as Vcm minus this quantity. So, I have 1 minus this quantity. So, gm gets out and we have ro 3 upon gm plus one upon r o 3.

And then I can say what is going to happen to the small signal VD over here. So, whatever current is flowing from Vs to the ground, through ro 3 same current must exit through ro RD by 2. So, we do not have any other path. So, Vs upon ro 3 I can say Vs

upon ro 3 must be equal to minus the current flow here, which is minus VD upon RD by 2 therefore, this is just going to be VD is just going to be equal to Vs upon ro 3 times RD by 2 with the minus sign. So, I can write this down as Vcm times gm RD by 2 upon one plus gm ro 3.

So, basically gm RD upon one plus gm rs, this is the rs the source resistance in this case this is what we are getting. So, this is the original gain for the differential amplifier when this would have been source, this has would have been ground then we would get gm RD by2, but in the denominator now we have 1 plus gm ro 3 which can be a large number, go ro 3 is the intrinsic gain of the MOSFET can be must larger than one.

So in fact, this can be approximated as you can ignore this one and compare this with gm ro 3 and therefore, we can cancel this gm and we are left with RD bound 2 r o 3. So, this is the magnitude of the common mode gain that we are getting from the input to the output, and it tells us that if your ro 3 is large we are going to get very small common mode gain; the common mode voltage over here that the output voltage over here is not going to have a significant swing.

So, having a larger ro 3; that means, having a larger output impedance for the current mirror is going to be advantage, that is going to us a larger a small signal resistance and that is going to give us smaller common mode gain that is ideally required for a good differential amplifier. So, one of the very important parameter that is a require for the differential amplifier is common mode rejection ratio, that is defined as the differential gain versus the common mode gain.

So, how will the amplifier is amplifying the differential signal and how will it rejecting the common mode signal. So, we had see the in this case the differential gain is gm RD, common mode gain is RD upon 2 ro 3 therefore, the common mode rejection ratio if I have to say CMRR which is A differential upon A common mode magnitude, that is just gm RD upon RD upon 2 ro 3. So, basically gm times ro 3.

So, larger ro 3 is going to give us is going to conducive to good common mode rejection ratio that is going to give us a better differential amplifier operation. And we have seen how to make the ro 3 large one of the possibility is to increase the channel length of M 3.

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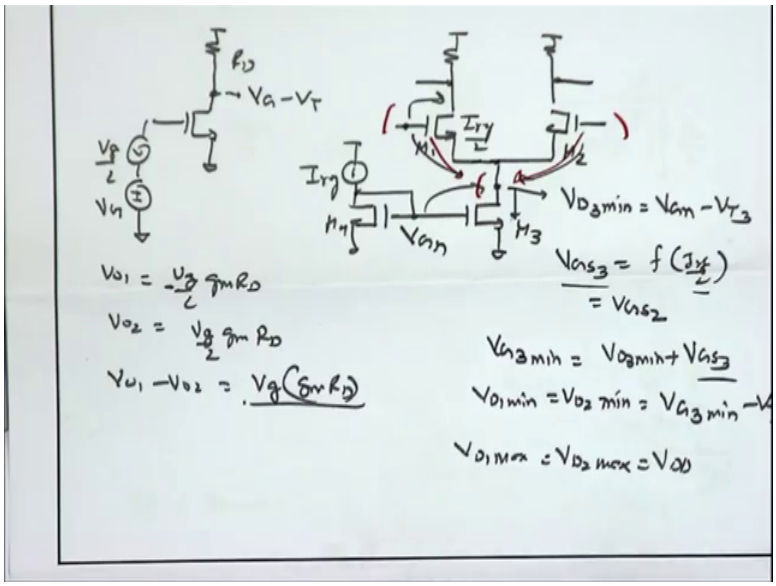

So, that we can have larger common mode rejection ratio larger ro 3; because remember ro 3 is one upon lambda ID and if you increase l lambda reduces. So, larger channel length of M 3 can be conducive to a better CMRR, but what is the disadvantage if I try to make the M 3 channel length larger the VGs required will be larger for a given current, but once again I can take w of M 3 large because from the point of view of ac, it may not you know it may not give you problem as for as the differential signal is concerned.

But once again if I talk about common mode response, if this is the common mode half circuit and if I am trying to make M 3 very large what happens? You are having some parasitic capacitance between this mode and ground which is resulting from several transistors M 1, M 2 as well as M 3 if I make M 3 very large once again this parasitic capacitance will go on increasing, and at higher frequencies the impedance combine impedance of this parasitic capacitance and ro 3 will drop, as a result the common mode rejection ratio will drop.

So, there are the tradeoffs. So, you can try to increase the w by L of the bottom current source transistor, you can try to make the channel length large, you can try to you know reduce the overhead voltage headroom required by M 3, then once again it if you are having larger size for this M 3 it increases up overall parasitic capacitance at this node and that is in turn can degrade the common mode rejection ratio at higher frequency

because it is going to you know reduce the impedance equiactive impedance between this node and ground.

So, there are always tradeoffs associated with differential amplifier designing. Now if this is regarding the differential operation and common mode operation the you know the small signal analysis differential gain and common mode gain for the simple differential amplifier with resistive load. We have also seen the swing we had seen the DC analysis and the freq small signal analysis. Frequency analysis for the common mode we dis if we discuss what is going to happen if you make the M 3 large in order to have a larger l or in order to have a smaller headroom that is going to increase this parasitic capacitance and again it is going to reduce a common mode rejection ratio that is un in desirable thing.

Regarding differential case a circuit is same as what we have analyze in the common source example. So, we do not need to talk a lot about the differential case, frequency response is going to be more less similar as what we discussed in the common source case, in case you are having a source resistance over here the same thing you can apply the miller effect based on the capacitances. So, exactly the same expression that we obtain for the common source, no need to discuss it further for the time mean.

What about the noise. So, do we need to do something (Refer Time: 30:50) with the noise. So, we are talk about the differential operation what happens to the differential operation if we talking about the common mode that noise produced by this transistors? So, differential operation we are considering M 1. So, definitely you know the effect of noise on M 1 is going to be similar, we are going to do similar analysis M 2 also similar only thing that they have to take into account is that noises or noise voltage we do not consider their polarities, we are going to consider their mean square values though we cannot say that the value over here will be V n 1 minus V n 2, it is just the mean square value.

So, we need to look at the mean square noise at this point within the half circuit we just going to be same as what we did for common source. What about M 3? M 3 if I talk about the noise of M 3 we definitely having input referred noise over here I can convert the channel current noise into input noise voltage and therefore, I assume that it may have some effect at the output because here we have a noise voltage V n g square V n g 3 square and that may affect the 2 outputs over here.

So, what is that effect? So, are we are we concerned about the noise of M 3 in this case on the output. So, if we talk about M 1 and M 2 they are independent transistors their noises are not correlated therefore, we cannot cancel them out because of the differential operation. We have to look at V n 1 square and V n 2 square produced by M 1 and M 2 in the separate half circuits, but M 3 if we are talking about the effect of this noise on the 2 branches over here, this is common source this is the common noise source.

So, the effect of this common noise source on these 2 are correlated it is not independent source therefore, we can say that it will cancel out will not really require to consider the effect of the equivalent noise voltage of M 3 on the 2 outputs because it is going to have this is the same noise source producing the output voltages at this point and therefore, we can you know ignore the effect of this equivalent input referred noise of M 3, I am just be concerned about the noise of M 1 and M 2 which is a first order.

So, this is regarding the DC small signal swing and the noise analysis of differential amplifier with resistive load. Now in case of our designs that we are looking at, we are going to introduce active load differential amplifier with active load and we have already had discussions on the common source amplifier with active load how to do the analysis like the DC AC small signal and noise. So, now, if I replace this RD by P mos load, once again the entire analysis for the differential half circuit remain same, common mode half circuit once again you know remain similar to what we have done for the resistive case only thing is rather than RD we have a Ro coming over there.

So, let us you know briefly discuss the differential amplifier with active load, we are going to do deal with 2 kinds of load for the differential amplifier one is going to be current source load and another one is going to be current mirror load which are both going to be utilized in our frontend amplifier.

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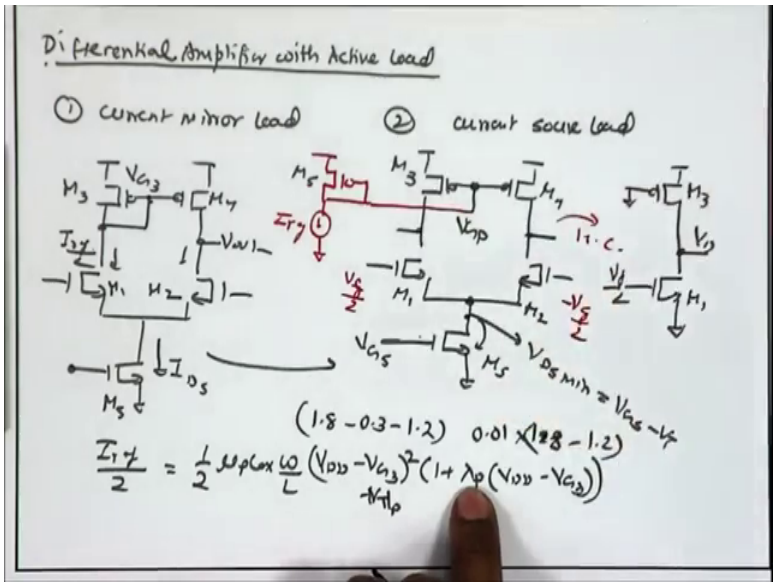

So, now drawing the reference branch it is assumed that this is connected to the reference branch.

Now the second one over here this is something you know very similar to what we have already done; common current source load and we assuming that this current source are once again coming from a reference P mos current mirror we do not have any connection over here, it is just to show that this 2 are just acting like current mirror. So, here the M 1 M 2, M 3, M 4 they are M 3 is forming current mirror with M 5 M 4 also forming current mirror with M 5. So, both of them are current mirrors with the reference branches M 5. In this case that is not the scenario, here you have one of the branches M 3 diode connected we are not using any reference branch we are not using a current mirror separate current mirror for obtaining VG.

Here as we have seen output is single ended we are taking the output only at one point, here the input as well as output both are differential. So, in this case input is differential output is single ended in this case input is differential output is also differential. So, this is fully differential amplifier and definitely it is going to have advantage whenever we are having several stages, multiple stages and you want to keep the signal differential all throughout with the prefer fully differential operation we do not want to convert it into single ended signal at any point unless we have process the signal sufficiently we have amplified sufficiently, now it is ready for digitization.

Even for digitization people now prefer fully differential amplifiers comparators which can have better robustness. So, in today's next signal design we can have the entire chain up to the adhesive amplifier in the comparators being completely differential fully differential. So, we are going to use this fully differential amplifier as the main amplifier in our design this is going to be the first stage of our frontend amplifier, but we are going to need assistance from another current mirror load amplifier with the single ended we will see why.

Now if I talk about the current source load here once again if I draw analogy we are having the differential signal VG by 2 plus minus, this node becomes an AC ground this is the DC bias provided by the reference branch, this again becomes an AC ground therefore, the circuit of this is very similar to what we have already done today this is an AC ground the input signal was applied here plus V g by 2, and this is an AC ground is M 1 and this is M 3. Which is the half circuit and therefore, the DC analysis, small signal analysis, frequency response, noise analysis, everything remain same only thing that we have to remember is the signal swing is going to have another factor of VD s call it M 5 VD s 5.

Because depending upon the V g 5 we need a minimum voltage here VD 5 min equal to V G 5 minus V T, and then on the top of that we have this transistor that is the only difference we have just discuss in case of the resistive load also. So, we are having some voltage headroom consumed by M 5 we say this M 5 current source is consuming some minimum voltage headroom and.

Apart from that rest of the things is so; analysis for the differential circuit remains same as what we have done. The concentration regarding the bandwidth the noise and the small signal gain all remain same. So, we do not have to discuss much about this four analysis; however, we have to discuss something about the biasing how do we bias the DC nodes, the drain nodes.

So, while discussing the single ended common source amplifier with active load we considered we discuss a problem that VD is you know very ill define. We do not have a very good control of V d. So, if we recall our derivation of the VD, we saw that this VD is going to be strongly dependent upon the lambda and therefore, it is not a very well

defined quantity, but in differential circuits we do have some mechanisms through which we can try to stabilize the V D.

So, we will see that how to you know with the help of the second amplifier over here which is the amplifier with current mirror load, we can obtain a desired the d c point at the output of this first amplifier. What about is second one it is going to help the first one, but before that it has to help itself does it have a well defined DC point? If the answer is yes then this guy can help the second one, but if this itself is does not have a well defined DC point t the output then we can remember the announcement make by the you know air hostesses is to wears mask first a of all it should help itself. So, let us see whether this can help itself.

So, how do we define the DC point at the output of this stage? So, we are having a different kind of load one of them is diode connected; and if you assume that this m 5 is acting like a good current source where ID 5 it is relatively constant M 5 is remaining in saturation for common mode as long as these 2 signals are close together gate voltage are close together suppose if signal is 0, the both the gate voltages are having same DC point I ref will going to define divide equally between these 2 nodes.

Therefore, on this branch I have I ref by 2 and this is something similar to our reference branch of the current mirror. So, this can produce a reference gate voltage VG3 using the quadratic dependency. So, this V g 3 is not strongly dependent upon lambda, it is having quadratic dependency I can solve I ref by equal to 1 upon 2 mu P cox w by L, V s g which is you know VD d minus VD 3 square be one plus lambda p V s d which is once again VD D minus you know V g 3.

And assuming you know V g 3 is going to be V few tens or hundreds of milli volt below VD d or below V again another term V t p mod V t p missed it. So, again the lambda dependency is much weaker because here you have a much stronger dependency determined by the square term or the quadratic term. So, here the V g 3 is not primarily determined by the lambda rather which is determined by the quadratic term. So, we have a scenario similar to the diode connected branch of the reference current source and therefore, we do have a well defined a relatively well defined V g 3.

now once this VG3 is available it is applied to the gate of end 4 and therefore, this is again acting like a current mirror this is a reference branch of the current mirror this is

something like the output branch of the current mirror. As long as both the input voltages over here are close if I talk about DC condition, we are having I ref by 2 in both the branches V g is same for both of them, V s g is same for both M 3 M 4, if these 2 transistors are matched we can assume that the DC voltage here is also going to be close to the DC voltage at this point. So, this current mirror action is ensuring a relatively well defined DC voltage at the output in this circuit. So, we have a relatively well defined DC point over here which is determined by Vsg of M 3.

Here the V out is not strongly dependent upon lambda and remember when it is dependent upon lambda the problem is that lambda is very small and it requires a very large changing VD, the source to drain voltage to accommodate for any imbalance, where as in case of the quadratic dependence it is much stronger dependence on VG 3. So, here V G 3 is getting detected by the quadratic dependence I can all together ignore this value. So, that talk about say some value practical values for 1.8 nanometer this is 1.8 VT3 close to say 0.3.

So, you are having 0.3 and VG3 will be close to you know VD d. So, that you have a overdrive voltage of around say point 2 one 3 volts. So, there is something like 1.2 or 1.3 something like that. So, you have a few hundreds of millivolt overdrive, this is the overdrive voltage V s g minus V T p. We are talking about something like 0.3 0.4 volts maybe lower than that if your current is smaller may be 0.1 volt and lower.

So, this quantity can be say 0.01 and once again this is 12 V sorry 1.8 minus VG3 around 1.2. So, as compare to the first term the second term is very small one point taken as a 0.2 times 0.01 because this lambda factor the dependency on the second term is much smaller. And therefore, VG3 is going to be determine mainly by or the VG3 is mainly determined by the quadratic term and not so, much by the lambda term. In earlier case in this particular case the VG3 is fixed we are fixing VG3 we forcing the VG3 equal to the V g of M 5. So, there we do not have any chance of adjusting VG3 it is fixed or dictated by the V g of M 5, but in this case the VG3 is being set by the I ref by 2, it is not dictated by another branch.

So, it is setting the VG3 by the dependence you know dependence on threshold voltage of M 3 and w by L f m three. So, basically the w by L 3 and threshold voltage of M 3 is going to determine what is my VG3 and as a result for common mode operation I am

looking at only the DC conditions these 2 branches being very well match the V out over here the DC condition is going to be equal to V G3.

So, I have a very well defined DC point and this can be used to help our first amplifier which has yield defined AC DC point.

Thanks a lot, we will see you tomorrow. Good night all of you.