Millimeter Wave Technology
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Module 6
Lecture No 31
Noise and Link Budget

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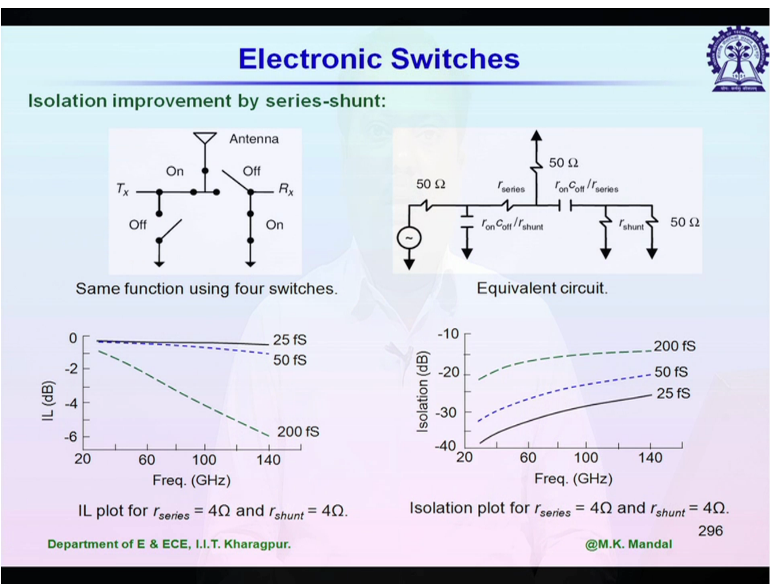

Okay so, first part we will continue with the electronic switches and then we will move to millimetre wave link budget and noise calculation and in presence of noise how we characterise any millimetre wave system. So, let us continue with electronic switches, last day we were discussing about a given switch, we can use it in shunt configuration as well as in series configuration. Now, usually looking at value typical capacitance or resistance values a few Ohms or capacitance a few pico farads that we have seen that in shunt configuration the switch will give better isolation. Now let us say whatever isolation we are obtaining from a given switch it is not enough, so in that case how we can improve the isolation further. So in that case we can use the same switch 2 number in series-shunt configuration, so here is one example.

So you can see one antenna, it is connected to receiver side and transmitter side, so now when the transmitter is connected to antenna in that case the switch whatever we are using in series configuration, it is in ON condition and in shunt configuration it is in OFF condition. So that means in equivalent circuit in right-hand side shown here, so in ON condition the switch will replace by its equivalent resistance R series and in OFF condition we will replace it by equivalent capacitance, which is c off and in this situation we call it a series-shunt

configuration. Similarly, right-hand side can be modelled, right-hand side together these 2 switches it forms a series-shunt switch and it is in OFF condition, so the switch or a PIN diode which is OFF, we represent it by c off and the switch which is in ON condition, we will represent it by series resistance, which is grounded.

So now how isolation improves in this case? So we see let us consider the switch which is in OFF condition that is the receiver side, so this PIN diode the first one it is open circuited, so it is represented by a capacitor so capacitor will give you some isolation. For the second pin diode it is switched ON, so if there is any RF signal it will be further grounded, so we have actually isolation improvement from the contribution of these 2 switches, but looking at the insertion loss value it will not be that good if I consider now left-hand side or the transmitter side, so in that case insertion loss will increase because of the resistance and the capacitor because in addition to the resister, we have a capacitor which is also grounding some part of the RF signal so insertion loss it will be poor.

But anyway, for any given application the main point is the difference between the insertion loss and isolation, how we can improve this difference. Now let us say we plot a figure of merit versus frequency, so left side it shows insertion loss and right-hand side it shows isolation versus frequency for different figure of merits. Now for the insertion loss plot what we expect that instead of single switch if we use series-shunt configuration, insertion loss will be higher, so let us compare 200 femtoseconds for this one at 140 gigahertz insertion loss is almost 6 dB. Now if I compare this one with previous case, let us go back to previous one, so here with r ON equal to 4 Ohms you can see insertion loss at 140 gigahertz it is 3.5 dB approximately, so in series-shunt configuration insertion loss increases, now look at the isolation values.

For 200 femtoseconds at 140 gigahertz we have at least 15 dB isolation, but if I go back in the previous case in this case for 200 femtoseconds, you see isolation is less than 5 dB at 140 gigahertz. So using series-shunt configuration this isolation has been improved from 5 dB at least 15 dB and the same logic is true for other figure of merit values. So what is the conclusion then, we can use series-shunt configuration to improve isolation at the cost of little increased insertion loss.

Now, some cases we may face problem due to input impedance matching problem, why? If I go back to this circuit, once switch we are using in series configuration, another one in shunt configuration, so as a whole this switch is ON so now whatever impedance seen by the

antenna if I change the state of the switch, then it will be OFF that means this resistor is open and this series resistance we have to replace by a capacitor and this shunt capacitor we have to replace by a resister in that case input impedance seen by the antenna transmitting side everything will change. And not only that, in series or shunt whatever we consider, so the capacitance or resistance whatever given by the switch, it depends on that particular device, we do not have any control over that.

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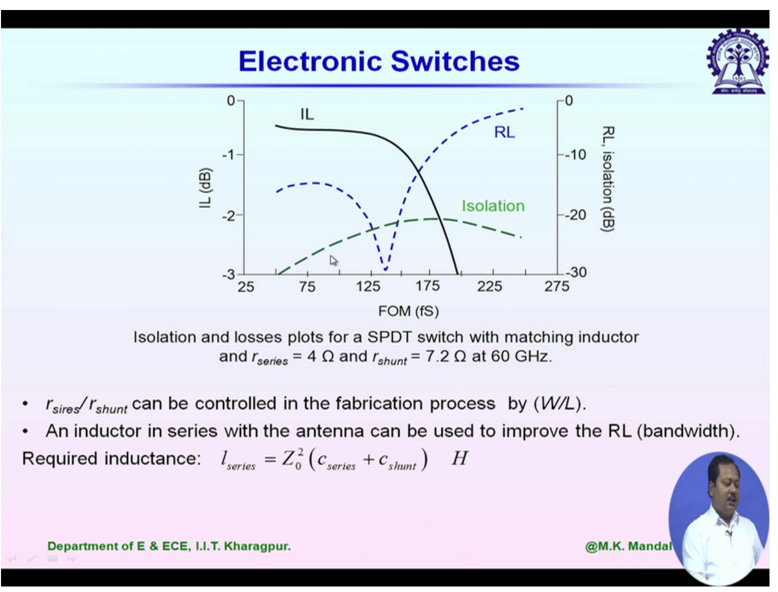

Now for a 50 ohms system we should match the input impedance, so sometimes it may happen if we simply by some switches and use in the circuit so input impedance matching it may be very poor, in that case how we can improve the impedance matching? We can use some inductor simply to improve the impedance matching, so let me show you one example. So in this particular isolation and loss plot for a SPDT switch with matching inductor, so when we add matching inductor we add a small value of inductor in series with the switch and the value of inductance L series it can be given as Z 0 square multiplied by c series + c shunt, so c series corresponds to the capacitance of the switch in OFF condition whatever we are using in series combination here.

Similarly, C shunt this is the capacitor of that PIN diode, which we are using in shunt configuration. So then the matching inductance value it depends on this capacitance values and the system impedance Z 0. Now if I look at the source of losses when the switch is ON so we have mainly losses because of the resistance, so resistance it is defined by fabrication process and for resistance improvement it can be done by changing the W by L where W represents the width of any MOSFET and L represents the length, same true for PIN diode, W

in that case represents the cross-section, L represents the length, so by fabrication process then we can tune the resistance value. Now look at this plot, so insertion loss it increases but return loss, it has a minimum value and it is a function of figure of merit.

So for a given inductor then and for a given capacitance value, we have some optimum value of r for which return loss will be minimum. So for this particular example when we are using r series equal to 4 Ohms, r shunt equal to 7.2 Ohms at 60 gigahertz, in that case we are having minimum return loss approximately at 130 to 140 Femtoseconds. Already we have discussed how to implement a switch by using PIN diode, now let us see how we can implement switch by using FET.

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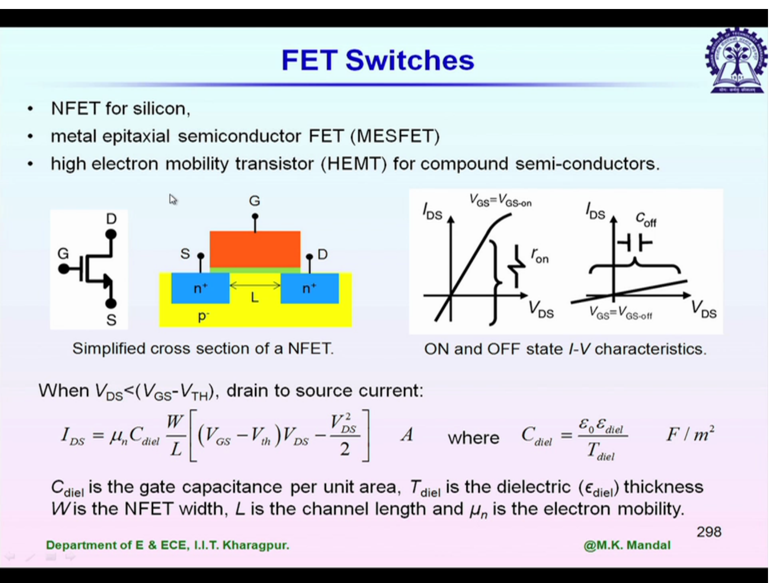

Now, in NFET or NMOS or PMOS, both are available in market but usually when we go for high frequency applications, NFET or NMOS is preferred, why? Simply because electron mobility is higher than hole mobility. So we can use NFET at even millimetre wave frequencies and there are some alternatives also, already we know the devices for example, we can use also MESFET as a switch, we can also use HEMT as a switch, but in all the cases we will prefer electrons as the careers. So in general, we can represent a FET MOSFET by this, so we have this is a 3 terminal device, if we neglect the body terminal then we have source, drain and gate, the control voltages is applied at the gate terminal. Now if I look at the variation of drain current versus V DS, so this first part of this graph, it looks like a straight line, we call it the linear region or the triode region.

And after that for a given gate to source voltage if we keep on increasing the gate to source voltage, then this current component it becomes constant or we call this is the saturation mode of the FET. Now, when we use it in the switching application, in that case we will be using this linear region and the cut-off region of the FET. So linear region it occurs for V DS, this is less than V GS - V TH, where V TH this is the threshold voltage and V GS this is the gate to source voltage, then in that case drain to source current, this is Mu n into C dielectric into W by L this ratio multiplied by V GS - V TH into V DS - V DS square by 2 ampere, where the C dielectric it represents the gate capacitance, it depends on the whatever insulation we have used for the gate and the thickness of that insulation.

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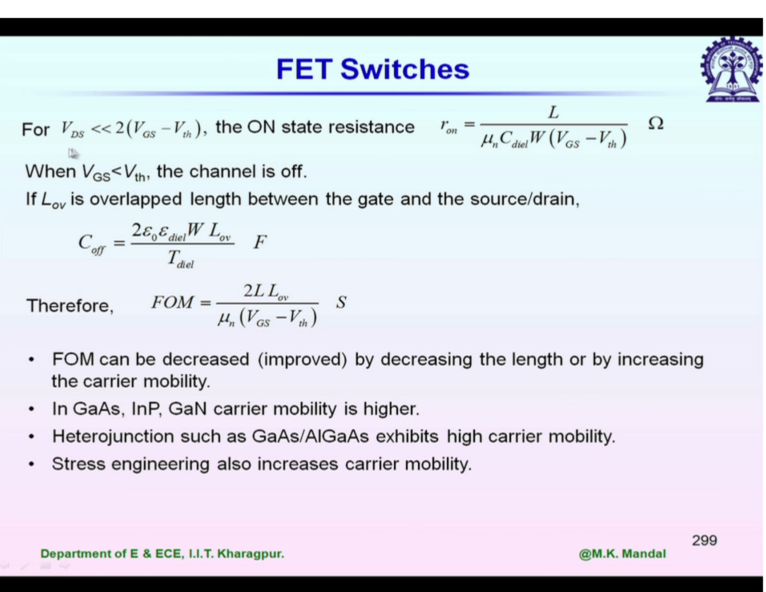

So C dielectric, it becomes a process parameter not only that W by L it is also a process parameter, which depends on the fabrication procedure and here L is the channel length and W is the width of the gate. So the ON state resistance we can consider a V DS value sufficiently smaller, then in that case r ON that is equal to L by MU n C dielectric into W into V GS - V TH Ohms and the channel is OFF, the switch is OFF when V GS is less than V TH, we do not have any inversion layer inside FET. So if L OV is overlapped length between the gate and the source drain, so OFF state capacitance we can represent like twice Epsilon dielectric into W L overlapped divided by T dielectric, it is in Farad. So for this given FET then we can calculate what is the figure of merit, it comes simply R into C, which is twice L L OV divided by Mu n into V GS - V TH and the unit is second.

Now for input figure of merit what we have to do, we have to decrease the channel length. Similarly, we have to decrease the V TH so W by L it is a process parameter, in that case we

have to use the minimum value so that you can have the less figure of merit value for improved performance of the switch. How we can decrease V TH, we can increase the dielectric constant of the insulator, whatever we use and the thickness of the insulator that should be as small as possible. Another way, we can use some group 3 group 5 material inside which carrier mobility is very high for example, gallium arsenide, indium phosphide or gallium nitride, so if the carrier mobility is higher in that case we can expect that r ON will be much smaller. Some hetero junction structure like gallium arsenide, aluminium gallium arsenide, they also exhibit high carrier mobility.

Stress engineering also increases carrier mobility, so this stress engineering last day I was discussing that another crystal let us say germanium or maybe silicon, so one crystal it is just… So if we place this crystal on another one and if we use a very thin layer, in that case, the first crystal it will try to follow the second crystal and sometimes the effective carrier mobility it depends on the crystal structure, so we can force the second layer to follow the first layer's property so this is called the stress engineering.

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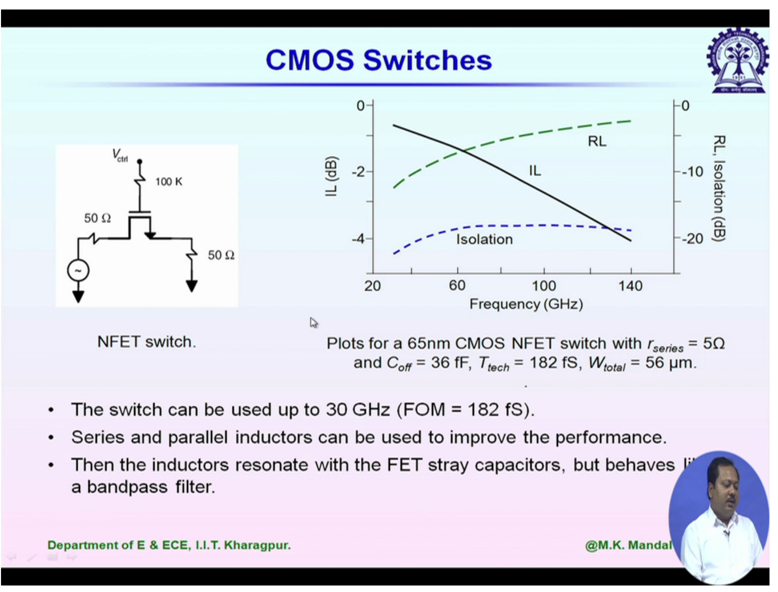

Now in CMOS technology, usually the figure of merit is very high and that is why it is not popular at millimetre wave frequency, typically they are used below 30 gigahertz, so here is one example of I l R l and isolation plot for a CMOS NFET designed using 65 nanometres technology, typical R series value is given as 5 ohms, C off 36 Femtofarads and T (())(16:22) figure of merit is coming 182 Femtoseconds. Sometimes, we can use parallel inductors to improve the performance of the switch, so this FET itself it will give you some capacitor and

inductors together it forms a resonating circuit and it behaves like a band pass filter. So that is how sometimes we can improve the performance of a FET switch.

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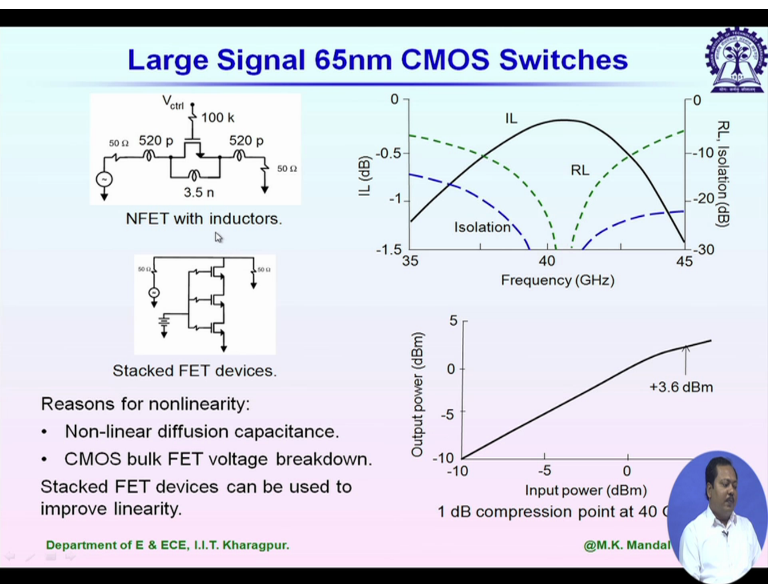

So here is one example of NFET switch with inductors, so for this typical switch we are using 520 Pico Henry in series and 3.5 Nano Henry in parallel combination and that will give a band pass filter like response, the response is shown here. So you can see insertion loss it is minimum at the resonating frequency, approximately 41 gigahertz. Not only that due to that resonant behaviour at this frequency return loss is maximum, so we have very less reflection from the input of the switch and also isolation is maximum. Now, one problem with FET or CMOS switch is that whenever we are using them, we are considering only small signal equivalent circuit and switching between the cut-off state and linear region.

But let us say, one FET switch already it is an cut-off region we are expecting that switch will be in OFF condition, but the applied electromagnetic signal magnitude is so high sometimes it can turn on the FET so we cannot use it for very high power applications, so this is the limitation for FET switches. So there is an alternative that we can use stacked FET configuration, so here is one example stack FET device. So instead of one we are using 3 FETs in parallel shunt configuration, so whatever voltage we are applying it is now being divided into 3 components, so that is how we can improve linearity of the given FET switch, but only one problem is that conventional CMOS fabrication procedure they cannot fabricate this type of stacked FET so we have to use some non-standard procedure and fabrication cost will increase.

Another important point, when we go for high power applications so what is the 1dB compression point of the switch? So you remember that we are assuming the switch as a linear device, so here how we obtain 1dB compression point this is first we have to plot the output power versus input power, it should follow a straight line if it is a linear device, but for high-power it starts to deviate from the straight line and when this deviation is 1dB, the corresponding input power we call the 1dB compression point of the switch. Here, this is the plot for a typical FET switch and we see for this particular switch 1dB compression point is that 40 gigahertz and it is coming for 3.6 dBm of input power.

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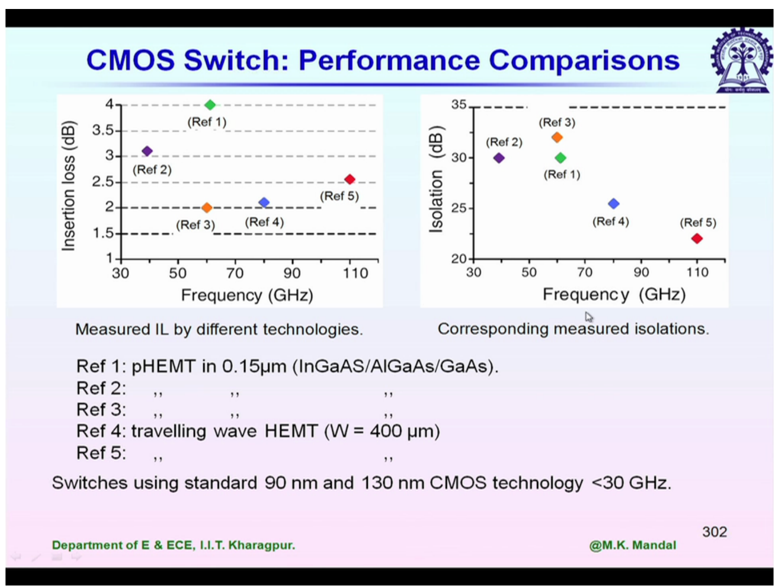

So here is performance comparison, we have different types of FET switches in HEMT technology, in travelling wave HEMT technology, so what is travelling wave HEMT technology? Here, multiple HEMT switches they are used in Cascade connection by using separate by separate transmission line section, so we use some transmission line among the FET switches to connect them and that is why we call it travelling wave type HEMT. So if we compare these switches performances, we see the insertion loss is lower for reference 3 and the blue ne reference 4, so mainly the HEMT and PHEMT they are better performance compared to conventional FET switches. Look at the isolation values, again PHEMT switches they are providing let us say 30dB isolation over 60 to 70 gigahertz. Typically, switches using standard 90 nanometre or 130 nanometres CMOS technology, we use below 30 gigahertz because of their very high figure of merit values.

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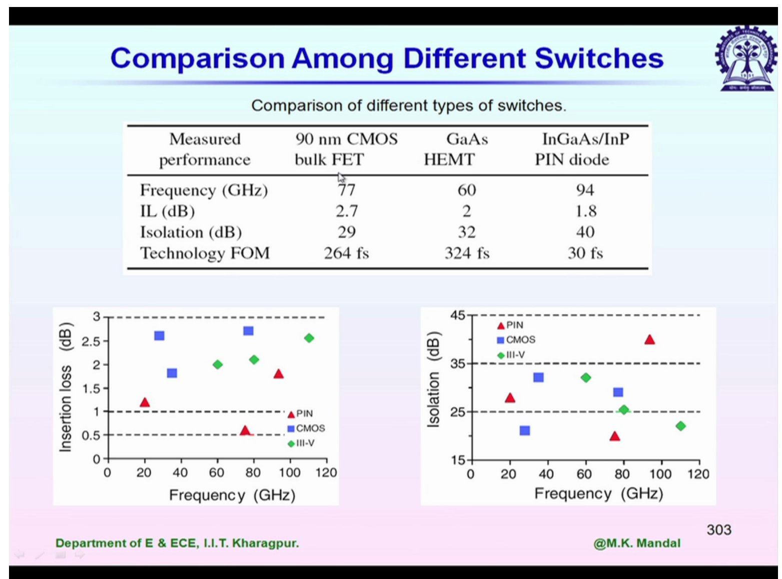

Now we know different technologies, we have FET switches, HEMT switches, PIN diode switches, so let us compare their performances. So these are the major performance comparison of some switches, which are available commercially in market. So measured values for FET switches typically at 77 gigahertz is providing insertion loss 2.7dB, isolation 29 dB and we see figure of merit is 264 femtoseconds. For gallium arsenide HEMT at 60 gigahertz we see figure of merit is 324 femtoseconds, but for PIN diode it is just 30 femtoseconds, so PIN diode among these 3 is a better performer. Here are some more examples, in all the almost all the cases, we see that PIN diode is providing lower insertion loss as well as better isolation.

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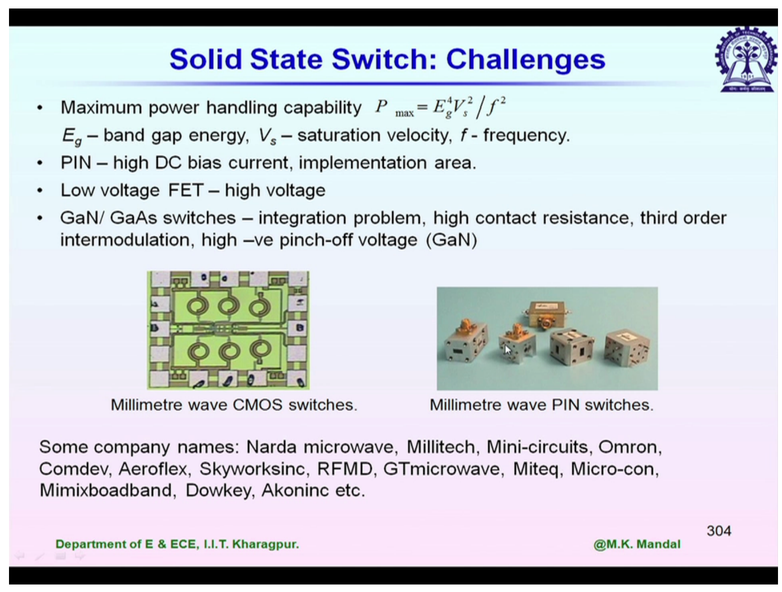

Now what are the challenges associated with electronic switches? So the first example is the maximum power handling compatibility, P max it can be given by E g to the power 4 into V s square by f square, where E g this is the band gap energy, so higher is the band gap energy maximum power handling capability is higher. V s is the saturation velocity, if the saturation velocity increases in that case also we can increase power handling capability and it decreases with increasing frequency, so different materials will provide different maximum power handling capability. Now if we use PIN diode, although in previous chart we have seen that PIN diode is providing minimum insertion loss and maximum isolation even at 100 gigahertz and beyond, but the main problem with PIN diode is the biasing current.

For PIN diode typical bias current it can be as high as 10 mili-ampere or even more than that. Now consider we are using a phase carry antenna or similar type of applications where we have hundreds of switches, so it will consume very high DC power so it is a problem for PIN diode. Next for FET, FET the problem is its low power handling capability, for high-power applications we cannot use FET switches, but the advantage of FET switch is its low power consumption compared to other switches. Similarly, gallium nitride or gallium arsenide switches although they provide better figure of merit compared to FET switches, but we face integration problem, high contact resistance, so finally we have to provide some contact switch by using some sort of metal, then third order intermodulation so it can generate high frequency components and high negatives pinch off voltage typically for gallium nitride-based switches.

So here are some examples of some fabricated switches, these are some photographs, left-hand side shows millimetre wave CMOS switches so this top layer this spiral they are actually inductors, we cannot replicate inductors inside chip, we have to fabricate inductors on top of the chip, so you can see this spiral they represents the inductor. So not only inductor, we need also capacitors so inductors and capacitors they use for RF and DC blocking. Right-hand side picture it shows several PIN diodes with their packages, so they are based in rectangular waveguide technology, inside the rectangular waveguide PIN diode is housed, you can see for a given component this small aperture it shows the input line, we have output line on the other side and the semiconductors, they are actually using for the biasing and for control signal. These are some name of the companies, different types of switches are available from these companies, so we will take a break then we will start millimetre wave propagation.