Millimeter Wave Technology.
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Lecture-18.
Antennas at MM-Wave Frequencies (Contd.)

So next topic we are going to start on chip antennas at millimetre wave frequencies typical chip dimension is a few square millimetre. And even at low frequency also but antenna dimension typically if I consider resonating antenna only at millimetre wave frequency its being comparable to chip size. So there is a possibilities of directly integrating 1 resonating antenna on chip.

And sometimes we can utilize the packaging also to integrate an antenna on the package itself. So what are the challenges we face at millimetre wave frequency? (())(1:03) to integrate and antenna on chip. Typically we use silicon or group 3 group 5 material like gallium arsenide substrate and this substrate they have very high dielectric constant more than 10 that we have seen.

So we will be facing problem of surface wave generation. If we don't take care and any remedies and then we may end up with no radiation at all from the antenna structure. So we have to solve this problem first. So at millimetre wave frequencies then let us first see. What are the typical applications bands are being used or targeted application?

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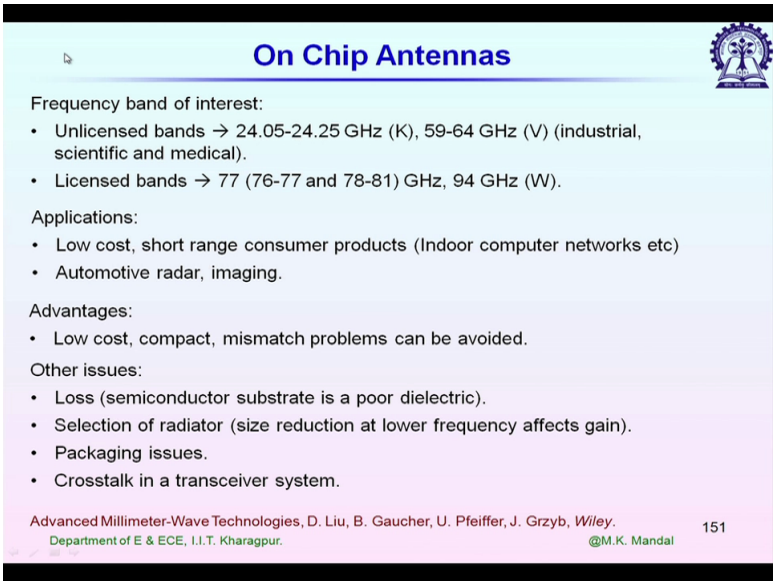

At 24 gigahertz we have one unlicensed band which is 1 ISM bands for industrial scientific and medical application. 24.05 to 24.25 gigahertz and again from 59 to 64 gigahertz at this band already we know that we have attenuation of millimetre wave signal due to oxygen resonance.

We have also some licensed bands at 77 gigahertz typically 76 to 77 gigahertz and 78 to 81 gigahertz there being used for automotive radar one more band at 94 gigahertz this is being used for imaging and sometimes communication so typical applications already in use and some of them targeted applications they are low cost short range consumer products like indoor computer networks we can also replace wireless LAN by millimetre wave link then automotive automotive radar applications imaging applications.

So what are the advantages of millimetre wave frequencies obviously the bandwidth and low cost, compact size and then the mismatch problem between different components it should be avoided. Some other issues already we know that semi conductor substrate its having some sigma part. So we cannot use semi conductor substrate as dielectric slab to realize the antenna structure not only that semi conductor substrate it has high epsilon R there will be surface wave generation which we cannot avoid.

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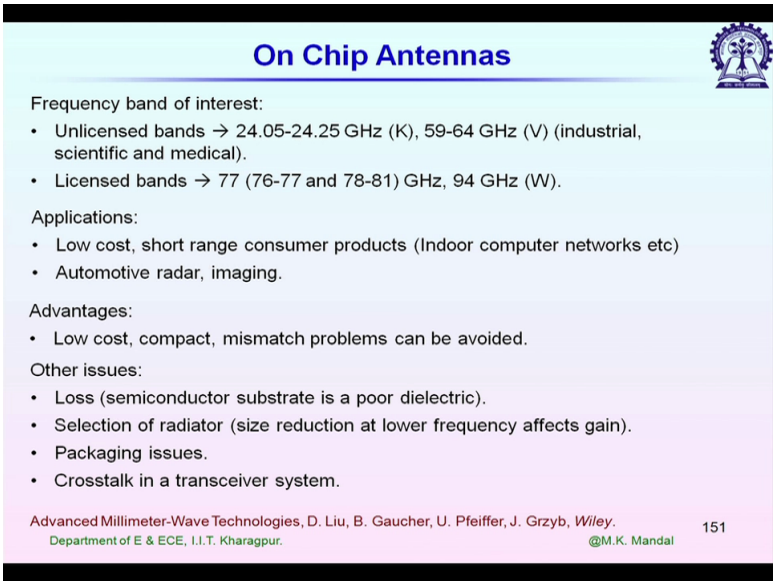

Some other problems selection of radiators we know different types of antenna structure like dipole antenna, look antenna, rectangular patch antenna then what type of radiator we should choose? We have to choose it very carefully for a given scenario and size of antenna it actually hmm influence the radiation characteristics.

Gain of the antenna it decreases with the effective area, physical dimension of the antenna and loss because loss increases with the reduced size of the antenna. Bandwidth that also decreases with reduced size of the antenna and antenna efficiency that again decreases with reduced size. So for all the an chip on chip antennas we will be facing this problems.

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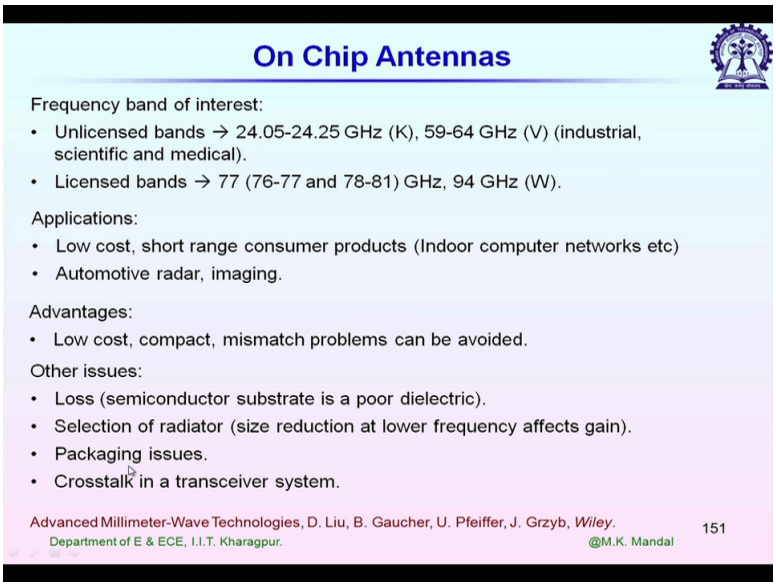

Some other problems packaging issues we use packaging for a protecting the chip from different weather condition then the packaging material it should be transparent to electromagnetic wave otherwise we won't be having any radiation through the packaging material. We have to be very careful about that when we are going to integrate an antenna and which should?

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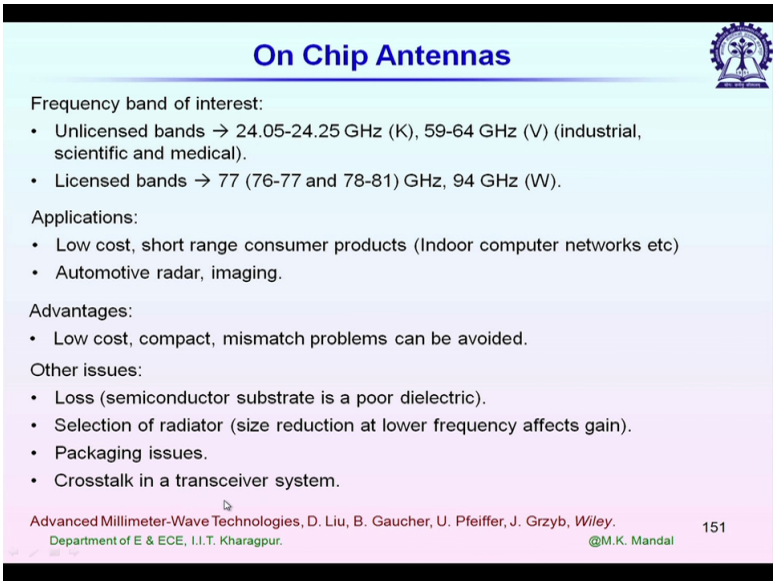

Then the crosstalk in a transceiver system let us say we have a transceiver chip where we have the both the transmitting part and the receiving part. Now transmitting energy is much higher compare to the receiving energy right. Even if there is slight leakage from the transmitter to receiver side it can damage the receiving component like it can saturate the LNA which is being used at the receiving part. So we have to be careful about that point also.

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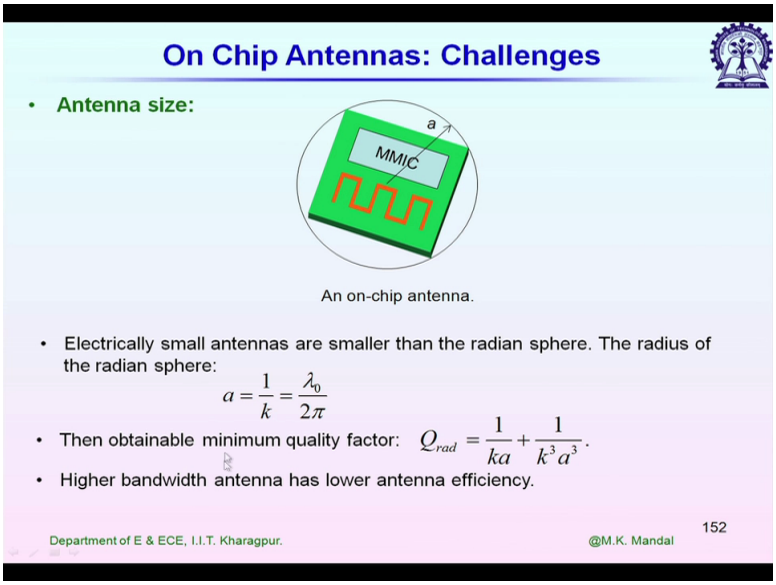

With this let us first define a few parameters then we will be seen the problems and what are the remedies? The first one is the antenna size at lower millimetre wave frequencies since the available area for antenna integration it will be always smaller than the wavelength. So we have to use electrically small antenna now how we define electrically small antenna? let us say the antenna it can fit inside one radian sphere .

Where the radian of the sphere is given by A it is defined as 1 by K in free space so that means K is 2 pie by lambda not and now if the antenna size is smaller than this A then we call it electrically small antenna. Then it can be shown there is a thumb rule obtainable minimum quality factor Q rad this is equal to 1 by KA plus 1 y K cube A cube. So if we decrease A or the antenna dimension then we will be having lower antenna efficiency. And higher loss and that loss its a wastage of power. Its not coming out as radiation from the antenna right.

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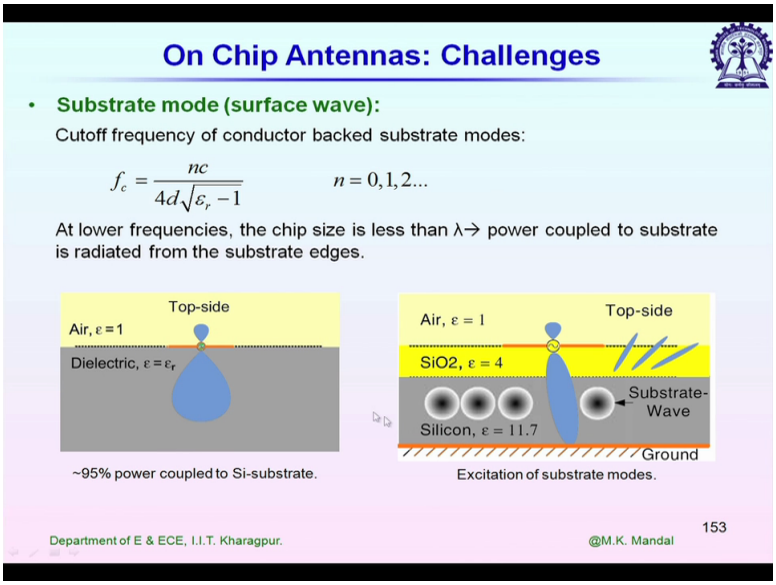

Now if I look at this left hand side structure let us say we are directly printing 1 dipole antenna on a silicon substrate. For silicon epsilon R is very high approximately 11.7 and outside we have air now the problem is that since epsilon R of silicon is very high almost all of the power radiated by dipole it will be trapped inside the silicon substrate. And outside we will not have any significannot radiation.

So that is why we cannot directly place 1 radiator above a silicon substrate or gallium arsenide substrate of other popular substrate. 1 procedure it can be we can we can use some sort of dielectric layer. In silicon we can easily generate silicon oxide which has very good dielectric property and now in the second example you see we are placing the dipole antenna above this silicon oxide layer for silicon oxide epsilon is approximately 4 but sigma part is approximately 0.

In this case again we have similar problem and we have the substrate wave generation or surface wave generation now what is the optimum thickness of silicon oxide so it should be as thick as possible to avoid power coupling to substrate but the maximum thickness that can be fabricated by using any process depends on the fab process fabrication procedure.

We cannot fabricate any any given value so it is limited by the fab process and typical silicon oxide that can be fabricated just taking nano meter its very thin and we cannot use that silicon oxide as the dielectric slab or the antenna structure. So it can be a solution though main problem then what we are facing here for both ground back structure and without ground structure is the surface wave generation or substrate mode.

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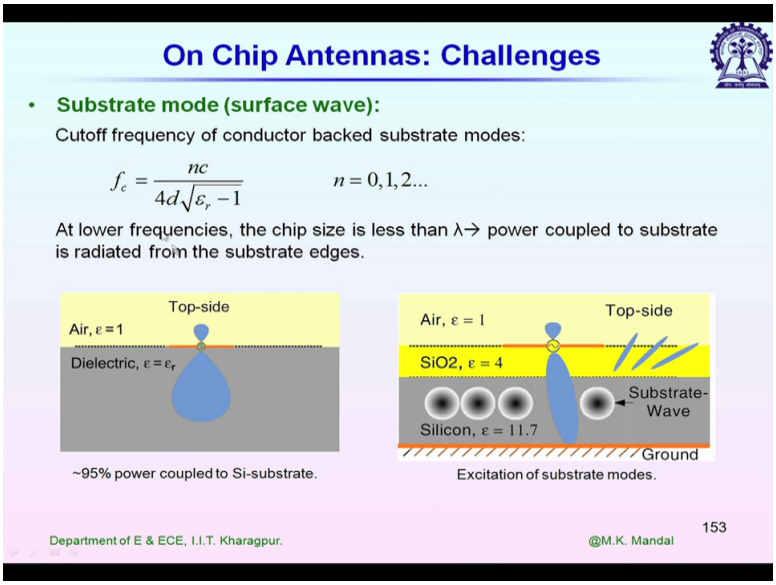

And already we know the cut off frequency for let us say conductor backed substrate it is FC equal to NC by 4d into square root of epsilon R minus 1 where D is the thickness of the substrate and epsilon R this is the dielectric constant. And for TM 0 and TE 0 mode you recall that we don't have any cut off frequency they can start right from DC.

So at lower frequencies when the chip size is less than lambda in that case power coupled to substrate is radiated from the substrate edge always we are having a finite size and what will be the problem. We will facing due to this (())(10:49) we don't have any control over this radiation from the surface wave from the edges. It will increase the cross pole level and the side lobe levels. And the gain overall gain of the antenna it will decrease.

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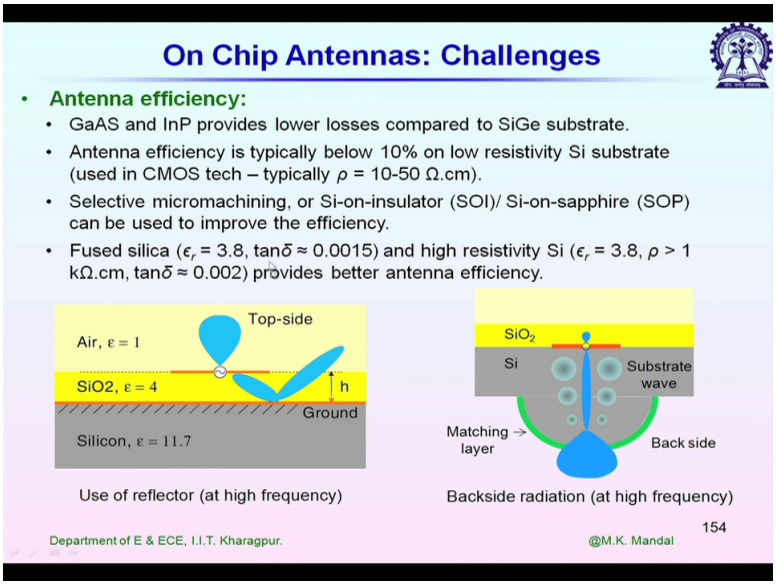

Let us consider some typical values antenna efficiency. How it depends? For gallium arsenide and indium phosphite substrate it provides lower loss lower sigma value compare to silicon germanium. And now for silicon germanium the sigma it again varies process to process. If we use CMOS or BICMOS process typical resistivity value is very small it is of the order of 10 to 50 ohm centimetre.

So we cannot use them as the substrate or dielectric slab. If we want to use silicon as substrate then we have to go for high resistivity silicon and that is expensive because it will we have to follow some sort of non standard fabrication procedure so typical resistivity needed a few kilo ohm centimetre. It high resistivity silicon that means doping concentration it should be as minimum as possible or you can say its almost like intrinsic semiconductor.

Now for gallium arsenide and indium phosphite we don't have any prob such problem like that. Different fabrication procedure they are completely different actually in terms of the metallisation where we place the metal layers. Sometimes we can use any metal layer if it is present just below the substrate so for group 3 group 5 materials (())(12:48) the fabrication procedure it starts with metallisation.

So we can utilize that metallisation at backed of the substrate as the ground plane but for silicon germanium we don't have such metallisation its start with bulk semi conductor. So we don't we cannot fabricate micro strip line structure we don't have any ground plane. So we have to integrate it from outside then. These points we have to keep in mind when we are selecting radiator or feeding structure.

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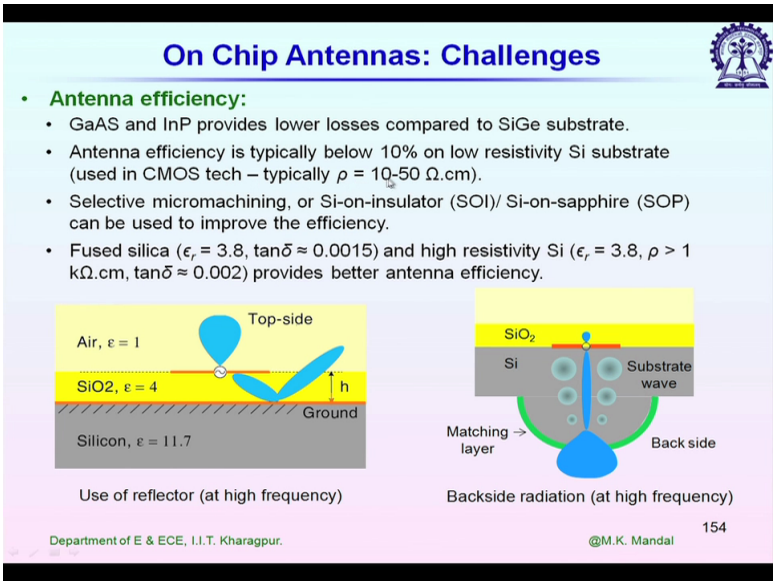

Now typically antenna efficiency is below 10 percent on a low resistivity silicon substrate because sigma is high so what can be the solution? We can use selective micro machining or silicon on insulator SOI or silicon on sapphire SOP technique we use some of them I am going to discuss next. We can also use fused silica for which epsilon r is 3.8 and tan delta point 0015 so it has very good dielectric property and we can use it as the dielectric slab.

And high resistivity silicon that already I discuss so typical values being used is rho more than 1 kilo ohm centimetre tan delta is point 002 so when we use this fused silica or high resistivity silicon it can provide better efficiency. Here are some examples how we can utilize the structure itself to improve efficiency of an antenna.

Then the first example we can see the dipole it is placed on that silicon oxide layer now we are intentionally fabricating 1 metal layer just on the silicon which we can use as the ground plane here in this particular example this ground plane is being used as a reflector. So if the thickness H in terms of lambda g it is quarter wavelength then the wave coming in this direction will be same phase that is how we can improve the gain of the antenna.

So whatever power coupled to silicon oxide layer it can re radiate in the same direction and that is how we can improve the efficiency of this antenna but fabrication process should support that silicon oxide fabrication. We need a thick layer of silica oxide. In the second example now the antenna is fabricated on a high resistivity silicon itself and you see the back side it is it is curved in form of a lense.

And the back side radiation what power being coupled to silicon substrate it is coming out from the length and on top of this lense structure we have a matching layer which we can use as packaging also and it is a transparent to radiation.

So that is another way to improve the efficiency of an on chip antenna but this type of technique it the fab lab is should support this fabrication in most of the cases in most of the fab lab they won’t support this type of fabrication. Because we need some non standard procedure for this type of structure.

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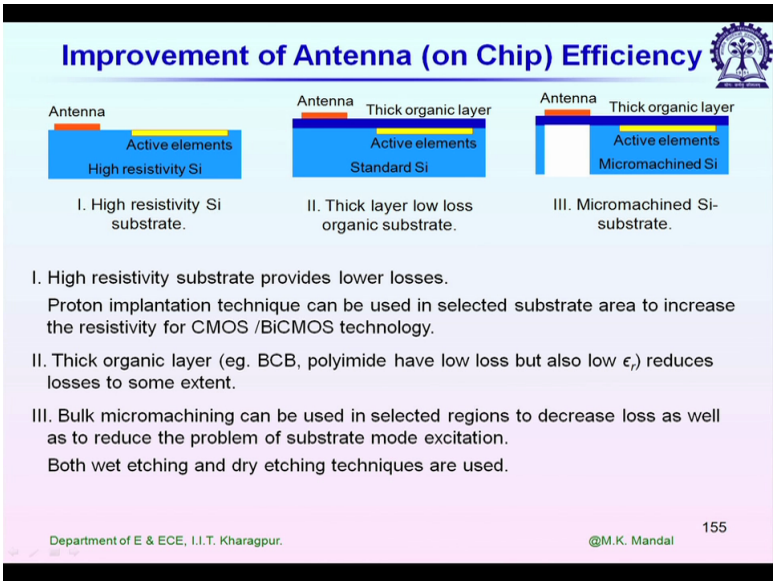

Then what are the typical procedure we use for the on chip antennas to improve their efficiency? Before that we need to what are the points we have to take care to improve efficiency. The first one we have to minimize surface wave mode generation for that how we can do it? Only way we have to reduce the thickness of the substrate and we have to decrease the epsilon R of the substrate so practically let us say how it can be obtained it can be achieved?

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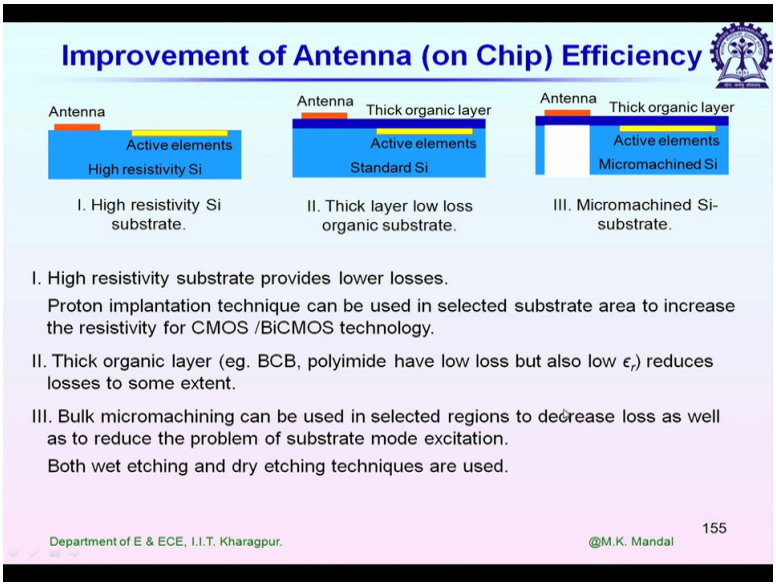

So in the first example what we are doing? The antenna structure itself it is being fabricated directly on a high resistivity silicon substrate obviously the radiation efficiency will be poor

but still we will be having some radiation since the loss inside the silicon substrate is much less is compared to the standard silicon.

And you can see 1 interesting point here that active elements are whatever the parts of the indicated circuit its far away from the antenna structure always the radiating antenna it is placed at 1 end of the chip. So that we can avoid coupling between the antenna structure and the other circuits of the integrate of the chip.

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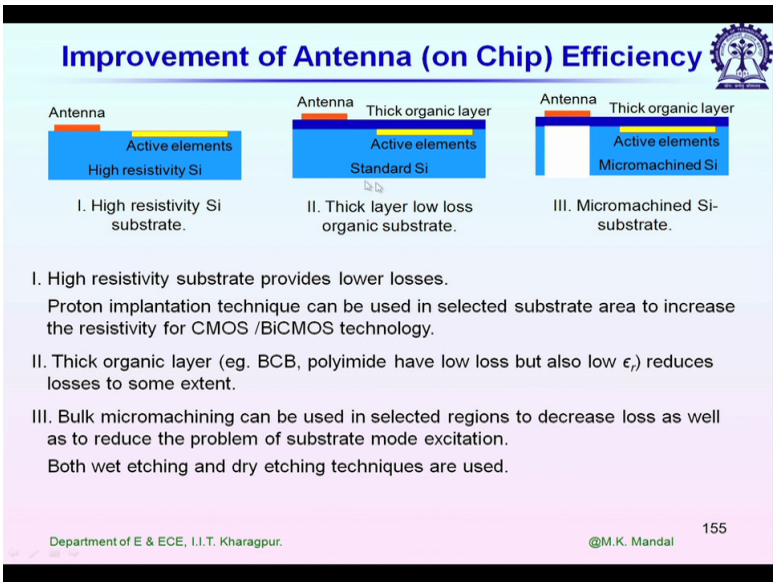

Now in second example antenna it is placed on a thick organic layer. So once chip is fabricated then we can put a thick organic layer on it. Typical material is DCB or polyamide they have low loss and also low epsilon R. So we can put it externally and then we can fabricate our antenna on top of this organic layer structure and this is the third technique most commonly used by using micro machining.

We have the same thick organic layer here and what we are doing by using micro machining we are removing simply the silicon structure just below antenna. So it looks like 1 ER cavity.ER cavity is placed below the radiator it can further improve the antenna efficiency. Because now we have epsilon R equal to 1below this radiator. So this is a very standard technique used at millimetre wave frequency to obtain higher gain and to improve the hence high higher efficiency of the antenna.

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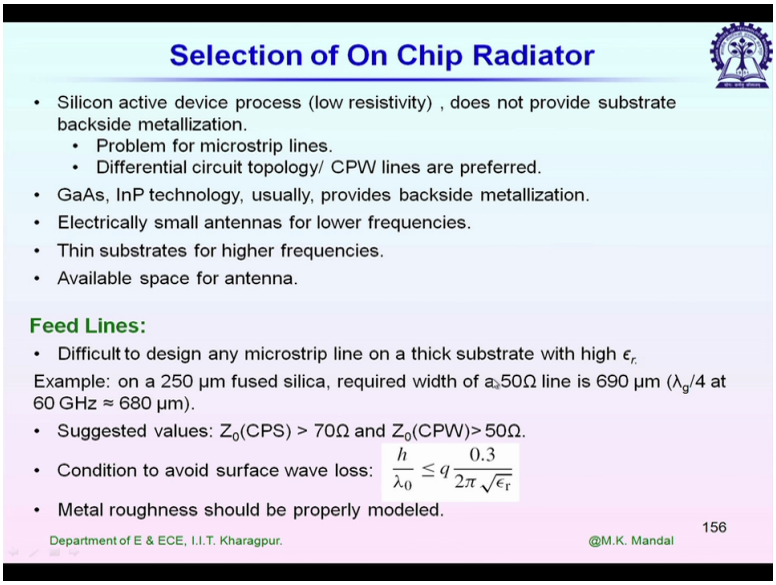

Now selection of on chip radiator as I discuss that different fabrication procedure they follow different steps gallium arsenide indium phosphite they start with backed side metallisation but for silicon germanium we don't have any backed side metallisation. So when we are going to choose the radiator type of radiator we have to be careful about it.

For example if I choose a micro strip patch antenna in that case we need one ground plane so it will be really difficult to fabricate it on standard silicon or germanium. But it will be easier on gallium arsenide substrate so for silicon germanium what we can do? We have to choose an antenna radiator where we don't need any ground plane for example dipole antenna or loop antenna.

Loop it can be wire loop it can be also slot loop. Next it comes feeding we may have CPW feed line we may have micro strip feed line but again we have some order issues. What are those?

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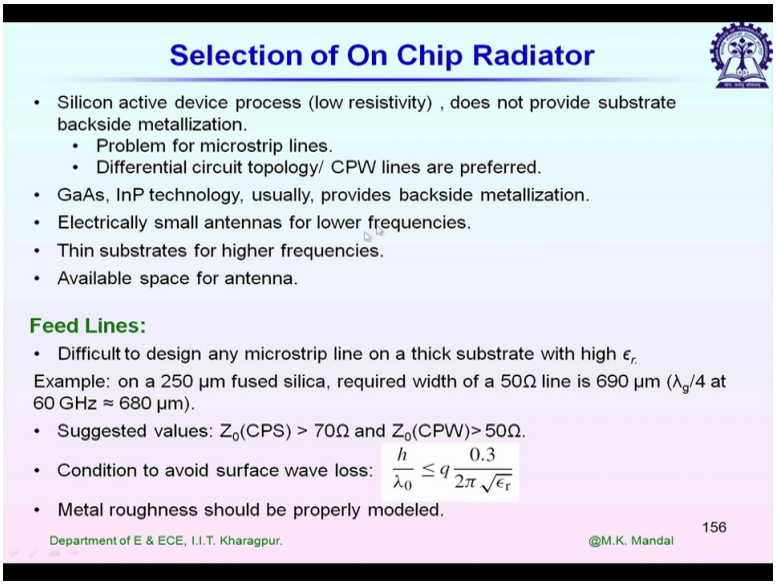

It is really difficult to design any micro strip line on a thick substrate with high epsilon R. The problem is that if the substrate is too thick then the width required for 50 ohm line its also wide and at high frequency 60 gigahertz and above lambda g al is already very small. Then we may have transverse resonance mode. So that is why we will what we will do? There will be using some other non standard values like let us say 70 ohm for 100 ohm for the micro strip line not 50 ohm. Let me give you some numerical example.

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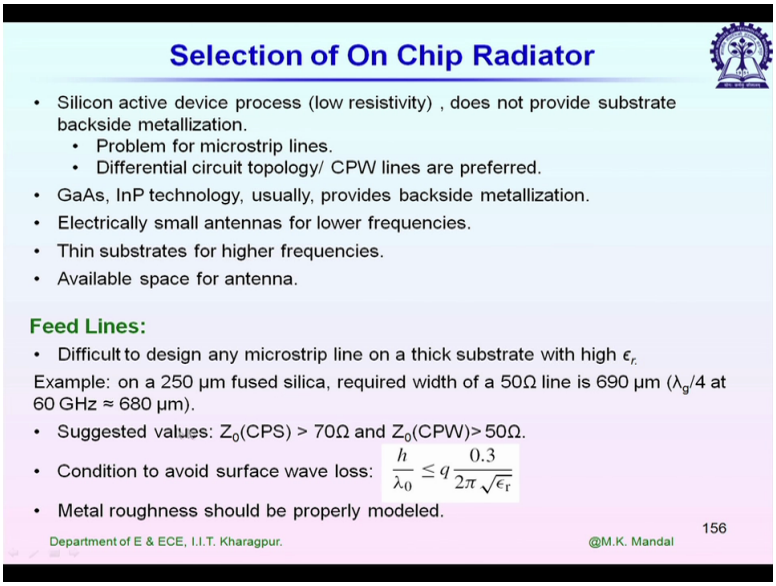

On a 250 micro metre fused silica requires width of a 50 ohm micro strip line is 690 micro metre where as lambda g by 4 at 60 gigahertz is 680 micro metre so we cannot use this. Then

the typical suggestive values for coplanar strip more than 70 ohm for CPW more than 50 ohm or for micro strip line also at least more than 50 ohm.

We have a thumb rule a condition to avoid surface wave loss H by lambda not where H represents the thickness of the substrate it should be less than Q into point 3 by twice pie root epsilon R. Now this Q its a parameter it depends on a type of line CPW CPS or micro strip line. Another important thing the metal roughness should be properly modelled.

So we already learnt that because of metal roughness or surface roughness we have increased conductor loss. Sometimes it can be as high as 200 percent compare to the smooth surface.

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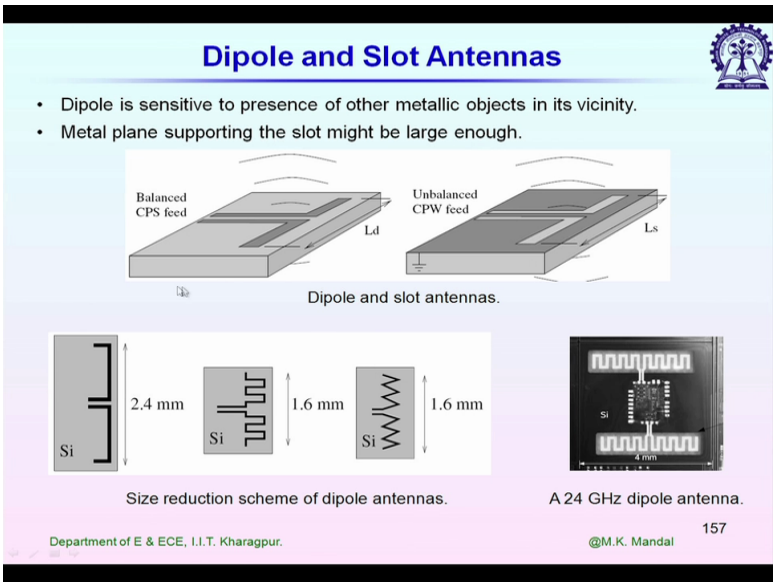

Now I am going to show you some examples of different antenna structures at millimetre wave frequencies. So the first example is dipole antenna its a balance antenna. so we for the feeding line we can we have to use some sort of balanced line 1 example is coplanar strip line its look like parallel wire but printed on the substrate. You can see directly then we can feed CPS to dipole antenna.

In this case if we have let us say CPW structure or micro strip line then we have to use 1 unbalanced to balanced transformation we call it balloon balanced to unbalance transformation. This is the second example this is a complementary dipole structure so this dark part is showing the metallisation where as the feeding line is CP CPW line slot and you can see the dipole it looks like a dipole.

But the arms are basically H slot in the ground plane of this antenna. it can also radiate it has complimentary properties. Here are some example of size reduction steps this is a 2.4 millimetre dipole antenna for 24 gigahertz application on silicon and now we can use some sort of meandering to reduce the size of the antenna. So that it can fit inside the chip right side you can see this is the fabricated example.

So from left to right total chip dimension is 4 millimetre its in silicon and you can see we have 2 antenna one is being used as the transmitting antenna and the second one is being used as the receiving antenna and the main chip part MMIC it sits in between and it is far away from the antenna structure otherwise there will be coupling between the chip structure itself and the antenna.

This is for a 24 gigahertz application and now when we reduce the antenna size obviously what will be expecting that antenna efficiency will decrease and antenna for this type typically the antenna efficiency is less than 10 percent.

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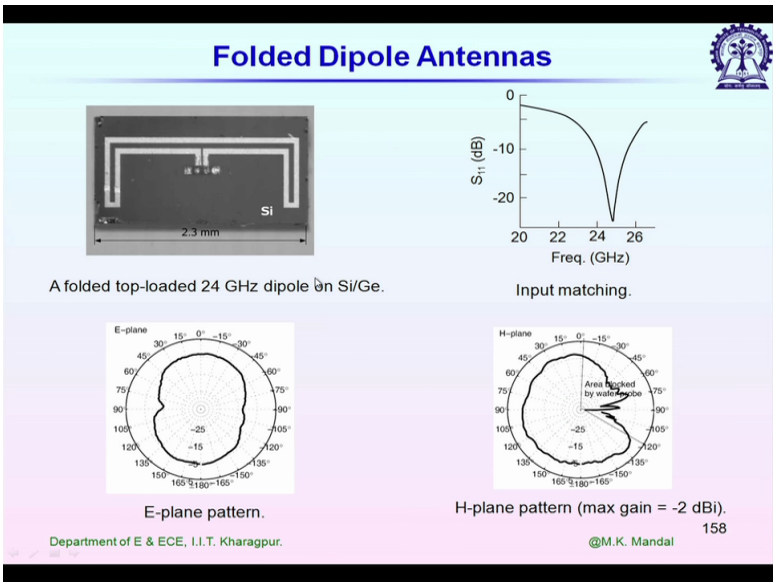

Another example folded dipole. So for dipole antenna typically antenna resistance at the resonance frequencies 73 ohm in some application we need higher input resistance radiation resistance. For that case we can use folded dipole antenna because folded dipole it has a higher antenna effi antenna input resistance compare to the dipole antenna almost 4 times of the dipole.

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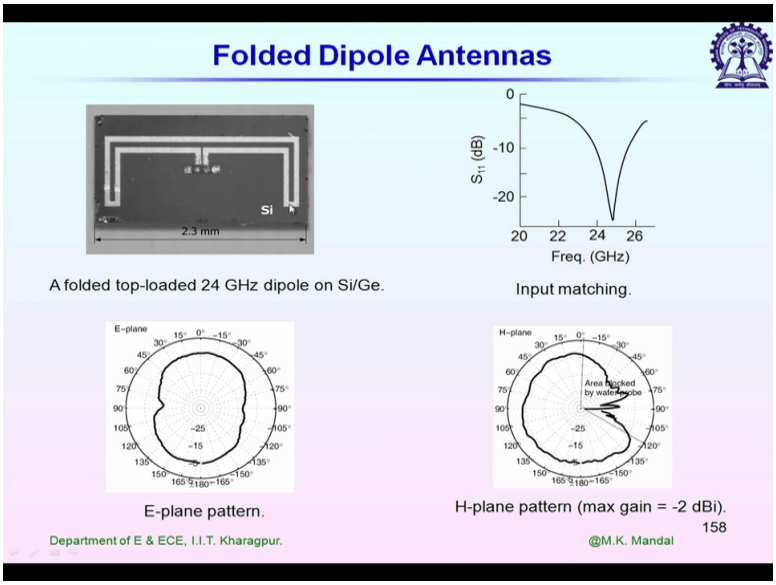

So this is 1 example of that folded dipole antenna fabricated on silicon technology on silicon substrate and you can see the measured characteristics for 24 gigahertz application. So its having good E plane radiation pattern and H plane radiation pattern typical gain obtain is minus 2 DBI for isotropic antenna if it is loss less ideal condition typical gain is 0 DB and for dipole antenna its 2.15 DB and for most of the antennas fabricated on chip it is below 0 DB.

This is due to loss from the antenna structure so gain is decreasing. Now if you look at the edge plane pattern plot here in this direction we don't have any radiation this is not the problem due to antenna. This is the problem due to measurement setter. It is being measured by a (())(26:34) station and (())(26:36) station are miss sitting this side so we cannot measure radiation pattern in this di direction.

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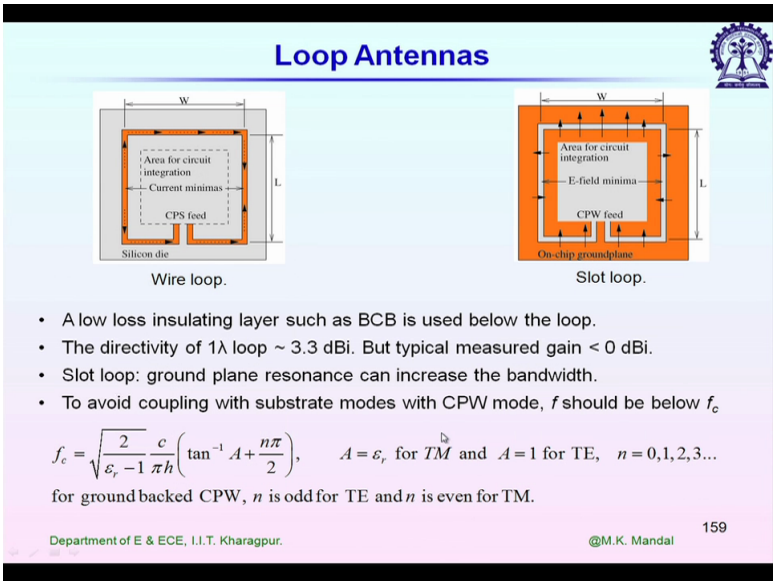

Next example is loop antenna. We can have wire loop and we may have also slot loop. Okay so let us take 1 break then we will continue with the on chip antennas.