Digital VLSI Testing
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Lecture - 07
DFT (contd.)

Next, we will discuss on scan architectures. Now, as I have said that, in a sequential circuit to test for the sake of testing it, we covert it into scan circuit.

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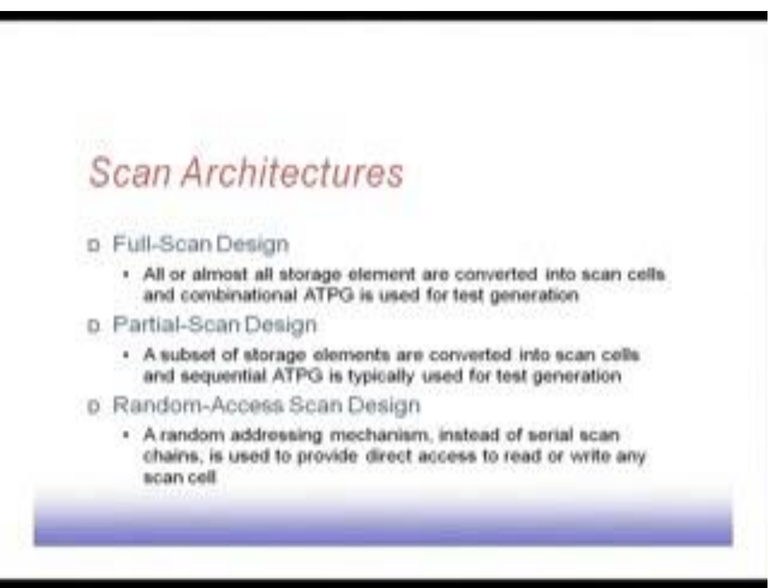

Now, there may be choice in the sense in that we may decide that all the flip flops will be converted to scan flip flops or another option may be that only a subset of the flip flops are converted into scan flip flop. And also in the access pattern by which we can access those indusial flip flops. So, in a full scan design almost or almost all storage elements are converted into scan cells and then combinational ATPG is used for test generation. So, here all the flip flops that are there in the design. So, they are converted to scan flip flops. So, now, for the test generation purpose since, we can control those flip flips externally. So, I can have a pure combinational test pattern generator to generate tests for the combinational part. And this flip flops can be tested before hand by applying some shifting pattern through this flip flop to this flip flop chain by may be for all 0, all 1, alternate 0 1, like that we can apply a few fresh patterns and get the confidence that the chain is working fine.

Other possibility is that only subsets of storage elements are converted to scan cell. And then all flip flops are not converted there may be logic behind this because as soon as we convert a flip flop into a scan flip flop. So, in most of the cases some multiplex are get introduced as a result the delay of the design may go up. So, there may be some flip flops which are critical. So, you cannot convert them into a scan flip flop. So, they continue to remain as normal flip flop. So, what happens as a result is that we get a partial scan design. In partial scan a subset of flip flops are converted into a scan.

So, naturally now we have to use a sequential ATPG. So, because now this circuit still remains a sequential circuit. So, a sequential test pattern generator has to be used for generating the test sequence. Now once we have converted the flip flops into scan flip flops, the connection pattern between them. So, they can define the access pattern. So, if all the flip flops are put on a chain in the way to access this flip flop is through a serial mechanism. So, it is a serial scan chain. So, on the other hand there may be these scan flip flops may be organized in a two dimensional way and then I can address this individual flip flops by my means its row address and column address giving a random access scan architecture.

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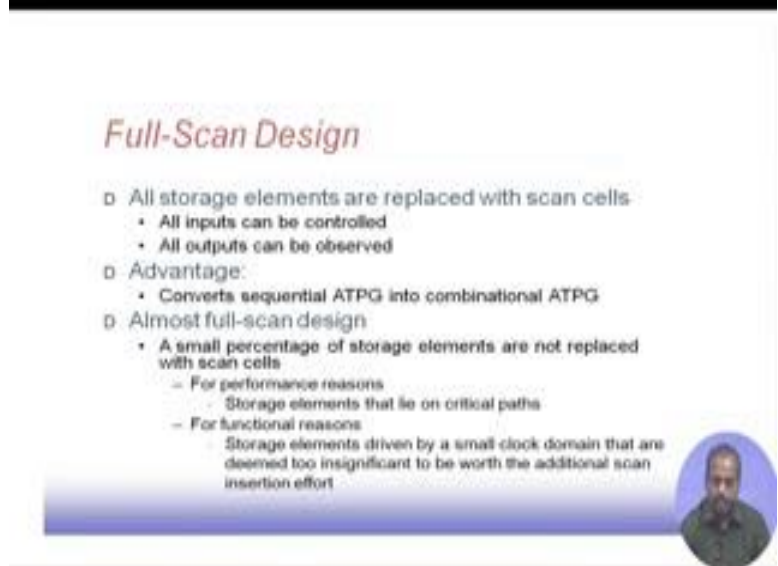

So, in the successive slide so will be looking into these architectures. In full scan design all storage elements are replaced with scan cells.

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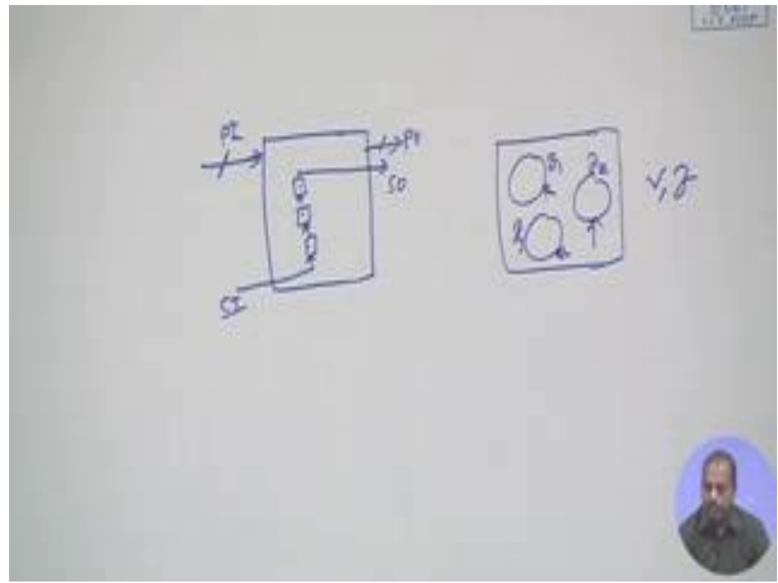

So, what happens in the design is that, if I have got in the design a number of primary inputs and then number of flip flops are there. So, what happens is that these flip flops are converted into a scan chain, they are converted into scan chain from the outside through the scanning line we can input the pattern into these flip flops and there is a scan out pin by which the content of this flip flops can be checked. And this is these are the primary output lines.

So, what happens is that for the testing purpose. So, I can consider these primary inputs as well as these flip flops as primary input. So, all of them can be configured can be viewed as a primary input. That is why all inputs can be controlled and at the same time all outputs can also be absorbed because they the primary outputs are absorbable and this scan cells are also absorbable through scan out point. So, advantage is it coverts sequential ATPG to combinational ATPG. So, this test pattern generation problem becomes simpler. So, it is no more a sequential ATPG.

Then, there is almost full scan design in which a small percentage of storage elements are not replaced with scan cells. So, this is for performance reasons because as I have already said that some of these storage elements may be on the critical path of the design. So, if we put them on the, if we modify to scan cell then the delay may be a problem. So, another issue maybe the flip flops location. So, if it is located haphazardly through a in the, it is far away from the, some flip flop is far away from other flip flops then, when

doing the scan stitching and making the scan cell then I have to have a long wire running from this cluster to that isolated flip flop to put it on to a chain so that also sometimes maybe undesirable. So, that is the reason.

And so also the clock distribution is another issue. Like storage elements driven by a small clock domain that are deemed too insignificant to be worth the additional scan insertion effort. So, if the clock domain is very small. So, what happens is that in any VLSI design if this is the full chip. So, it is divided into some regions. So, each region may be guided it may have its own supply voltage v and the frequency of operation f. So, say this region is running at frequency f 1, this is at f 2, this is at f 3. So, in some sense I can say that the clock for this region, clock for this region and clock for this region they are different.

Now, if you see that in f 2, there is only very insignificant portion of the circuit that is put there in f 2. Then it maybe better that we do not consider it for scan design. The reason being that, may be doing some very significant part of the job, for the testing purpose. So, you may omit that part. So, as a result there is no necessity to put in on to a scan chain that will unnecessarily link in the scan chain and created other problems.

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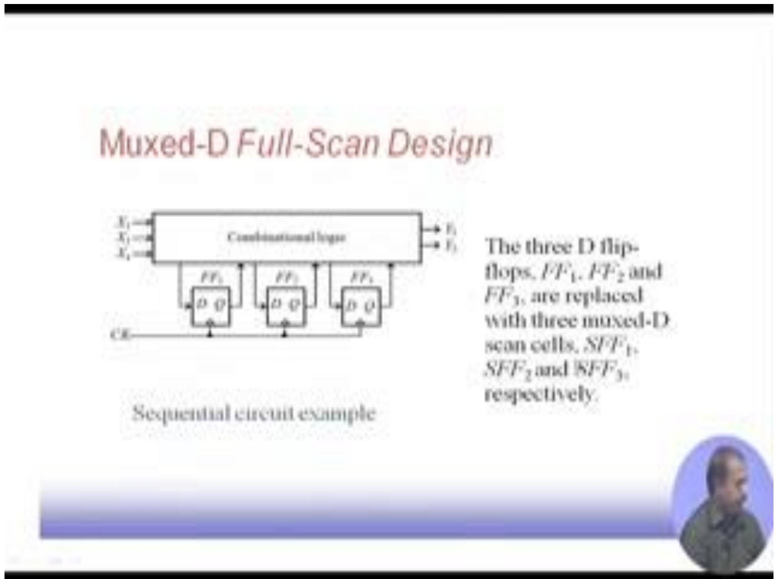

So, sequential circuits; so, suppose this is a sequential circuit. So, where we have got three flip flops FF 1, FF 2 and FF 3 and then we have got this combinational logic. Similarly, so these are X 1, X 2, X 3 are primary input Y 1, Y 2 are the primary output.

Now what happens is that in a Muxed full scan design these flip flops 1, 2 and 3 they will be replaced by three Muxed D scan flip flops; SFF 1, SFF 2 and SFF 3.

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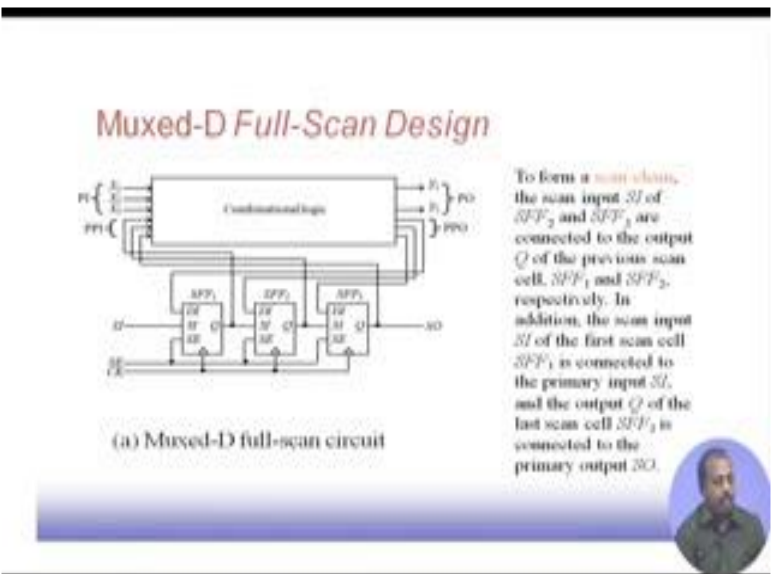

So, this is the representation. So, you see that. So, design of this scan flip flops we have seen before hand. Now as far as this combinational logic is concerned. So, it has got X 1, X 2, X 3 as input plus these flip flops are flip flops outputs are coming as input; that is a pseudo primary input. Similarly it is generating this primary output and pseudo primary output. Now since these scan flip flops are put on a chain. So, I can control these values that are coming into these individual flip flops and that way I can control the value that should go to PPI. So, whatever for testing this combinational logic for a particular fault, we need some specific bit pattern in X 1, X 2, X 3 and some bit pattern in PPI, PPI lines. So those can be done because through this scan chain I can shift appropriate pattern on to this flip flops as a result this combinational logic testing will can be facilitated. So, I do not need to bother about how to initialize this flip flops to the pattern needed at the PPI input.

Similarly, if this combinational logic test pattern that we apply. So, it reflects the faulty output at Y 1, then it is fine. So, we directly observe it. It may so happen that the faulty output comes in one of these PPOs. If it comes in one of the PPOs then, in the next cycle when they shift when this is captured on to this scan chain then, in the next shift, next few shift cycles. So, this content of this scan cell will be shifted out to SO. So, naturally

that PPO is also become observable. So, that way the ATPG for this combinational logic become simpler by introducing basic scan chain.

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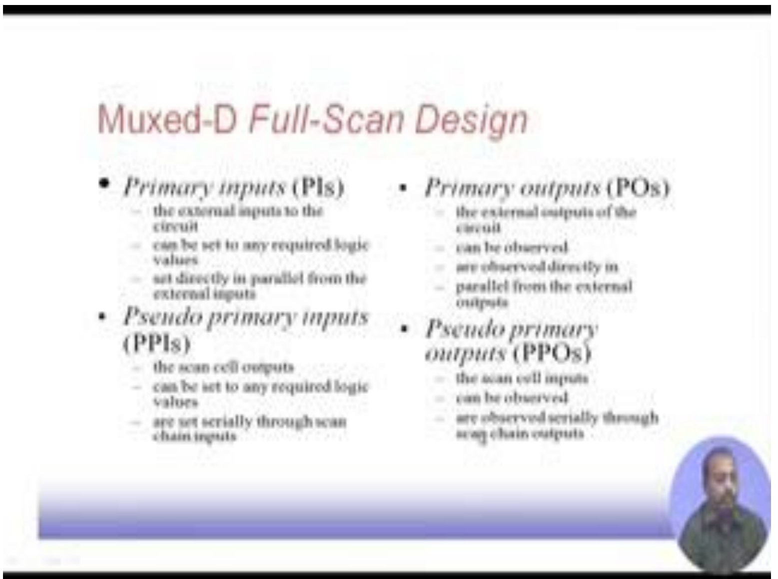

So, primary input. So, these are the external inputs to the circuit can be set to any required logic, that is because of primary input and say they are set directly in parallel from the external inputs. So, in this case these lines X 1, X 2, X 3, they are fed parallelly from the external world. Now, then there are pseudo primary inputs. So, these are these are the scan cell outputs and it can be set to any required logic values by doing this scan shifting and but this has to be done serially, unlike this parallel input, unlike this primary input X 1, X 2, X 3. So, this PPI setting has to be done via serial shifting.

So, that time is necessary. Similarly primary outputs so these are external outputs of the circuit. They can be observed very easily and they can observe directly in parallel from the external outputs. So, all these outputs are anything that is reflected on PO lines so they are seen directly. On the other hand, there are pseudo primary outputs. So, these are they are available at the scan cell inputs and they can be observed, but of course, observed through serial shifting of scan outputs.

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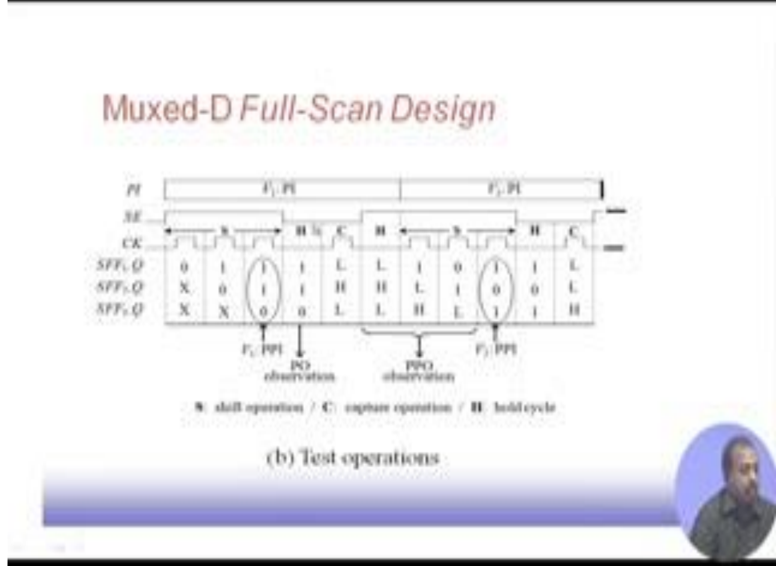

So, how do you apply this test pattern? Suppose I have got a test pattern where, this test pattern is divided into two portion; this test pattern V 1, it has got a primary input part and a pseudo primary input part. So, primary input part is it is some value. So, it is not specified here some three bit value maybe there and for the pseudo primary input suppose the desired setting is 1 1 0. So, what is done? First this shift enable is made high and the clock is applied. So, these are the three shift cycle. So, first we in the serial input we output a 0. So, that after the first clock cycle the flip flops 1, gets the bit 0. Then at the next cycle at the serial input we put 1 and this 0 of the first flip flop shifts to the second flip flop and in the third cycle this 0 comes to the flip flop 3, this 1 that we are introduced comes to flip flop 2 and in flip flop 1, this 1 is introduced. So, this actually now I have got this pseudo primary input bits having the proper values.

Then this shift enable is disabled, shift enabled line A C is disabled and there is a hold cycle that is given that is, that utility we will see later. For the time being we just ignore it, there is a hold cycle after that this clock another clock pulse is given. So, this is called capture because at this time this value is held at the input and this. So, this combinational logic it will evaluate this input, this V 1 the primary input part it can be set to proper values at anytime up to this part, up to this point, up to this shifting point at any time. So, for the sake of simplicity we can assume that there V 1 is set at the beginning of the shifting itself.

So, now after that so this capture cycle is one pulse, clock pulse is given in the capture cycle. In the hold cycle the circuit value with a combinational logic it evaluates this input pattern and sets the primary output and privacy to primary output to prepare values. Then in the capital cycle the pattern that we have. So, that is actually captured on to the flip flop. So, that is in the captured cycle from this combinational logic output the bits, the pattern they get captured on to this three scan flip flops in through their data input line.

Now, after that there is another hold cycle given. So, that we can see the primary pseudo primary output, the first bit of the pseudo primary output we can see that is this L. So, this is actually checked then, for the next pattern we start shifting. Say if next pattern is V 2 and V 2 for V 2, there is a primary input setting. So, that is not our concern say, for it the pseudo primary bit is bit should be 1 0 1. So, this 1 is shifted at the first clock cycle. So, as a result this L that will we had at flip flop 1. So, that get shifted to the second scan cell and this edge of the seconds scan cell comes to the third scan cell as a result we can view this second scan output. This SFF 2 output of previous corresponding to previous pattern is now observable.

Now, in the next another shift pulse, another clock pulse is given with shift enable remaining high. So, now, this 1 comes to the seconds scan cell and then new zero pattern that we have applied at the serial input. So, that comes into the first flip flop and this L goes to the third flip flop. So, we can see the third flip flop. So, after this clock we have got all the three bits of this pseudo primary output shifted out and we could see the values.

Now this pattern has got the loaded, this pseudo primary input part of V 2 has got loaded. So, again one hold cycle is given and then a capture pulse is given. In the hold cycle the combinational logic will evaluate the value and then in the capture cycle the values that are computed at pseudo primary output. So, they will get captured on to the flip flops and again in the next pattern V 3, the current response L L 8 will be shifted out through the scan out line and the next pseudo primary input part will get shifted into the flip flops. So, that way this testing operation will take place.

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Muxed-D *Full-Scan Design*

Circuit Operation type	Scan cell mode	*TM*	SE
Normal	Normal	0	0
Shift Operation	Shift	1	1
Capture Operation	Capture	1	0

Circuit operation type and scan cell mode

So, we can find out that, this circuit now operates in several mode like in circuit operation type normal and scan. So, if TM the test mode is 0 and this shift enable is also 0, so that is a normal operation, now that is a normal operation. So, the circuit operates in normal mode. Now if this test mode is 1 and the shift enable is also 1. So, that is called a shift operation. Now the pattern will be shifted to the scan chain. Now of course, the combinational logic, since it is a combinational logic it will do some evaluations, but those evaluations are not meaningful, we are not interested in those calculations. We will only be interested when this shifting is over and once the shifting is over. So, we give a hold cycle. In the hold cycle the value gets, the combinational logic it will evaluate the values.

And then comes the capital cycle, for the capital cycle. So, this test mode is made 1 and this shift enable is made 0, as a result the values that will be there in the pseudo primary output will get captured on to the flip flop, so that way this capture operation. So, we have got three modes of operation in this full scan design. One is normal mode, one is shift mode and another is capture mode. So, they are identified by these setting of these TM and test mode and shift enable lines.

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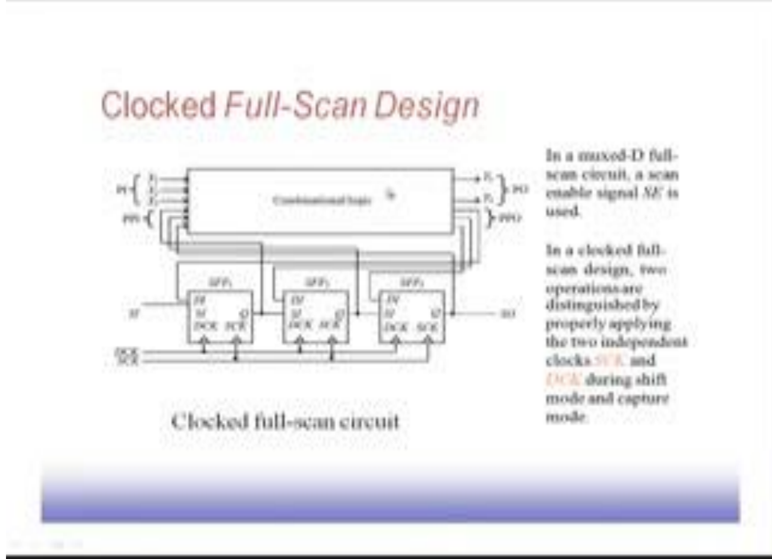

Then comes this clock scan, full scan design. So, when a clocked over full scan design. So, we have got two clocks; as we said that there is a data clock and there is a scan clock so, DCK and ACK. So, for the normal operation of the system this DCK lines will be, clocks will be given to DCK and SCK will remain permanently low and for the scan part or so. This SCK line will be giving pulse, they will be given pulse and this DCK part will be, DCK clock will be deactivate.

So, in a Muxed full scan designs, full scan circuit is scan enable signal SE is used. So, this is the. So, here we do not have any SE signal. So, that was there in the clock full scan design, in Muxed full scan design. In clock scan design we have got two clocks; DCK and SCK; two independent clocks for shift mode and capture mode of operation. So, operation is now very simple like whenever we want to do the shifting part, shifting part of the pattern. So, this SCK pulses will be given and the values will be given on to this SI. So, that the values are loaded onto this flip flops and then we give the DCK clock so that, this data that is there. So, combinational logic will evaluate this Q values and these PI values; that is the PPI values and PI values and accordingly the proper values will come in this Y 1, Y 2 and this PPO bits. And then when this DCK clock will be given.

So, this from this PPO lines, the values will be coming into this flip flops to this DI line; the data input lines. And then after again that shift clock will be given and when the shift

clock is given so these values will be a get shifted to the next place. So, when the SO output, so, we can see really see the output, while the shifting in a next pattern will be going on parallelly. So, otherwise it is same, but only thing is that instead of a separate scan enable line. So, we have got a separate clock line; SCK.

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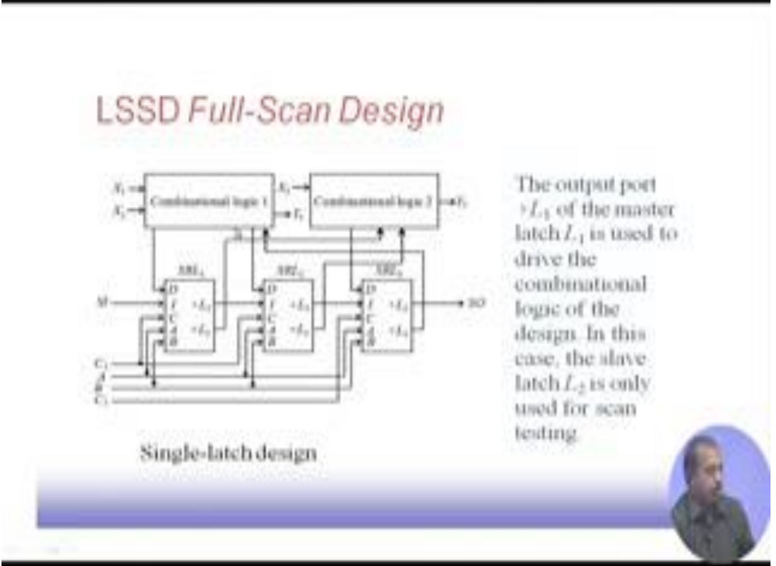

Next, we will look in to this LSSD full scan design. In LSSD design so we have got the output of, output port plus L 1 of the master latch L 1 is used to drive the combinational logic of the design. So, in this case so this L 1 plus is used for the driving the

combinational logic. So, in this case the slave latch L 2 is used only for scan testing. So, basically this, in case of LSSD design so we had two version. One is the latched version and another is that we have; one part is that this latch is driving the combinational logic and the second part is that for the shifting. So, we need double latch. So, that is actually done by this L 2.

So, this L 1, so this combinational logic produces some output, that is latched here and this latched output is going to combinational logic too as input. So, that is the basic circuit design that we have. Now to handle this scan shifting part so, this scanning line is coming and this L 2 plus line is driving the input of the next one, input of the next latch. So, similarly this L 2 plus, this drives the next latch. So, this way this is SI line and L 2 plus line. So, they will be construct the scan chain and this part, so this L 1 plus line. So, they are used for driving the circuit. So, these L 1 plus line drive this circuit and this L 1 plus line drive this circuit. So, this is from the design of the circuit. So, we do not have anything to design at this point because that was the way the circuit was designed. So, it had two part; logic one and logic two and these flip flops. So, these latches where there, where this L 1 plus and L 1 plus. So, they were driving the two different combinational logic portions.

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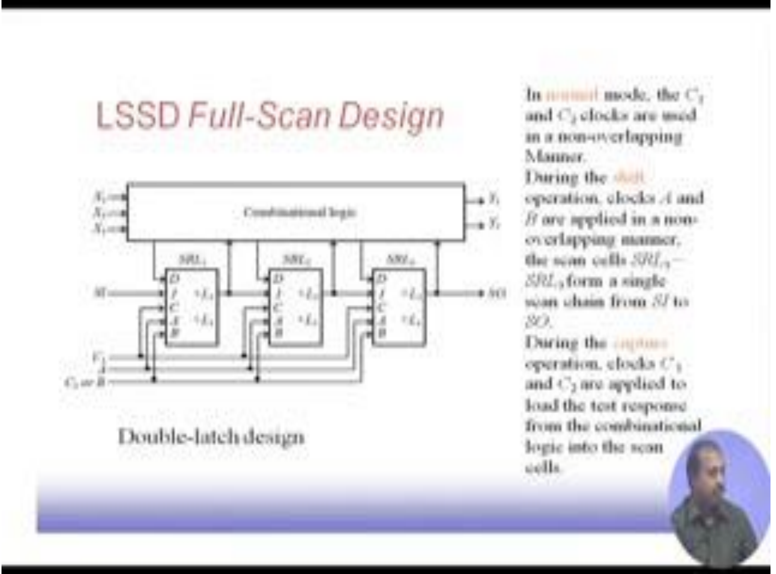

So, if we are having a double latch design. So, double latch design here the combinational logic that we have. So, there L 1 plus lines are not used, but L 2 plus lines

have been used in the original design. So, in this case we have got this L 2 plus line feeding this combinational logic and at the same time these L 2 plus logic also forming the scan chain. So, there is no problem because now this L 1 plus lines are not required. So, in the previous case L 1 plus lines were required for driving the combinational part, but here it is not required.

So, in normal mode of operation C 1 and C 2 clocks are used in a non overlapping fashion. So, C 1 and C 2 clocks are used in non overlapping fashion. So, that the data that is coming to the first latch is shifted to the second latch and then it is available at the, for operation in the combinational logic. So, during shift operation will be using clocks A and B in a non overlapping manner. The scan cell SRL 1 to SRL 3 they will form a single scan chain from SI to SO. So, for this C 1 and C 2, so, they are used in for normal operation in a non overlapping fashion and this A and B so, they are used in non overlapping fashion for scan shifting. And similarly during capture operation this C 1 and C 2, they will be applied to load the test response from the combinational logic. So, that way they are remaining same. So, double latch design so if your system requires a double latch design then, you have to do it like that. If the design itself is a single latch design then we have to use the previous mechanism. So, in both way we can have this latch based for latch based design so we can frame scan chains like this.

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There are several rules for this LSSD designs like all storage elements must be polarity hold latches. So, this is one requirement. So, you cannot keep any storage element has normal latch because then this scan chain cannot be framed. The latches are controlled by two or more non overlapping clocks; this C 1, C 2, A, B like that. A set of clock primary inputs must follow three conditions; any set of clocks you take that they must be they must follow this condition. The all clock inputs to SRL must be inactive when clock primary inputs are inactive. So, there should not be any other clock coming to the flip flop or coming to the latches. So, only the prime primary clocks that we have. So, they should drive these clock inputs of SRLs. The clock input to any SRL must be controlled from one or more clock primary inputs. So, there should again the thing is that every clock input of an SRL has to be controlled by some primary input.

And second thing is that no clock can be ANDed with another clock or its complement. So, if you AND then there is a problem because the operation becomes difficult to predict. Like when, this clock signal? How to enable it? How to disable it? So, that logic becomes complex. Many times what happens is for the designing purpose. So, we do we put some logic on the clock line. So, do some ANDing of clock signals. So, that when both the signals are active then only this will be active like that, but it should not be done here and ANDed particularly has to be avoided because ANDing means they are overlapping clocks. So, it will be active only when both the clocks are active. So, if you are taking, if you do an ANDing; that means, that line output is going to be an ANDed operation. So, that will be active only during overlapping clock. So, we do not want any action, we do not want the clocks to be overlapped because in that case the operation becomes unpredictable.

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LSSD Design Rules

- Clock primary inputs must not feed the data inputs to SRLs either directly or through combinational logic
- Each system latch must be part of an SRL, and each SRL must be part of a scan chain
- A scan state exists under certain conditions:
  - Each SRL or scan out *SO* is a function of only the preceding SRL or scan input *SI* in its scan chain during the scan operation
  - All clocks except the shift clocks are disabled at the SRL clock inputs

Then clock primary input mast not feed the data input to SRLs either directly or through combinational logic. So, this clock primary input it should not be connected to the DI input for the same reason that, in that case the data input will also change when, the clock input is changing. So, when clock input is changing if data input changes then of course, there may be a set of hold timing problem or if it is via through combinational logic ANDing will say some logic operation around clock and then applied to the combination then applied to the SRL data input then, also the same problem that during the clock is changed, during the when the clock is active the data input may flicker. So, as a result the operation may be problematic.

Each system latch must be part of an SRL and each SRL must be part of some scan change. So, it says that there should not be any latch left as it is. So, that is one part and also each SRL, each latch must be part of this, they must be put into some scan change. So, no latch remains uncontrolled. So, that is the whole thing no latch remains uncontrolled.

A scan state exists under certain con condition. Each SRL or scan out SO is a function of only the preceding SRL or scan input SI in its scan chain during the scan operation. So, this is the first condition that in any for any scan cell its content in the next clock cycle, it is dependent on the content of previous scan cell only. So, it is or from the scan primary input. So, it is only on those two parts the scan out will depend. So, it is not that it

depends on some other logic and all that. So, the scan chain is actually from one chain to another chain the connection is a straight connect, one fillip flop to another flip flop on a chain or sorry one latch to another latch on a chain. So, they are that is a straight way connection. So, there is no logic in between. So, it is not a function or something else and all clocks except the shift clock are disabled at the SRL clock inputs. So, this is also necessary because when we are shifting. So, all other clocks must be disabled only the shift clock should be applied.

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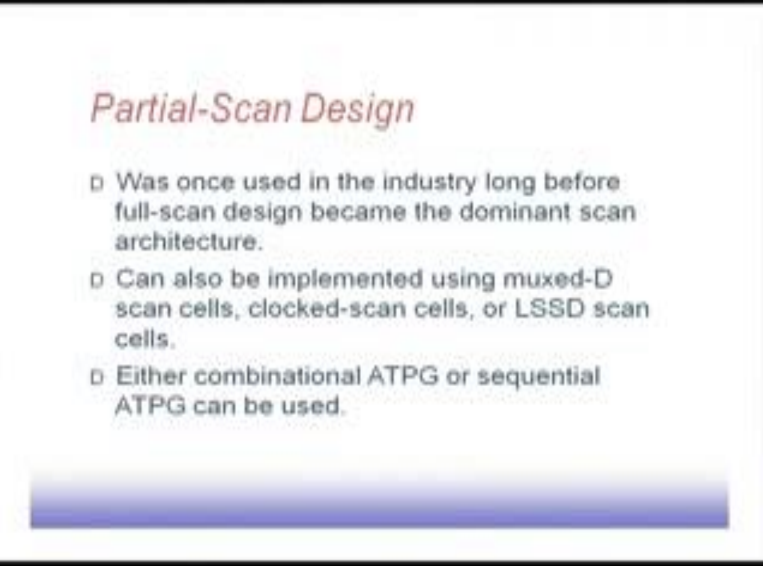

So, next the partial scan design; in partial scan design what we do is that we will be considering only a subset of latches or flip flops for putting on to into this scan chain. So, the problem with full scan design is that we cannot, it may not be possible to put all the flip flops or latches on to a chain. So, partial scan design will try to resolve this issue and try to come up with solution. So, that we have less complexity, we have many of that design all design criteria are made in terms of timing, in terms of power in terms of area and all that.

So, we continue in the next lecture.