Digital VLSI Testing
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Lecture - 06
DFT (Contd.)

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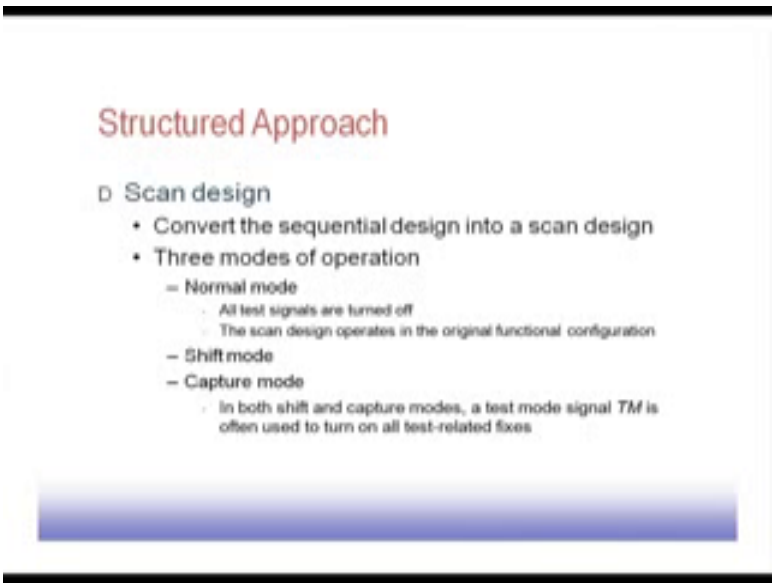

Next we will look into the structured approach for this DFT design. So, this they come under the broad heading of scan design. So, it says it converts the sequential design into a scan design and as we have notated earlier, in scan design what happens is that? This flip flops that we have in the design. So, all those flip flops are converted into scan flip flops and they are connected over a chain.

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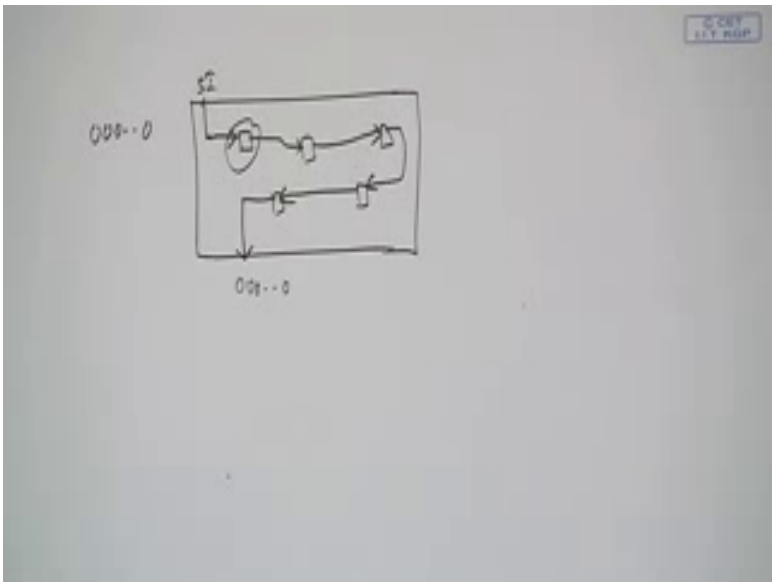

So, conceptually we can say that ok, if this is my full chip and in that chip we have got a number of flip flops distributed into this design.

So, testing such a system becomes difficult because this flip flops they are feeding some logic and for testing those the parts of the logic. So, we need to put this flip flops into some value and for initial sequential ATPG techniques. So, they try to do this thing. So, that we can somehow put this flip flops to our desired values, but that is very difficult because it depends on the transition pattern of this finite state machine, that we that gets created here. So, what is done? In the scanned design this flip flops are modified. So, that they becomes scan flip flops and in the scan flip flop modes. So, all these flip flops they can be connected over a chain from the some input which is known as scan input and they are connected over a chain like this. So, they are connected over chain like this and now what happens is, you can very easily set all these flip flops to some desired values and we can get the test pattern part which is, which should be loaded into this flip flops very easily loaded into them.

So, this scan design will convert this sequential design into a scan design. So, when we have done these things. So, we need not consider the circuit any more as a sequential circuit. It can be treated as a combinational circuit only because all these inputs they can be controlled from outside. So, there is no more requirement to check the flip flop. Of course, we need to check whether this flip flops are having correct values they or not we

can they can load the proper values or not for that purpose. So, we can have some flash pattern maybe we write. So, all 0s on to this scan chain and pass it through this chain to see whether at the output also we are getting all 0s or not.

Similarly we can pass some other pattern like alternate 0 1s and see at the output whether alternate 0 1s are coming or not. So, that way we can get the confidence at the scan chain is working properly and after that we can start applying the test patterns that part of which for every test pattern part of it can be in this scan chains.

Now, there are three modes of operation, in a scan design there are three modes of operation normal mode; so in the normal mode of operation. So, this is all test signals are turned off. So, there is no scan chain coming into picture at this point of time. The scan design operates as in the original configuration. So, you have got the same original circuitry as is original circuitry is operating. Then there is something called a shift mode. So, in the shift mode so we shift the test pattern into the scan chain, so that is the shift mode and then in the capture mode. So, the response of the circuit is captured corresponding to the applied test pattern. So, that way it can be the response gets loaded into the scan chain and then there would be another shift out, which is not shown explicitly because that is basically a shift mode part. In a shift mode while we are shifting in the next test pattern, the previous response can be shifted out. So, that way we can do this shift, this response shifting together with the pattern, test pattern shifting. So, this is the test mode signal TM is used to turn on the test related fixes all whatever test necessary.

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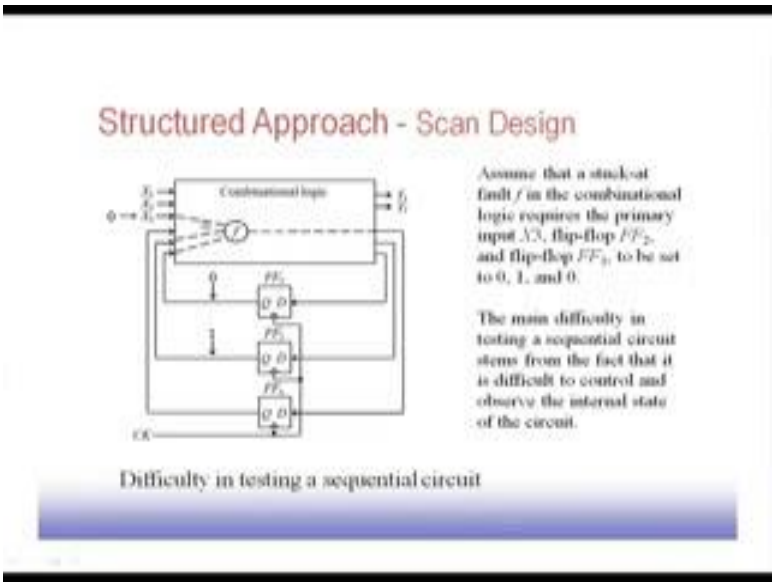

So, this is the scan design. So, suppose we have got some stuck at fault at this a point f. Now to excite this fault f, it may be necessary that we need it may be requires at the primary input X 3 flip flop f 2, FF 2 and the flip flop FF 3, they should be set to 0 1 and 0. So, this should be set to 0, this should be set to flip flop 2 should be set to 1 and flip flop 3 should be set to 0. So, this is the test pattern requirement. Now as I was telling the difficulty is so this bit since, this X 3 is primary input. So, you can easily set it to 0, but the problem comes in setting this 2 bits to 0 and 1. Why? Because when you reset this whole finite state machine, this flip flops are in some state depending upon the start state of the system and then the transitions will occur into this flip flops as defined by the finite state machine itself, the specification of the finite state machine.

So, after the say so whether I can get this particular state very easily or not. So, it depends on the FSM. So, what is done? In case of scan circuit, this will be converted into a pure combinational one. So, and this is actually the difficulty that I was talking about in testing sequential circuit. So, getting this scan, getting the flip flop into some desired values, so getting FF 3 to 0 and FF 2 to 1.

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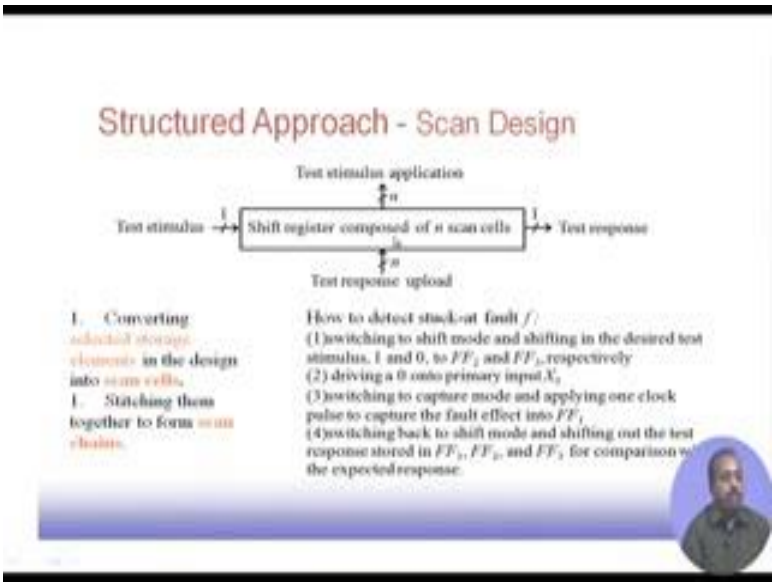

So, in scan design what is happening is that, this all these flip flop they are converted into a shift register and suppose if I have got n flip flops in the circuit, then n the shift register will consist of n scan cells and they are. So, there is a test stimulus pin that is added to the system. Through this test stimulus pin the pattern will be, this register will be loaded serially. In n clock cycles this shift register will be loaded serially. Now after this shift register has been loaded then this test stimulus will be applied to the circuit and then the response of the circuit will be captured on to this scan flip flops and then it will be done.

So, for the previous circuit that we had so previous circuit I have to apply f 3 and f 2 as 0 and 1. So, what do you do? So, first of all we switch to shift mode and shift the desired test stimulus 1 and 0 to flip flop 2 and flip flop 3. So, this can be done by shifting serially and then after this has been shifted then, we apply 0 to the primary input X 3. Now, X 3 has got 0, flip flop 2 and flip flop 3 have got their desired values. Now we switch over to capture mode and apply one clock pulse. So, that the circuit operates normally. So, that and the responses they get loaded into the flip flops. So, this flip flop 1, 2 and 3 they have got their responses captured. And then we go back to the shifting mode and we shift out the response flip flop 2, 3; 1, 2 and 3 for comparison with the external at the good response. So, what is happening? If this is the actual, this is if this is the circuit and the test that we want to test.

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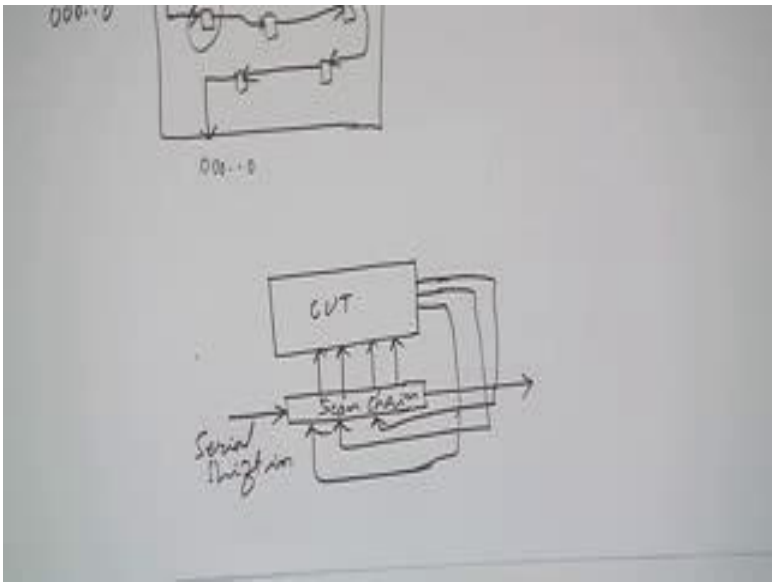

Now, we have made a shift register which is also known as scan chain. So, in this scan chain we serially shift in. So, this is the serial shift in and after we have got this data shifted in. So, we load this pattern. So, this pattern will be applied to the circuit by means of applying in the capture cycle by applying this input to the circuit. So, the test pattern is applied.

Now, what happens is that, the circuit will respond with it, with the output values and the output values will again be loaded on to this scan chain. So, output values suppose these are the output values. So, they will again be loaded on to the scan chain. And once they had been loaded, then we can shift out the response from the chip, from the scan chain by again going to the next shift in mode. So, it will be shift out the pattern and it will be getting the output visible at the scan chain output.

So, what is done? So, we convert, now here what we have assumed is that if the circuit has got n flip flops then all those n flip flops are converted into scan cells. Now if we convert a selected range of them. So it maybe that we do not convert all of them to scan flip flops because of some reason that we will see later. So, that maybe converted into a partial scan type of design and then we need to stitch, we need to connect between all these chains, all these a flip flops to a form a scan chain.

Now, in a design I can have a single scan chain or I can have a multiple scan chains. So, depending upon the design that we do or this number of scan chains we create. So, we

can have single scan chain, we can have multiple scan chain so both are possible. Of course, for if I have got multiple scan chain then I must have the provision for loading those chains separately. So, in most of the cases we have got multiple scan inputs and scan in and scan out pins for that or some another type of chaining can be done there. So, that we can visualize them as separate chains and load them in one chain at a time.

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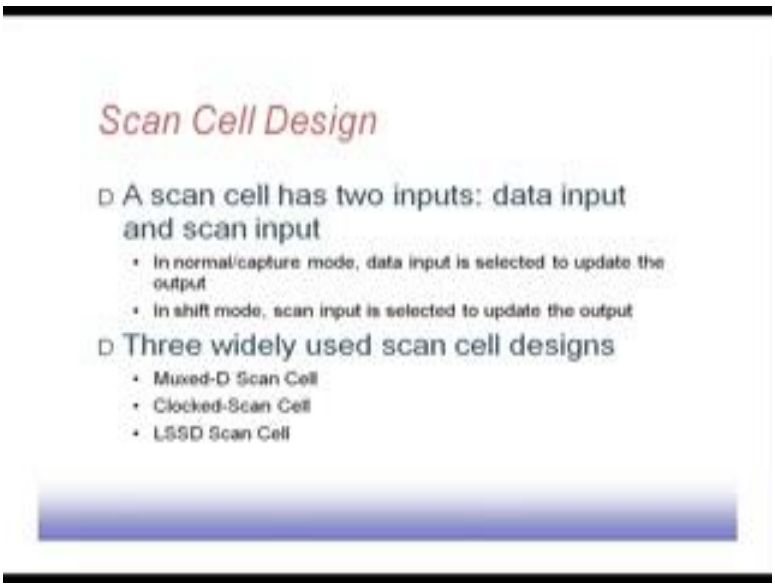

Now, how do we convert is normal flip flop or normal latch into a scan cell, normal sequential element into a scan cell? Say scan cell it will have two inputs; one is called a data input, another is called a scan input. In normal mode or in capture mode data input is selected to update the output and in the shift mode scan input is selected to update the output. So, we have got two modes; normal mode and shift normal mode, normal and capture mode and shift mode. So, depending upon the mode so the data input or the scan input will be going to the output. There are three widely used scan cell design techniques one is a Muxed D Scan Cell, Clocked Scan Cell and LSSD Scan Cell.

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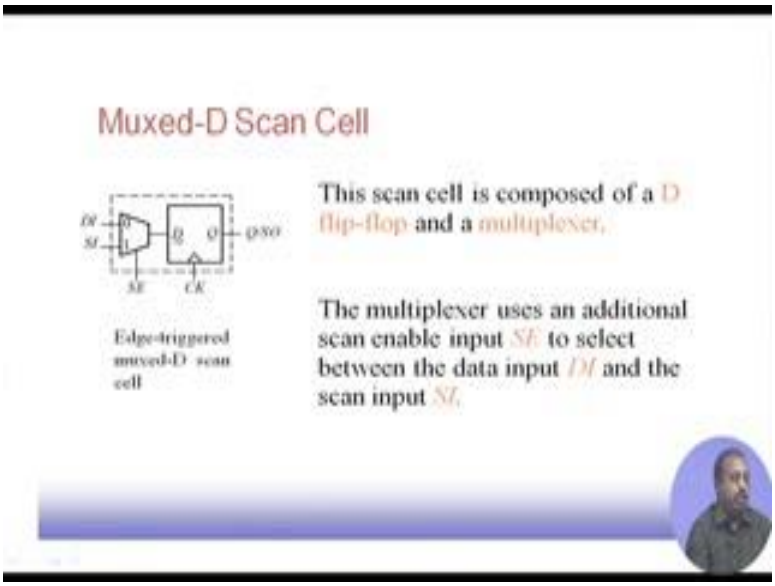

The first one the Muxed D scan cell is like this. So, before the flip flop we put a multiplexer. So, this flip flop is the original flip flop that we had in the circuit. So, before that we put a multiplexer. So, this multiplexer has got two input; data input and scan input and there is a scan enable line. So, if this data input is, if we want that the circuit will operate normally then this data input will be selected and this data input will go to this D flip flop and that way the circuit will operate normally. On the other hand if we are thinking about putting some test pattern on to this flip flop then, this scan input will be, scan enable line will be made equal to one and the value that we put on the scan in line. So, that will be loaded into this through this multiplexer it will come to the D flip flop.

So, this edge triggered. So, this is this particular design is an edge triggered Muxed D scan cell. So, it is possible that in my design I have got my edge triggered D flip flops. So, if my design uses this edge triggered D flip flops. So, we can put multiplexers before that and convert it into Muxed D scan cells. And since you can understand that this can be, this process can be automated very easily. So most of the CAD tools they will allow us to do this change automatically. So, they can do this conversion automatically.

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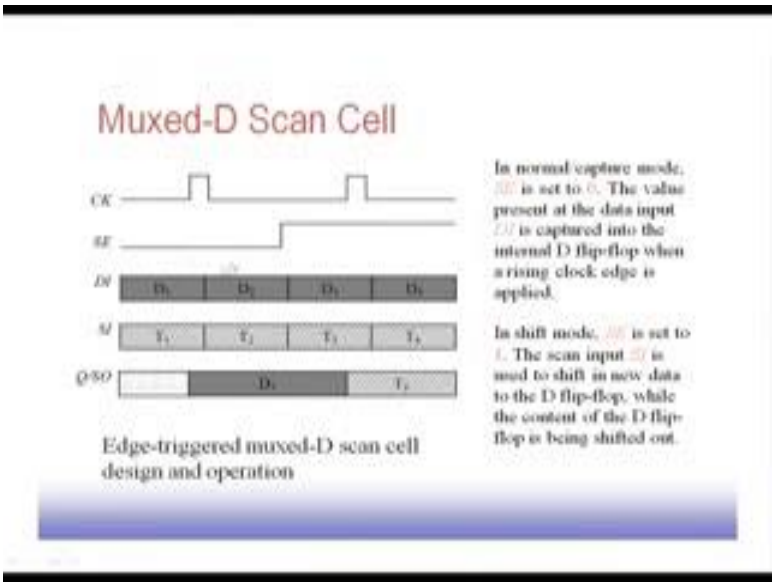

So, this is the timing diagram. So, when you are applying say, when this scan enable the SE line is 0. So, at that time whatever be the content of data input DI, so that whenever the clock comes so it gets loaded into the flip flop. So, this Q are the SO lines. So, they will be getting this. So, now, after sometimes so here the clock was high. So, the value D 1 got loaded. After that this clock comes again at this time, but by that time the scan enable line has been made high. So, when this clock comes. So, instead of loading this data D 3 so, it loads the test value T 3. The test input T 3 to this SI line and that T 3 is loaded here. So, this is the. So, depending upon this scan enable line made low or high. So, either the data input is loaded or the scan input is loaded.

Next, we consider level sensitive edge triggered design. So, what happens is that in some cases. So, if that Muxed D scan cell what was happening is that the flip flop that was being used. So, that was an edge triggered flip flop. Now if my design is such that it uses level triggering. So, it does not use this edge triggering. So, incorporation of this edge triggered flip flop into the system will interact with the design. So, the design will not operate correctly. So, what is required is, for my scan operation I want this edge triggering, but for normal operation I want level sensitive operation or this latch based design.

So, this is basically this level sensitive, edge triggered Muxed D scan cell design. So, what happens is for the normal operation of the system this clock input is high and this

scan enable is low as a result whatever is the data input it comes here. So, it come it goes to this D flip flop and then it goes to this Q output. So, this level this latch will be operating as level sensitive latch for the clock and it goes there, goes to the Q output, it operates as a D latch.

On the other hand, when I am talking about the scan operation, scan operation is edge triggered. So, I have a D flip flop here. So, that is edge triggered flip flop. So, when this scan mode is on, then this scan value the SI will be coming to this D input and then that. So, once it is there in this D input when this clock was high. So, it got latched here, but the value will be come to the scan cell only when this clock edge comes, the negative edge of the clock comes. So, here on the when the level, clock level was high at that time the value came here and when this now the clock edge goes down, on the falling edge of the clock the value get latched on to this flip flop.

So, in this case shift operation is conducted in an edge triggered manner, while normal operation and captured are conducted in a level sensitive manner. So, if my design is such that it does not support this edge triggered operation, it supports only level sensitive operation then this instead of using this Muxed cell we have to use this Muxed D scan cell. Another possibility is that we have got two different clocks; this data clock or two independent clock, data clock and this scan clock.

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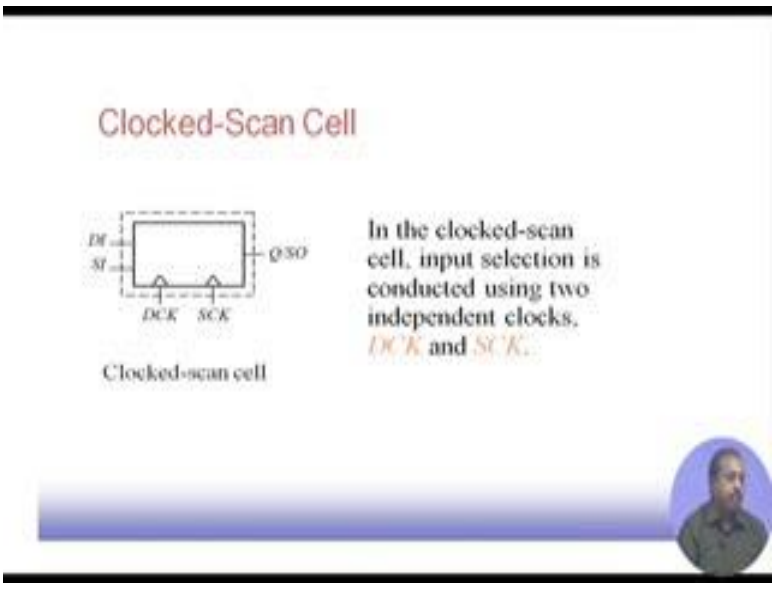

So, this is another possibility. So, the cell is designed in such a fashion that it operates with two different clocks; so this when, the data clock is given, so the circuit operates in a normal mode and when this scan clock is given the circuit operates in a scan mode.

So, in a clocked scan cell the input selection is conducted using these two independent clocks DCK and SCK and in the. So, they are to be. So, applying these clocks is a bit crucial because they have to be done in such a fashion that they are not applied simultaneously. So, these has to be done. So, they are applied in non overlapping fashion and that is ensure like if this testing is done by some test engineers. So, the test engineer will definitely ensure that this data clock and the scan clock they are non overlapping in nature.

So, this is the operation of a clocked scan cell. So, here I have got. So, this is suppose a data input and this is the scan input. When this data clock is given so value D 1 is put into this Q and when this scan cell is scan clock is given then, this scan data SI is loaded into the flip flops. So, you see that we have got this DCK and SCK. So, they are applied in a non overlapping fashion and when they are applied in a non overlapping fashion. So, we can load the values on to the corresponding latch and the flip flop the Q and SO line can come accordingly.

So, in normal or captured mode the data clock DCK is used to capture the contents present at the data input DI into the clocked scan cell. The shift mode, shift clock SCK is used to shift in new data from scan input SI into the clocked scan cell, while the content of the clocked scan cell is being shifted out. So, that shifting is done simultaneously for input test pattern and output response of previous pattern.

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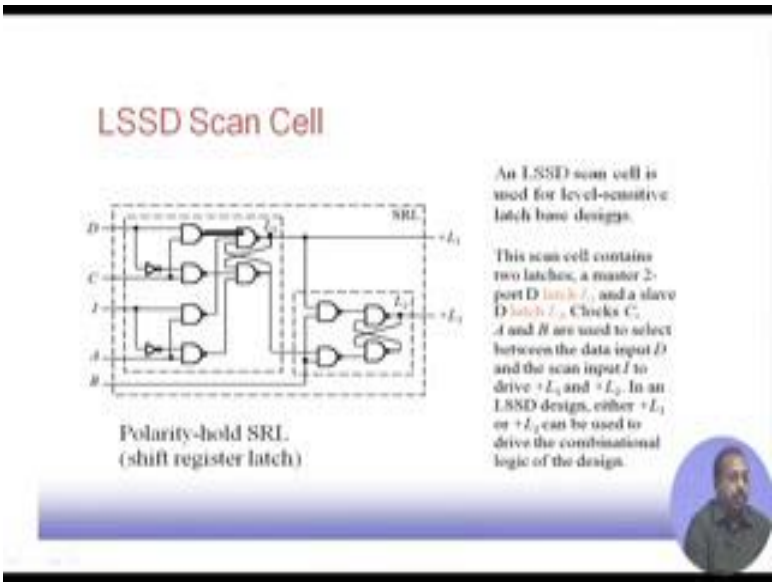

Another type of design which is known as LSSD scan cell, here what happens is that, it is used for level sensitive latch based design. So, here the scan cell consist of two latches. So, this, a master two port latch L 1 and a slave D latch L 2, so clocks C, A and B. So, these are the different clock signals. So, they are used to select between data input D and the scan input I, to drive this L 1 plus and L 2 plus. What happens is that? So, this is the latch. So, this line can directly drive the combinational circuit or it can it may so, happened that through a double latched goes and after L 1, it comes to L 2 and from L 2 it actually goes.

So, we have got to select between this a plus L 1 and plus L 2. In LSSD design either plus L 1 and plus L 2 can be used to drive the combinational logic part. So, that is the. So, we have in some cases. So, in some design it is double latch design. So, that the double latching is provided and if it is in some part is not double latch. So, it is single latch then it will be going from plus L 1 only.

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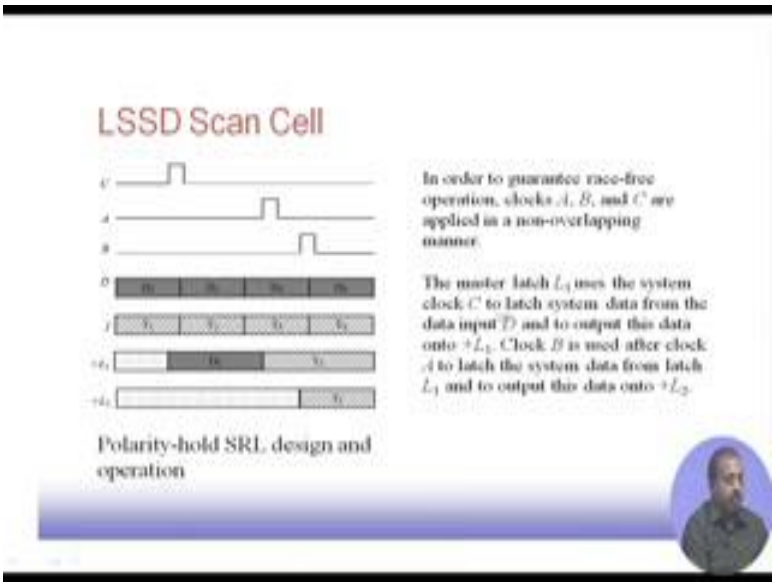

So, this is the operation. So, when this C clock is high then latch L 1 uses the system clock C to get the data from D and put it on to the output. So, this D data is coming. So, D goes to plus L 1, it does not go to plus L 2 does it goes to only plus L 1 line. On the other hand this clock B is used after clock A to latch the system data from latch L 1 and send the data to L 2. So, if you look into this design first, this when this clock is applied. So, data is coming to L 1 and after that this clock A is applied. So, that this L 1 data goes to L 2 and after that this clock B is applied. So, that this data is coming here. So, that is going to plus L 2.

So, if you want that the circuit B driven by plus L 2. So, we have to apply clock in this sequence C, followed by A, followed by b, but if you want that it will be applied the data B available from plus L 1 itself then, we do not need to apply this A and B. So, it can directly go from this C. So, if you design does not support this edge triggered flip flop at all. So, suppose for my scan chain design also I do not use this edge triggered flip flops. So, for that purpose I can use this type of design. So, that we can use this three clocks; C, A and B in this sequence that is; first C, then A, then B. So, that this content gets shifted through this plus L 2 line. So, we have got some provision for that.

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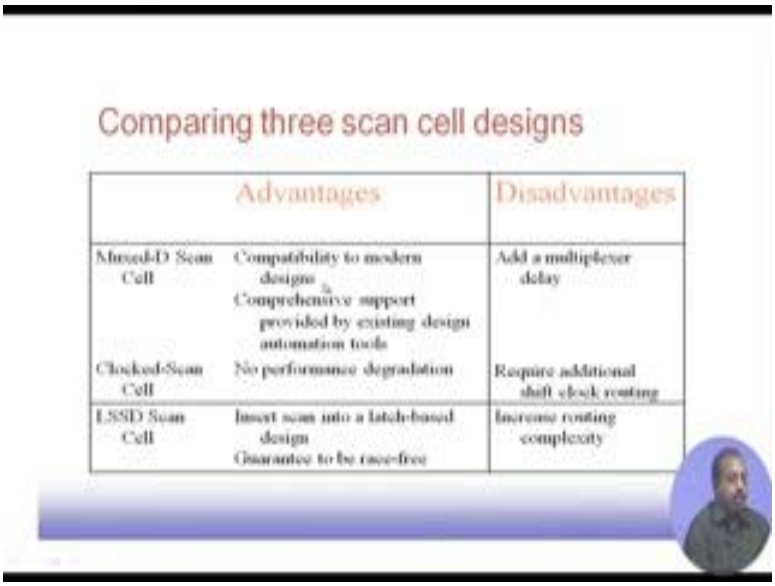

So, to compare between this, so this Muxed D scan cell. So, the compatibility, it is compatibility to modern designs. So, that is there then, a disadvantage is that it adds one multiplexer delay. So, before the flip flop we have got multiplexer. So, that multiplexer delay will come into picture. They provide comprehensive support for to by existing design automation tools. As I was telling the process is very much automated now. So, you can ask the CAD tools to do this scan chain insertion. So, it will find out all the flip flops that we have in the design and it will modify all those flip flops to scan flip flops do the proper stitching between them. So, that you get the scan chain made.

And this clocked scan cell, so the advantage is that there is no performance degradation because now i do not have any multiplexer into the picture. So, the flip flop does not have any multiplexer before it. So, that delay does not increase. So, even if that flip flop comes on to the critical path the delay is not increased. So, we have got the performance of this system is not sacrifices; however, the disadvantage is that we required additional shift clock routing. So, in the clocked scan cell we have got two clocks. So, and the two clocks are to be distributed throughout the chip. So, wherever this flip flops are there, scan flip flops are there so there that both the clocks should go. And clock routing is one of the very important problem in the VLSI design process because thus Q in the clock, the power consumption. So, they play major role in deciding how the clock should be distributed.

Now, if you have this another clock into picture. So, then that also has to be routed and same two different parts. So, that increases the complexity further. And for LSSD scan cell. So, we can insert scan into a latch based design. So, this is the point I was talking about. So, if that, if you design philosophy does not allow flip flop based design. So, previously whatever technique we have discussed the scan part that was done by the flip flop. So, for circuit opera normal operation it was through it maybe through latch, but for scan parts. So, this done by the flip flop.

So, if the design philosophy does not allow you to have this flip flop based design then what to do? So, then we have to have latch based design only. Then, this LSSD chain, the LSSD scan cell design so that is actually allowing us that avenue. So, you can have a full latch based design of your scan chain and by controlling this C, A and B properly. So, you can make it to operate as a scan cell. So, it guarantees to be race free and it also increases the routing complexity.

So, stop here in this lecture continue in the next one.