Digital VLSI Testing
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Lecture - 42
Boundary Scan (Contd.)

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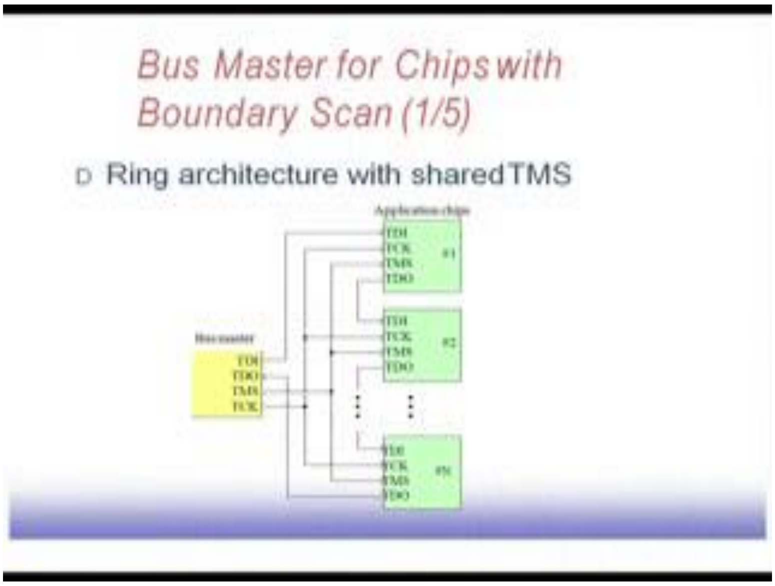

Bus Master for Chips with Boundary Scan (1/5)

- Ring architecture with shared TMS

So, bus master architecture for chips with boundary scan. So, one possibility is that they are connected in a ring’s architecture. So, this bus master has got this TDI, TDO, TMS this mode select and this clock signal. So, what happens is that this application chips, so they are connected in a daisy-chained fashion. So, as we have shown in the very first slides, very first few slides in the boundary scan technique that the TDO of first chip is connected TDI of next chip, so that way it is connected. TDO of second chip connected TDI of third chip and finally, the TDO of the final chip comes back to the TDO of the bus master. And these test modes select line, so it is common to all the chips. So, all of them are doing the same mode of execution, and the clock signal is also common, so that is going. So, this way they are connected in a ring form, so they execute the same instruction in all the chips.

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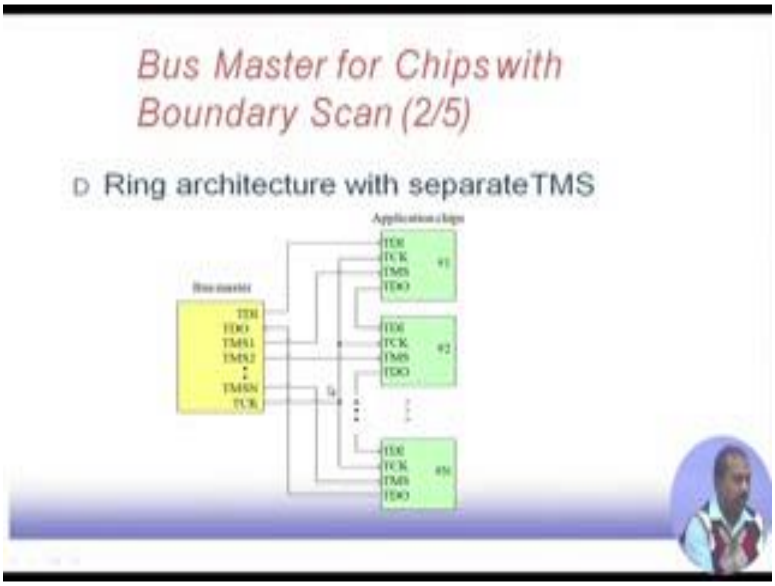

Bus Master for Chips with Boundary Scan (2/5)

- Ring architecture with separate TMS

So, we can have with separate test mode signal like say if we want that different chips should execute a different test mode instructions like some of them maybe doing EXTEST, some of them INTEST some of them are doing IR configuration. So, like that, so if it is different then you need to have a number of this test mode select lines which are distinct for different chips. So, we have got one TDI and one TDO that part remains same, so then they are they are daisy-chained, so TDO is output connected to the TDI of next one and all that, but this TMS lines, so they are distinct. So, these for each chip, there is a TMS line; and this clock signal is common to all them. So, that the test clock signals, so that is common to all of them, so here separate architect separate ships can execute separate instructions.

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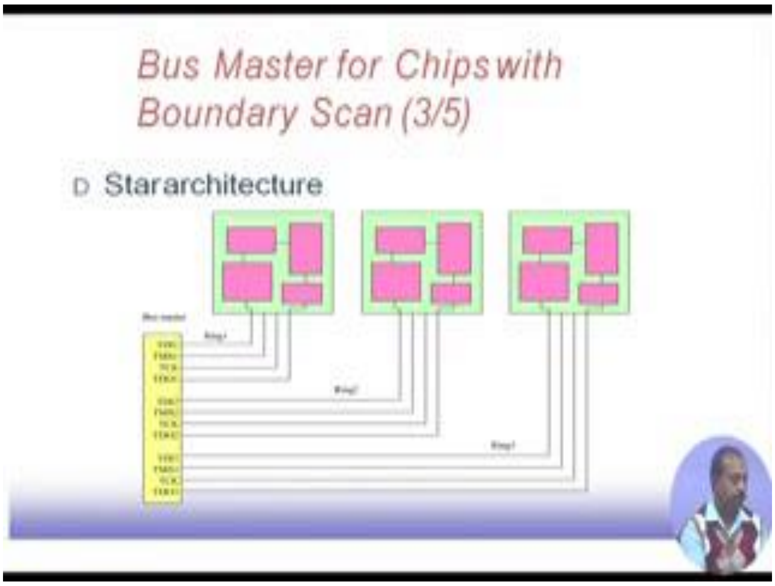

Bus Master for Chips with Boundary Scan (3/5)

- Stararchitecture

Can also have a star type of architecture where we have got to one bus master, but there are several such rings. So, this is these chips are in one ring, these chips are in another ring, these chips are in another ring, so that way we have got 3 different rings. So, in a particular ring, so we have got TDI one test data input one and test data output one, so they are forming the boundary scan for the first few chips. For the second module, I have got TDI 2 and TDO 2 forming that chain; and third one TDI 3 and TDO 3 forming the chain.

So, we have test clock signal is actually common to all of them, here it is not shown explicitly, but the same TCK line is going to all of them, but this mode select line is different. So, all chips within the first ring they execute same instruction; similarly chips within the second in they execute same instruction like that. So, this is also a possibility if we got large number of chips, so if we want them to operate in different modes then this may be the possibility of connecting them.

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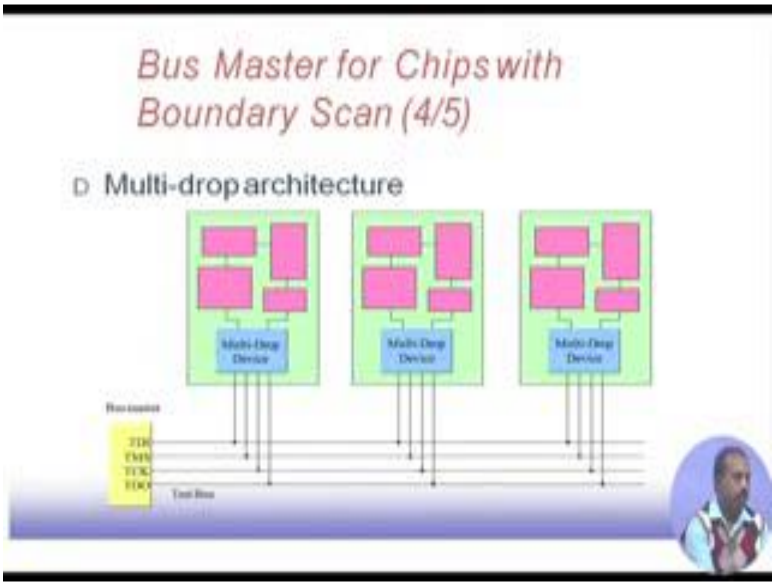

Bus Master for Chips with Boundary Scan (4/5)

- Multi-drop architecture

Now, multi-drop architecture, so multi-drop architecture means from this is like a bus, so your test bus consists of these 4 lines TDI, TMS, TCK and TDO. And naturally we have got a multi-drop device connected to each bus. So, in this particular case, what happens is this TDI signal is trans; all this signals are transported over the bus now there must be some sort of addressing mechanism. So, this multi-drop device, it must have some device id; and by looking into this TDI bits it should be able to understand like whether this operation is for this particular device or not. So, if it is for a particular device then only this TDI line will be transported to the TDI of actual TDI of this boundary scan of these 4 chips.

Similarly if it is not that the maybe this device has been addressed, so based on that address, so TDI line will be coming to these chip, so that way it may be possible that we have got a multi-drop bus type of structure but as we know that it makes the design simple because I have got a simple bus from higher a number of devices are dropping, but the problem is that since we have got a number of devices, so bus performance is going to be affected. So, you cannot to drop a large number of devices from a bus, so as it crosses say 8 or 10 devices then it starts showing declination in the performance, so that is another issue. So, bus master configuration with this multi-drop architecture, so this can also be used in many cases.

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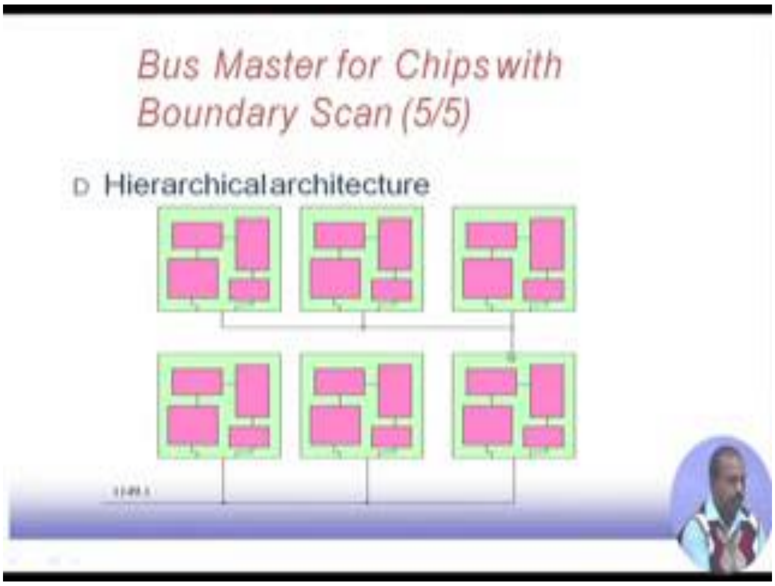

Bus Master for Chips with Boundary Scan (5/5)

- Hierarchical architecture

So, another possibility is a hierarchical organization. So, hierarchical organization, so this is 1149.1, so all those lines that TDI, TDO then your TMS and TCK, so all those lines are coming here, so they are connected on a multi-drop fashion on this. And so this is the first level of hierarchy. Whereas, if this TDO, so from these chip, so it may be going to the next one that is forming the next level of hierarchy. So, these devices they are at the first level, then this chips they are at the first level of this hierarchy, this chips are at the second level of hierarchy.

So, this hierarchical architecture can also be used, so it depends on a type of application that we have if the set of commands that are required for testing say this set, this set of chips is less and less complex compared to the first one then may be this may be a possibility. So, when may be whenever we are going to test these particular chips all this chips are to be tested, so in that case also it may be the thing that it is configured like this. So, this hierarchical architecture, so that can also be used so depending upon the application that we have the types of chips and the way we are going to connect them their physical location on the board, so this hierarchical architecture may be beneficial.

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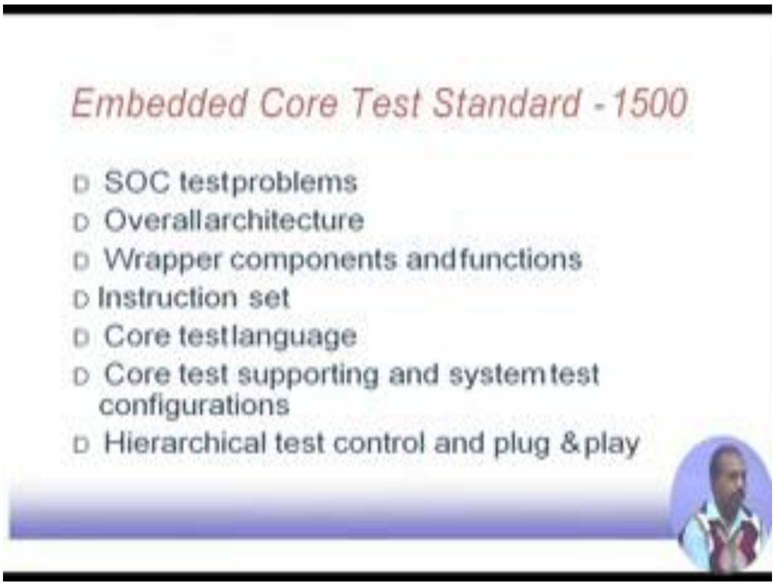

Embedded Core Test Standard - 1500

- SOC testproblems
- Overallarchitecture
- Wrapper components andfunctions
- Instruction set
- Core testlanguage
- Core test supporting and systemtest configurations
- Hierarchical test control and plug &play

So, that talks about 1149.1 standard. So, there is another standard 1149.6 which we do not discuss in detail in this course, because that is some extension like it has supported the high speed application high speed test bus, then it has got analog interface and things like that. So, some augmentation has been done. Rather we will look into another standard for embedded core test which is known as 1500 standard. So, this 1500, so this standard is similar to 1149.6, but instead of being applied at board level, it is applied at the chip level, it is a core test standard. So, we will look into this, so the sub domains that we look into is associate test problem what are the problems there then architecture what is the architecture upper configuration, etcetera.

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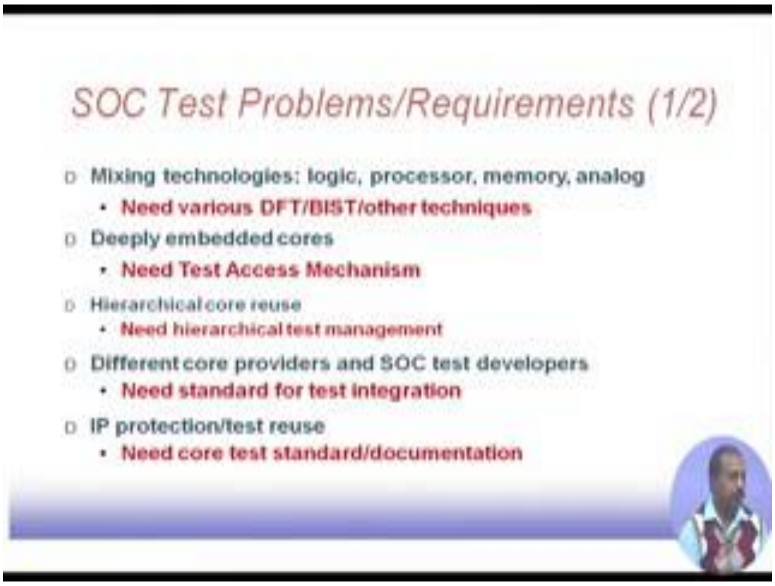

SOC Test Problems/Requirements (1/2)

- Mixing technologies: logic, processor, memory, analog
  - Need various DFT/BIST/other techniques
- Deeply embedded cores
  - Need Test Access Mechanism
- Hierarchical core reuse
  - Need hierarchical test management
- Different core providers and SOC test developers
  - Need standard for test integration
- IP protection/test reuse
  - Need core test standard/documentation

So, what are the SOC test problems or requirement? First of all what is SOC, so system on chip based design is a way ahead step ahead to the board level design. As I have told that in a board level design, we get the different chips from different vendors and we integrate them on a board. Now, if I have a board then maybe on this board, I have put a number of chips and then these are various chips that we have.

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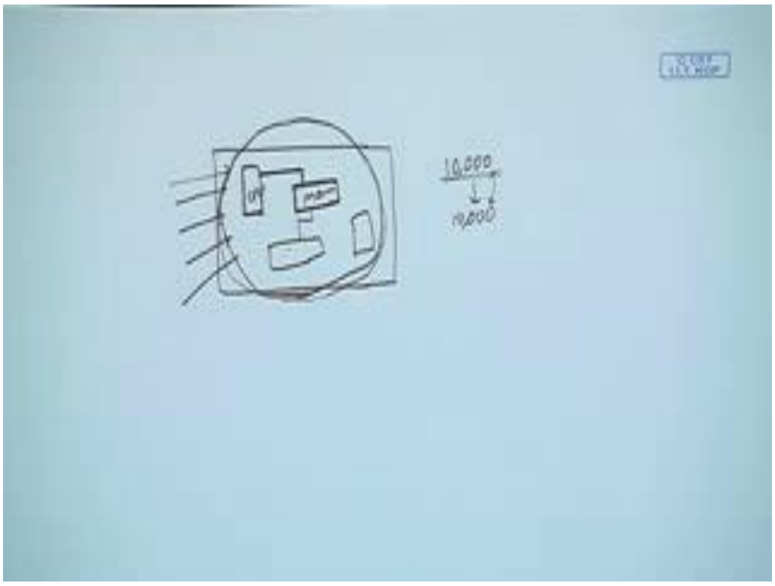

And for testing purpose, so this chips they are said to be they are shipped into the market by the vendor, and they have done their own testing, so naturally we can be confident about their correctness. So, these chips they may be assumed to be correct. But what we need to test is the interconnect between the chips, so this interconnect, so this is a copper line running between 2 chips, so that line has to be tested. Similarly, this may be another copper line running between the chips, so that has to be tested, so this way we need to test this individual chips individual interconnects. So, chip testing is not a major concern when we are going for this board based design. But is the problem with board based design is that as we are trying to speed up, as we are trying to increase the performance of the system, so it is seen that this of chip communication is at least ten times slower than on chip communication.

So, if this happens to be the say the CPU and this happens to be the memory then, within CPU cause communication is much faster as we know the register access is the fastest is very first within the CPU. But whenever CPU tries to access memory, so it has to access using of chip bus and then speed drops, so latency though you went memory both are semiconductor devices. It is due to the interconnect physical interconnect that we have outside the chip that may be a copper or maybe some other metal, so that is going to introduce the delay.

So, how to break this is speed bar barrier, so speed maybe this barrier may be broken if this entire thing is fabricated on a single dye. Now, when we are doing that when we are trying to do this thing, so I am not interested anymore in the chip available as CPU or chip available as memory I am rather interested in getting the in getting some synthesizable descriptions of them, so that I can do my own manufacturing of the whole unit together. So, for that matter, I have to go to different vendors take their designs, but as soon as I say that, so it is contradictory because say no CPU designer company will give me their design as such, so that I can manufacturer it.

So, rather what they will give is some sort of a layout level description of the components. So, layout level description after CPU, layout level description of the memory, so if those layouts are manufacturer to properly they are fabricated properly on a silicone dye then the whole thing will operate. And as system integrator, so my role changes from designer, it becomes integrator as a system integrator what I need to do is to add some extra logic add some interconnect between the devices, so that this whole thing is become whatever I am looking for, so that a design is implemented.

So, the major problem that we have is now we have to mix up various technologies like we have there are some logic design, some extra logic that I was talking about, so some extra thing that is needed that has to be there, then there are processor is there memory is there then we analog components. So, we will see later that this memory testing itself is a different domain, so it does not follow the conventional fault models and conventional test techniques. So, for that I need to have a different type of test. Similarly, analog circuits if we are going to test then they require different types of test, so it is very much unlikely to have the expertise of all these techniques available at one place.

Secondly, generation of test pattern is difficult because I do not have the full detail of all these components. So, I cannot to design at ATPG process, so that test pattern can be generated for the processor until and unless I have got the gate level net list of the processors. So, naturally that stops an integrator from designing the test vectors or test technique for a particular component of this board or this chip. So, what we have to do is we have to rely more on the core developer, core vendors, so they will also provide the test pattern, they will also tell how the test patterns may be applied what are the responses, etcetera.

So, we need various DFT BIST or other techniques. So, design for testability BIST some of the cores may be BISTED core, they have got there a BIST mechanism there, so from outside world I need to just trigger the BIST, some of them may be having some particular type of scan chain configuration. So, from outside world I have to feed those can chain with proper patterns, so the requirement changes unlike if design which is done in house and it is done by the single designer, so here actually different vendors core vendors, they have got their own DFT, own BIST and all those things, so bringing compatibility is a big issue. So, from outside world, we have to do something we have to add some extra thing into the system, so that it becomes the whole thing becomes compatible and the test sessions can be run.

Second important problem with SOC based design is the embedding of the codes, so codes are often deeply embedded. So, as I was telling that may be in this example itself I have got this whole thing fabricated onto the chip. Now I cannot say that this CPU is good in a PCB level design or board level design, I could say that the CPU is good because that is certified by the CPU vendor. Now, that is not the situation the processor vendor that is not the situation why, because if everything is fine about this particular design maybe the silicon itself may be impure at that point, so that at way some fault may develop. So, at the since I am designing whole chip myself, so the testing responsibility also come, so I cannot say that this individual components are fine, I need to test only interconnects. So, here the complexity is more I have to test the chips the components as well as the interconnects.

So, if I want to test say this particular component then I have to apply some test pattern. Now, how do I apply test pattern the vendor of this particular module this particular core they have told these are the 10,000 test patterns if you apply and find the corresponding responses 10,000 good responses. So, if it is all correct then you know that this is fine my design has been fabricated properly. Now, how to get rid of how to apply this 10,000 pattern, so core vendor cannot tell because core vendor does not know in which environment it is going to be put. Now it may, so happen that from the chip input, so if these are the inputs to the chip, from the chip inputs reaching this memory itself is a problem, so that access may be difficult.

So, for deeply embedded core, so it is very difficult that we find a functional path through the chips. And we can apply through the cores and we can apply the pattern to the core under test. So, we need to have some sort of test access mechanism, so it may be a functional path through the cores or it may be some dedicated path. So, whatever we do some test access mechanism be has to be designed.

Third important issue is the hierarchical core reuse. So, since today we are designing a system which is consisting of a number of cores, so tomorrow if another system is designed where this system is a component. So, as a result, we are going to reuse the SOC that we had designed previously as a core in the new design. So, naturally these previous SOC that we had designed, so it has got its own test structures in it; and those test structures we cannot change, so they are remain in there. Now for this new SOC that we are designing since this is coming as a core, so for the new SOC, this becomes a hierarchical testing. So, the first level cores are to be tested and then for this IP reuse I have to use the next level of access mechanism, so that way there is a hierarchical core reuse case, so that will be there and we need to have hierarchical test management policies. So, test access mechanism as well as the test scheduling algorithm they should be able to take care of this hierarchy.

Different core providers and SOC test developers, so this is another problem because the there this test developer this core vendors, so or core providers they are having their own design, they have done their own test pattern generation or BIST whatever it is or some DFT or structure. But now after that it is given to the integrator or the integrator with integrators group will also have the test developers who are working at the SOC development work. But the problem is the interface between the group of people, so that is another issue. So, if there is no standard in this integration process, then it is very difficult to follow whatever the test pattern or test testing mechanism the designer has provided and how to exploit it at the system level, so this is another issue.

And finally, the IP protection and test reuse, so we need core test standard documentation. This is another very important issue, so without divulging the IPs how can we ensure that this IP can be utilized its test philosophy can be utilized. So, this reuse IP reuse is very important issue and somehow under this SOC design paradigm, so we have to take care of this.

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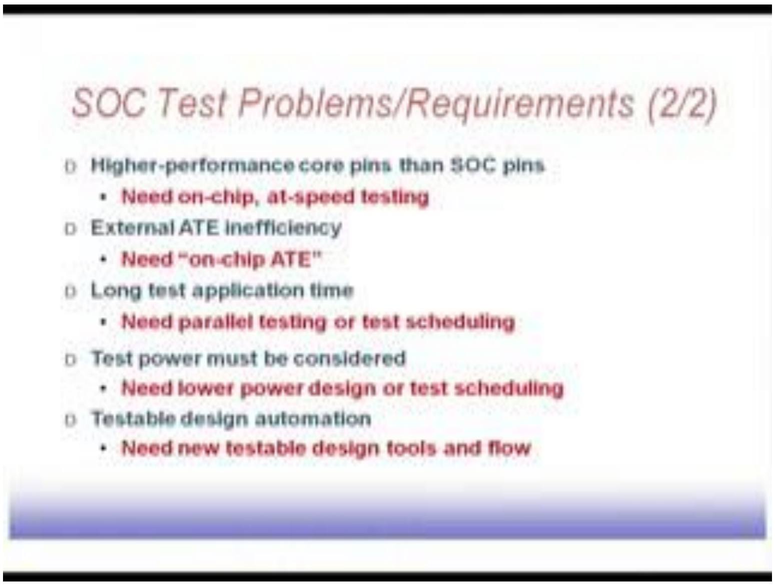

SOC Test Problems/Requirements (2/2)

- Higher-performance core pins than SOC pins
  - Need on-chip, at-speed testing
- External ATE inefficiency
  - Need "on-chip ATE"
- Long test application time
  - Need parallel testing or test scheduling
- Test power must be considered
  - Need lower power design or test scheduling
- Testable design automation
  - Need new testable design tools and flow

Higher performance core pins then SOC pins. So, basically what can happen is that this SOC pins, so we have got may be that SOC operates at some frequency and when we are doing testing in particular, so this SOC pins they are operating at some frequency, but internally the cores they can operate at a much higher frequency. So, this higher performance core pins, so in those cases those pin those IP cores that we are talking about which can operate at higher frequency, they must be done for them we need to do a delay tests, so for that we need some at speed testing of those cores. So that may be there.

Then external ATE, external ATE may be inefficient. So, the problem is that the ATE cost is very high, ATE cost is high and ATE cost is dominated by mainly 2 factors; one is the memory size, another is the frequency of operation the channel that we have number of bits that the ATE can have send parallel to the tester for testing. So, this makes this whole process very difficult. So, this ATE is slow now for a new design in my company may be I am doing a design at a high frequency, but existing ATE is operating at a low frequency, so I have to somehow test this chip with a available low frequency ATE, because ATE equipments are very costly. So, I cannot go for a new ATE just to test this new chip.

So, there must be some mechanism by which I can use this low speed ATE or inefficient in that sense inefficient ATE to do the testing of this high frequency chips that we have.

Or in some sense, we can say we need some sort of on cheap ATE that is a very desirable situation. But it is very difficult to have so one chip ATE is difficult at least at most we can have some sort of beast mechanism by which we can do a built in self test of this individual core that that possibility remains, but otherwise it is difficult.

Then long test application time. So, what has happened in the SOC design paradigm is that you see you have got, so many components to be tested. Now, the IP vendors they have provided us with a set of test vectors for each of the cores. Now, if this entire system was designed by a single group or single person, then they could have filtered out the test patterns or they could have found out the test patterns which can test a number of faults in different components, so that way there may be a possibility of doing a compaction of test set. So, we can identify which of the test patterns are very important, they must be applied and which are not, so important, so that is possible only when we know about the design detail, how it has been designed, very which part was taking care of the most important operation of this module. So, like that in the absence of those information, so we cannot do any pick and choose, so what we have to do is simply apply all the test patterns that the vendor are provided, the core vendor has provided to the core under test. So, that makes the problem of this test time and important issue, so we this test time becomes very long somehow we need to handle this problem.

So, how can we reduce time, one possibility is to do parallel testing. So, you test a number of modules parallelly, so that is that way the test time will get reduced. Other possibility is do such some sort of test scheduling, so we schedule this the testing in to session, so that it is divided into proper time frames, so we will have some tests parallelism implemented. But this test parallelism has got its own problem as well because the test power is another important part that comes. So, number of modules being tested parallel means the number of modules they are going to consume power. So, as we have discussed previously that in normal mode of operation, those modules may not be working simultaneously, but in the testing process to reduce the test time we have made all of them to work together. So, if you do this thing then of course, there is a necessity to have high power consumption it may be possible that all those power values are high, so as a result they consume lot of power.

So, we have seen lot of discussion on the test power minimization, but test scheduling is another way by which we can schedule this core tests, so that they do not consume high power. So, high power consuming cores will not be tested parallel or something like that has to be evolved. Then testable design automation, so this is the tool flow that we that has to be created, so that given a design and this other parameters like this vendor specific parameters, then this whole testing process has to be automated, so that is the other issue. So, these are the important problems and requirements for the SOC test issue. And we will see that how this problems will be addressed in the subsequent discussions.

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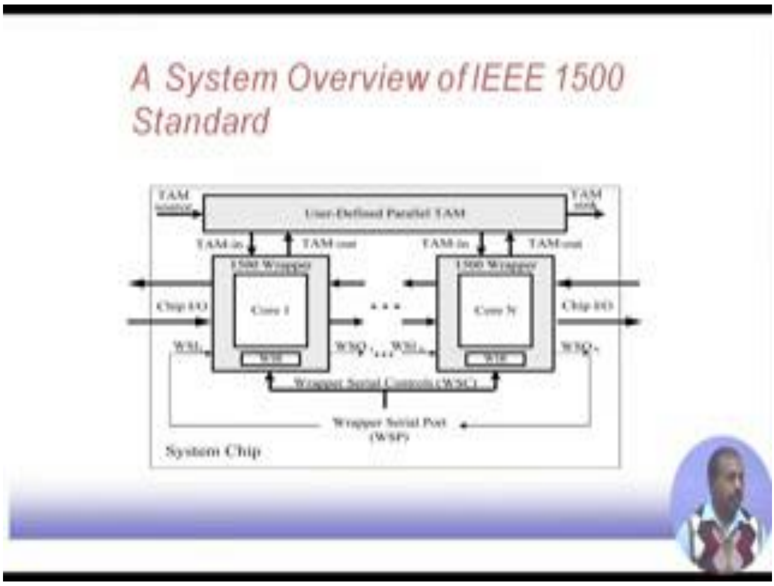

A System Overview of IEEE 1500 Standard

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So, this is a typical view of this P 15 this IEEE 1500 standard. So, we have got this sort of structure, so these are the individual cores core one, core 2 up to core N. Now this cores they have got this 1500 wrapper, so every core is wrapped with this 1500 wrapper, so that from this interface it appears to be uniform. So, this interface we will have some parallel inputs like this chip input output pins it may be coming to this say core one and naturally they are to be passed through this P1500 wrapper there you can understand there should be some sort of boundary scan cell here through which this input will come to each core one. Similarly there will be some boundary cells here by which core one output will go there. So, this cheap parallel input output, they will be fed to different cores and they will go like this.

Apart from that we have got there may be other thing in the sense, there may be some more mechanism by which the user can apply a number of test bits parallelly, so that is known as a test access mechanism. So, this may be user defined parallel test access mechanism, so from test source, which may be ATE channel or something like that. So, some ATE channel may be test patterns will be transported through this TAM; and similarly at this end, we will have the TAM sink, so that may again be the signal values response values going to the ATE. So, this way the user may define some parallel test access mechanism. So, from this parallel test access mechanism this TAM in line, so that they can come to this 1500 wrapper similarly tam outline may be feeding this timeline. So, if the user has seen the test patterns into this TAM line, so this TAM in it can reach this 1500 wrapper and through which it can be applied to core or it may be possible this wrapper has got serial inputs that WSI. So, WSI serial input may be given from this serial wrapper serial port and that way it can that test pattern may be fed serially in to the boundary scale cell. And from there this boundary from the boundary scale cell it can be applied to the cores.

Similarly, we have got a number of WSI and WSO lines for each chip has got one WSI line and WSO line and they may be chained in some fashion, so that we can say that this scan patterns can go serially through this chain. And there will be some wrapper signal controls which controlling this wrapper signals, so how this shifting will takes place, whether it will be a parallel capture or serial capture parallel transfer or serial transfer, so all those things can be controlled by this wrapper control. So, this 1500 has to do this whole thing, so it has to control both the serial part as well as the parallel part.