Spread Spectrum Communications and Jamming

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Lecture – 45
FHSS Tracking

Hello students as we are done with the frequency-hopping code acquisition technique for frequency-hopping spread spectrum receiver. Today, we will discuss about the frequency-hopping spread spectrum communication tracking mechanism since at the receiver.

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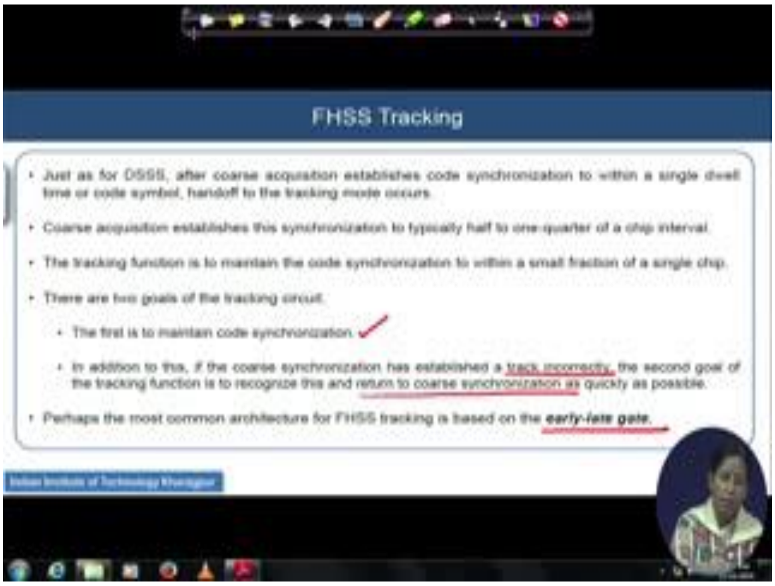

FHSS Tracking

- Just as for DSSS, after coarse acquisition establishes code synchronization to within a single dwell time or code symbol, handoff to the tracking mode occurs.
- Coarse acquisition establishes this synchronization to typically half to one-quarter of a chip interval.
- The tracking function is to maintain the code synchronization to within a small fraction of a single chip.
- There are two goals of the tracking circuit.
  - The first is to maintain code synchronization. ✓
  - In addition to this, if the coarse synchronization has established a track incorrectly, the second goal of the tracking function is to recognize this and return to coarse synchronization as quickly as possible.
- Perhaps the most common architecture for FHSS tracking is based on the **early-late gate**.

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Like direct sequence spread spectrum communication here also, the tracking is performed after code acquisition is done, I mean the code alignment, coarse alignment is done by any one of the three techniques that we have discussed. And then we really understand that there is some residual code error, residual offset is there. And we are in by means of tracking we will be trying to correct that and we will be trying to continuously keep on monitoring the phase offsets that are happening in between the incoming signal and the locally generate sequence time-to-time. And if some offsets are there we need to try to we will try to correct it within the range of the operation.

If the correction is not sufficient to bring them align in them again then it is a job of the tracking circuit that he will trigger the coarse alignment once again. And because if it goes beyond its correction range, it will trigger the tracking code acquisition once again; and then code acquisition output of the code acquisition will be fade again to the FHSS tracking network.

So, the goals are two types goals are of two fold. The first one is actually to maintain the code synchronization both the coarse as well as the fine. And in addition to this, if the code synchronization has established the track in correctly always incorrectly already it is.

The second goal of this tracking mechanism is that he will recognize this I mean identify this and return to the code synchronization as quickly as possible. So, trigger turn on the code synchronization as fast as possible. So, he is actually doing a very crucial job, where are the coarse acquisition is also done perfectly or not that is checked first inside the tracking mechanism and in the tracking circuit. And then if it is not done properly then he will trigger the coarse acquisition once again, and then if it is done correctly then he will enter into the second phase. Perhaps the most common architecture of this FHSS tracking is based on the early late-gate.

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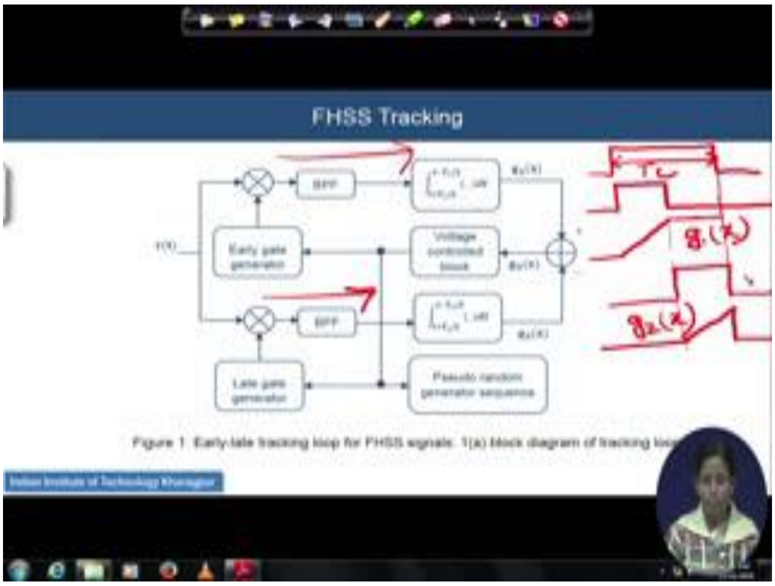

FHSS Tracking

Figure 1: Early-late tracking loop for FHSS signals: 1(a) block diagram of tracking loo

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And the early-late-gate circuit, this is the circuit where actually the FHSS tracking goes on. Remember there is a early-gate generator, and do you remember the hopefully will be remembering that we had a early-gate generator in the DSSS hopping tracking and also we had a late-gate generator in the DSSS tracking. So, similarly here also we have early-gate generated and a late-gate generated in the circuit. And if there is a perfect synchronization with suppose with early-gate and remember this code generator a generating the chip for half of the chip period, and late-gate generator is generating for the remaining half part of the chip.

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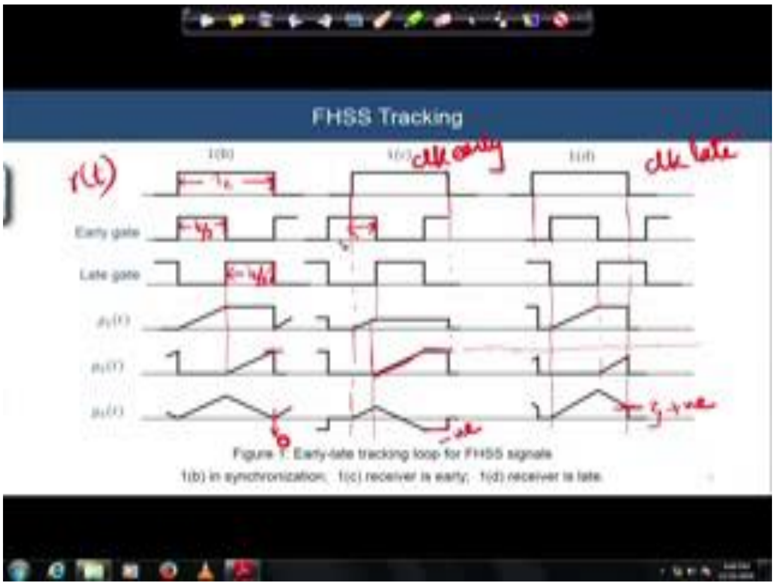

FHSS Tracking

Figure 1: Early-late tracking loop for FHSS signals
1(b) in synchronization; 1(c) receiver is early; 1(d) receiver is late

For suppose example if this is a total duration of a chip, early-gate will be generative with the perfect synchronization sequence where synchronization point early-gate will be perfectly generating the chip for the half of the period; and late-gate will be actually generating an another chip for the next half of the period, clear. So, given that it is T c. So, T c by 2, T c by 2 is taking care by the early-gate and the late-gate. And when they have synchronized also, so the early-gate outputs this integrator output, so the after this multiplication and the band pass filter when this instigate when enters into the integrated for the early-gate generator, this integrator integrates for the period of the first half only and it generates an output called g 1 x.

Now remember if they are in the perfect sink node, there integrator output slowly grows up and it reaches maximum at the end of the T c by 2, and it remains at T c by 2 for the rest part of the chip duration. So, what is happening, we will explain it in the diagram next. So, I am told that if it this is the whole chip duration T c, so for perfect synchronization case for T c by 2 times you are having the gate have generated the pulse from the early-gate generator. If I filtered this signal output, so for this it will be filtered out. And then here are the signal will be now integrated. So, integrator will integrate and slowly if I integrate a square wave, so slowly it will be integrating and actually it will give me a sorted wave kind of. And then after the at the end of this T c by 2, when this early-gate output is coming down, then the g 1 x will contain he will constant whole this value of this integrated output till the end of the chip period. So, this is a situation.

So, similarly if I look into the late-gate generator, late-gate generator is like this. Late-gate generator output actually comes for the rest half of the T c by 2. So, it is T c by 2 to T c, it is a late-gate. And if I look into that late-gate is getting multiplied this signal is getting multiplied with the signal incoming signal, band pass filter has passed it, I mean it is filtered it and fed into a integrator; integrator is integrating it for the next half of the signal. So, the integrated the output if this is my g 1 x, so g 2 x will be actually giving me an output like this and end actually both of them are coming down. So, he will come down. So, g 2 x is like this will show me the output like this.

So, this is the way the upper path and the lower path is working in the early and late-gate tracking loops circuit. So, after addition what is going on we will discuss in the next timing diagram, where this is the fundamental work that is happening into the whole circuit. Remember where from this PN sequences are getting generated. So, there is a common source of the locally generated random sequence and that is fed both through late-gate generator as well as the early-gate generator. And early-gate generator, late-gate generator: according to the trigger coming from the PN sequence generator they are generating their corresponding sequences with respect to the T c by 2 duration of the T c by 2 with the gap of the T c by 2 also from each other.

And remember what is happening, if we understand like this. So, this was the early-gate half T c by 2, this is T c by 2. So, let us start the explanation once again. Here I draw the figure like this, this was the T c, this was my T c by 2 period, this is another T c by 2 period for the late-gate. And g 1 x, so g 1 t it will be integrating like this and it will be holding good. And then you are having the next one and then we will be having the next one; and then at the end actually it will start integrating from here. And at the end it will be having the maximum peak, and the same value is a hold till the end of the T c. And for the lower one it will start at this point integrator output we will start integrating at this point because there is the start of this pulse. So, we will start at this point, it will end, you will be having a peak value or it will come down because at the end of the T c everything is coming down.

Now, at the output of this g 3 t, let us go back and visit where this g 3 t is, g 3 t is here that means, output of this g 1 and g 2 x is getting added and get fed this adder output is getting fed into the voltage controlled oscillator block. So, if I now add these two signal what I should see when they are perfectly synced with the incoming signal. So, the output of the adder will start from here like this, it will reach the peak. After that you now this is a negative voltage going up, so the adder output will come down.

And exactly in the perfect synced position it should come down to zero, because the voltage positive voltage is equivalent to the negative voltage because both of them having the partial duration of T c by 2 got the equal time to charge up and integrate. And hence actually you will get a perfect triangular wave at the output of the error. And at the end of the T c time period finally the adder output will be equal to 0 that is a situation when there is a perfect sync perfect sync condition is going on with the incoming signal.

Now, in the second picture, we are showing what will happen if the clock starts early. If the clock starts early, then see there early-gate has started early. It is division is again T c by 2. And corresponding to when he is coming down, the late-gate has also started generating, but remember the generation of the early pulse as well as the late pulse getting exhausted before the time of the chip is exhausted. And they are starting this much time earlier than the actual arrival of the incoming pulse.

And what will happen now at the output of the first integrator. First integrator is related to the early-gate. So, the integrator will not get any value, will not give you any value here, because this time the pulse as not receive this is a receive signal r t, there is no receive signals the pulse will the integrator will start working at this point. So, he will get only this much time period to integrate. So, he can never reach to the peak value that he got earlier for the full period of the T c by 2.

So, suppose I am getting T c by 4 duration to get charged. So, I will charge half of that what I got earlier for the early-gate integrator output. And the integrated output whatever is received at the end of this T c by 2 period then he will be holding this value till the end of the chip period. Similarly, what is going on for the negative pulse the negative pulse is starting from here, but even the negative pulse has got full swing even in this period of the negative pulse the full period of the time that the pulses are on. So, he will be charged up fully as per the peak value that he got earlier times when the synchronization was there. And he is holding that value till the end part of the till end part of the chip duration.

Now, funny thing is happening at the output of the adder. Now, see and slowly the timing diagram at the output of the adder. What adder has done from this period to this period adder has got a positive value, then adder has started getting the negative value. And the negative value as a peak value of the negative voltage was higher than the positive one, definitely he will cross the 0 of the zero-axis, and we will give a ending up with the negative value and he is holding that value. So, adder output you are getting negative some negative voltage here, here adder output was 0; getting adder output is 0, 0 target that the perfect synchronization situation well aligned situation. But if your clock is early to indication you will come at the output of the adder because adder will show you that you are ending up with the negative voltage.

So, what adder will tell then adder will tell the voltage control oscillator here the voltage control oscillator here to actually delay the clock because clock has started early. So, he will delay a clock little bit. Based on the level of the remaining part of the voltage, you can also calculate the amount of the delay required for the clock pulse. So, 1 d is a example when the clock started late. So, this is a situation when clock was advance, clock started early, and here is a situation when clock started late. So, let by this period. So, this is the output for the T c by 2 of the early-gate; immediately after that following that this is the output for the late-gate remember.

Now, the situation is just opposite of the 1 c. Here the positive integrator the integrator associated with the early-gate generator, he will get the full chance of getting charged up to here; and he will be holding the value up to this. What is happening with the negative value with this negative value is this negative one negative charge is starting from here and he will be here actually your charged and in the chip duration is getting ended. So, he will not get enough time to charge fully to the value of this one. So, he will be charged up to this value.

Now, at the output of the adder is interesting to see adder will see the positive voltage up to this then he will see decrement of the positive voltage by this amount by which amount by this amount. So, he will actually start decreasing by an amount, but he will be ending up as a negative voltage is less than the positive voltage here total positive peak value of the positive voltage is higher than the peak value of the negative voltage he will be ending up here. And this is the remaining positive voltage now you are getting at the output of the adder, who is saying that clock is late, you need to start little bit early.

So, you are going positive way you are going late. So, you please move left and here you are going negative means you are going early. So, you have to make yourself late. So, now seeing the situation of the value at the output of the adder the voltage control oscillator is adjusting the phase of the clock to readjust the clock's location. So, this is the way the tracking is going on in an early I mean early and late-gate based FHSS tracking.

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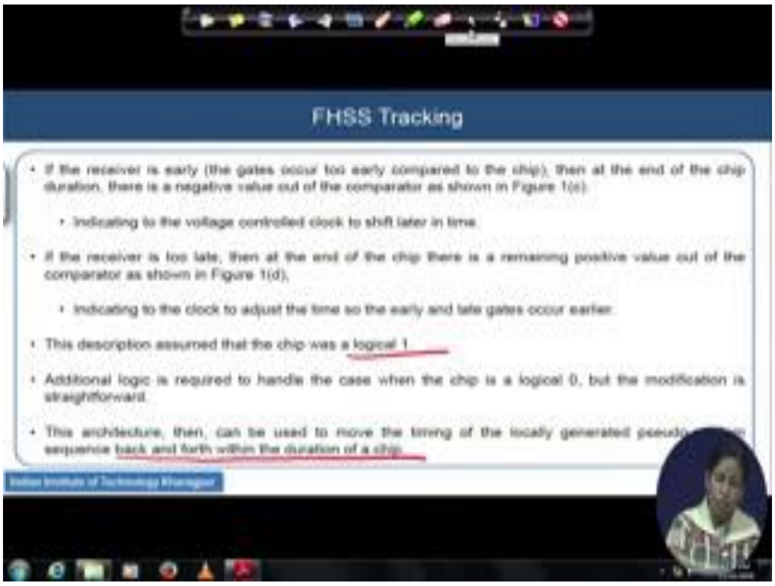

FHSS Tracking

- If the receiver is early (the gates occur too early compared to the chip), then at the end of the chip duration, there is a negative value out of the comparator as shown in Figure 1(c).
  - Indicating to the voltage controlled clock to shift later in time.
- If the receiver is too late, then at the end of the chip there is a remaining positive value out of the comparator as shown in Figure 1(d).
  - Indicating to the clock to adjust the time so the early and late gates occur earlier.
- This description assumed that the chip was a logical 1.
- Additional logic is required to handle the case when the chip is a logical 0, but the modification is straightforward.
- This architecture, then, can be used to move the timing of the locally generated pseudo sequence back and forth within the duration of a chip.

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This whole description we have done is based on the logical value one, where the chips are actually taking a plus positive voltage and they are of rectangular shape. You may need some additional logic, if you try to do the same thing with the logical values 0, but that is very trivial kind of the modification that you need to do, and the architecture almost will be same. And a locally after getting output from the adder circuit what this receiver is doing is they are making a back and forth within the duration of the chip the alignment of the code alignment of the code is getting back and forth. I mean the clock pulse is getting back and forth and hence the sequence generation that is going on that is getting adjusted inside the chip duration.

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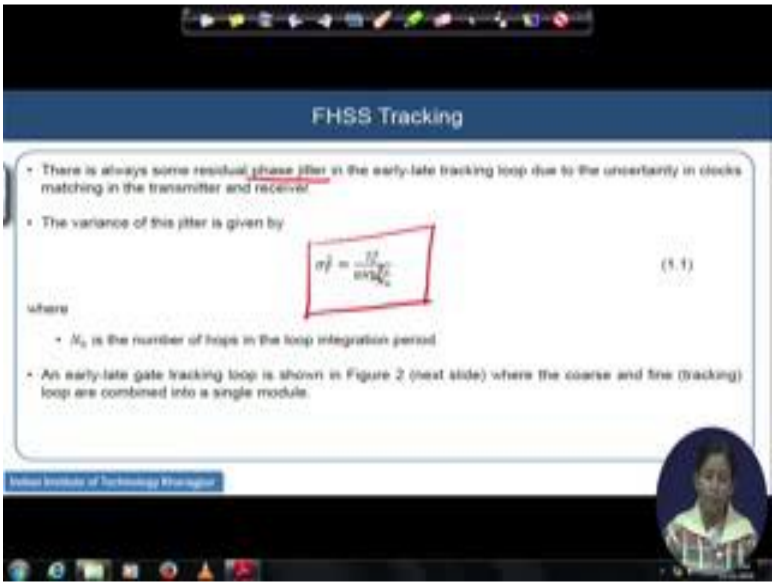

FHSS Tracking

- There is always some residual phase jitter in the early-late tracking loop due to the uncertainty in clocks matching in the transmitter and receiver
- The variance of this jitter is given by

$$\boxed{\sigma_j^2 = \frac{T_c^2}{SNR\,N_h}} \qquad (5.1)$$

where

- N_h is the number of hops in the loop integration period

- An early-late gate tracking loop is shown in Figure 2 (next slide) where the coarse and fine (tracking) loop are combined into a single module.

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But remember that even after this tracking, there may be some amount of the error, this cannot be 100 percent corrected all the time. So, the remaining residual error after the tracking we call the phase jitter, and which is basically the uncertainty in the clocks matching in the transmitter and receiver. And the variance of the jitter is given by this where your N 0 is your two-sided power spectral density of the noise and E c is the power of the chip, chip power I should say. And this T c is the duration of the chip and N h is the number of the hops in the loop integration period; and it is the function of all the three parameters T c, E c, sorry four parameter T c SNR and that N h. And this early-gate tracking loop fine and coarse tacking can be combined also in some cases you know some practical circuits, where the coarse and fine the both tracking both combined one can be actually modeled in a single module as we are seeing in this circuit.

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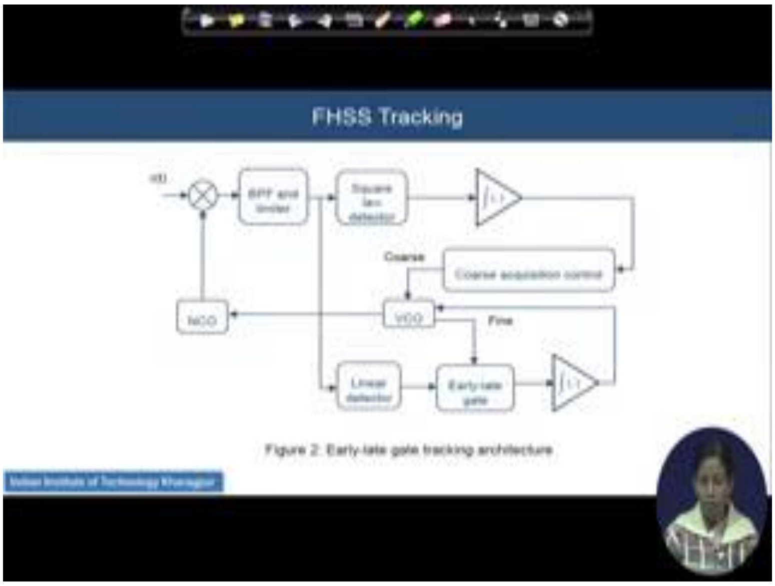

FHSS Tracking

Figure 2: Early-late gate tracking architecture

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Look for our code acquisition, what we understood as if it is some serial acquisition FHSS technique, so there is locally generate generator voltage control oscillator driving your NCO. And locally see the correlator it is a active correlator and see their search is going on. Suppose, this coarse acquisition control has acquired the coarse alignment between the receiver and locally generated one and that will be fed inside the coarse; at the same time output of the b p band pass filter and the limit can be after linear detection can enter into the early late-gate whole structure. And at output of this early late-gate one and the output of the adder also that will fed into the voltage control oscillator voltage control oscillator is finally controlling it and then in this loop actually the final tracking mechanism is going on.

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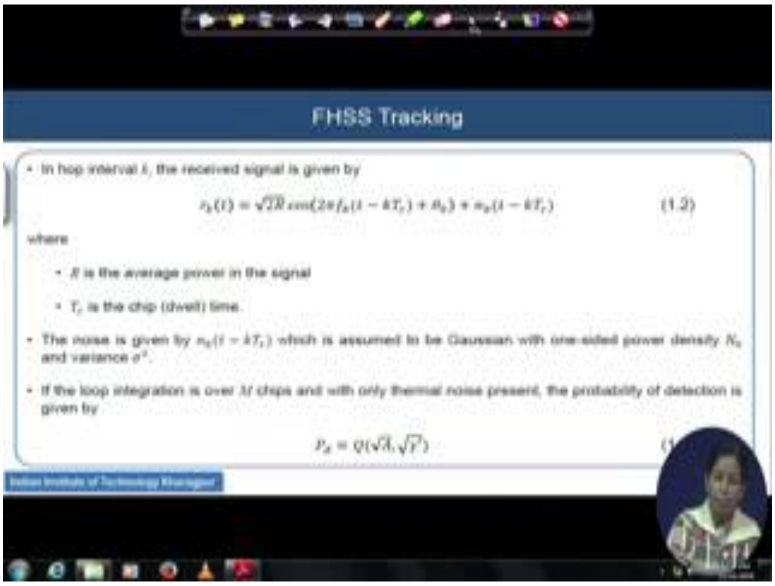

FHSS Tracking

- In hop interval k, the received signal is given by

$$r_k(t) = \sqrt{2R}\cos(2\pi f_k(t - kT_c) + \theta_k) + n_k(t - kT_c) \qquad (1.2)$$

where

  - R is the average power in the signal
  - T_c is the chip (dwell) time.

- The noise is given by $n_k(t - kT_c)$ which is assumed to be Gaussian with one-sided power density N_0 and variance σ^2.
- If the loop integration is over M chips and with only thermal noise present, the probability of detection is given by

$$P_d = Q(\sqrt{\lambda}, \sqrt{\gamma}) \qquad (1$$

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Let us look into the little bit mathematical analysis of whatever the case we have explained to a through the diagram. And the hoping interval case to receive signal now we are going to write we understand this expression we have seen several times T c is chip dwell time and capital R is a average power in the signal received. n k will be the, it is a k-th hop interval, so n k is the noise process additive white Gaussian noise process associated with this k-th interval. And remember as we had assuming that it is having a zero means, so sigma square the variance will be the power also. It has zero will be one sided power spectral density of this noise.

And if the loop integration that we are running over the capital M number of the chips with only the thermal noise present and we at the beginning we are not considering any interference of the jammer present. The detection probability we understand that it will be a function it can be approximated by a Q function where they are normalized threshold will play some role. And here actually the role will be played also by the number of the search that is a number of the tone that is getting start over the serial mechanism.

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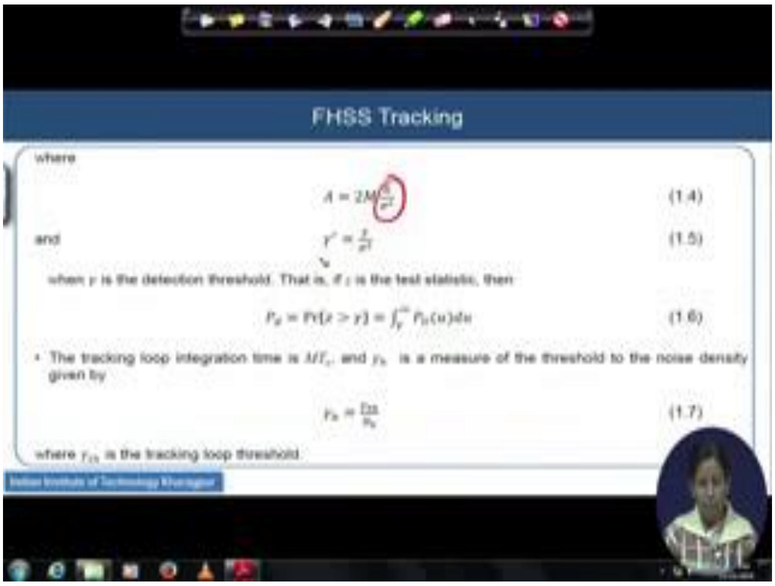

FHSS Tracking

where

$$A = 2M\frac{R}{\sigma^2} \quad (1.4)$$

and

$$\gamma' = \frac{\gamma}{\sigma^2} \quad (1.5)$$

when γ is the detection threshold. That is, if z is the test statistic, then

$$P_d = \Pr[z > \gamma] = \int_{\gamma}^{\infty} p_z(u)du \quad (1.6)$$

- The tracking loop integration time is MT_c, and γ_h is a measure of the threshold to the noise density given by

$$\gamma_h = \frac{\Gamma_{th}}{N_0} \quad (1.7)$$

where γ_{th} is the tracking loop threshold.

And remember that the number of the tones that you are getting searched over the tones that is also fundamentally not only than capital M, this is also a function of your SNR R by sigma square is going on. And this capital M is the number of the tone over which you are running the search; and gamma is our predefined threshold. So, we understood that we have normalized it with respect to the noise variance because we really wish to reduce the false alarm probability.

So, the detection probability will be there. If the probability that the test statistics is crossing the SNR value, and it will be definitely can be expressed by the case that the probability is crossing from gamma to infinity and tracking loop this integration time if I understand that chip duration is T c in then total time that over which the tracking loop is running will be capital M into T c. And gamma T h will be the measure of this threshold to the noise density, instead of gamma dashed actually our gamma h is equal to equivalent to my gamma dashed and tracking loop threshold it is.

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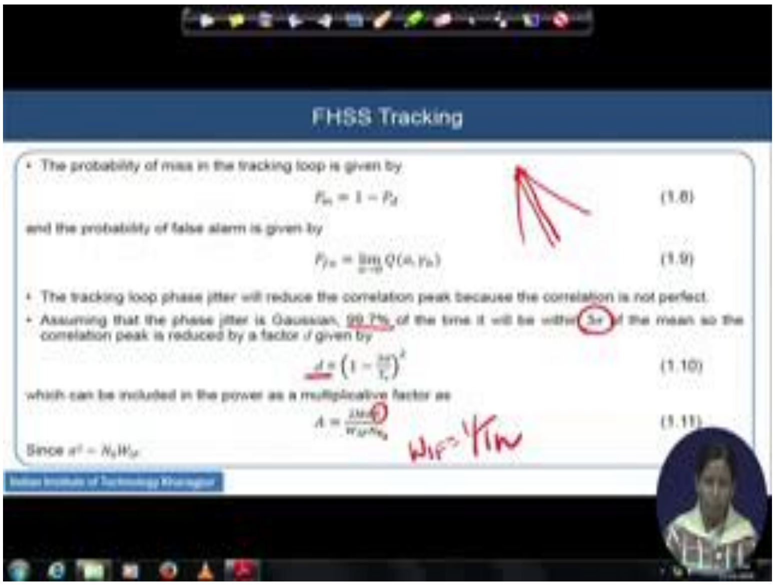

FHSS Tracking

- The probability of miss in the tracking loop is given by

$$P_m = 1 - P_d \quad (1.8)$$

and the probability of false alarm is given by

$$P_{fa} = \lim_{a \to 0} Q(a, \gamma_0) \quad (1.9)$$

- The tracking loop phase jitter will reduce the correlation peak because the correlation is not perfect.
- Assuming that the phase jitter is Gaussian, 99.7% of the time it will be within 3σ of the mean so the correlation peak is reduced by a factor d given by

$$d = \left(1 - \frac{3\sigma}{T_c}\right)^2 \quad (1.10)$$

which can be included in the power as a multiplicative factor as

$$A = \frac{2Md}{W_{IF}N_0} \quad (1.11)$$

Since $\sigma^2 = N_0 W_{IF}$

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If this is the explanation, similarly so the missed detection will be one miles the detection probability we understand; probability of false alarm will be they taking a limit of this function where a tends to the 0 value. And the tracking loop jitter, the phase jitter will reduce thus correlation peak because the correlation peak is not perfect because of this remaining offsets, you can never actually hit or never actually you can actually detect the peak you will be because of the jitter, you are close to the peak that this much amount of the residue error you will be spending ending up with.

And if we consider that the jitter will with which wherever we will be if I consider that is a random variable, and it is a can well approximated by the Gaussian and 99.7 percent of the time it will be within the three sigma of the mean. So, that the correlation peak is reduced by a factor of d, and then the d will be given by 1 minus 3 sigma by T c square. So, what we are considering here is that we are binding the jitter, we absorbed the jitter will be there the remaining offset whatever is there, fist of all it is Gaussian distributed and 99.7 percent of the time is close to just 0.3 percent of the time you are actually getting a means that one more than 99 percent of the time its values the jitter values within 3 times the sigma of the mean. So, view are within very close to each other and then this reduced in the peak from peak whatever the amount he will be used it can be measured it can be given by this formula.

And now if I understand, this is a way by this factor from the peak value the signal power will be reduced. So, I can actually multiply the R, which was actually the power of the receive signal you are not getting R, you are getting a fraction of this R now. And capital M is the times you are integrating over. And W IF we understand that W IF will be 1 by the threshold 1 by the hopping time period of the fast frequency-hopping, and here the sigma square will be coming in the expression of capital A as we have seen earlier that we have seen, but here this sigma square we have changed by a factor, we are changed by a factor there is a variance, so that total power it is a noise power also. So, we have changed it by the power spectral density of the noise multiplied by the noise bandwidth. This is equivalent to signal bandwidth also. So, A has turned to be like this.

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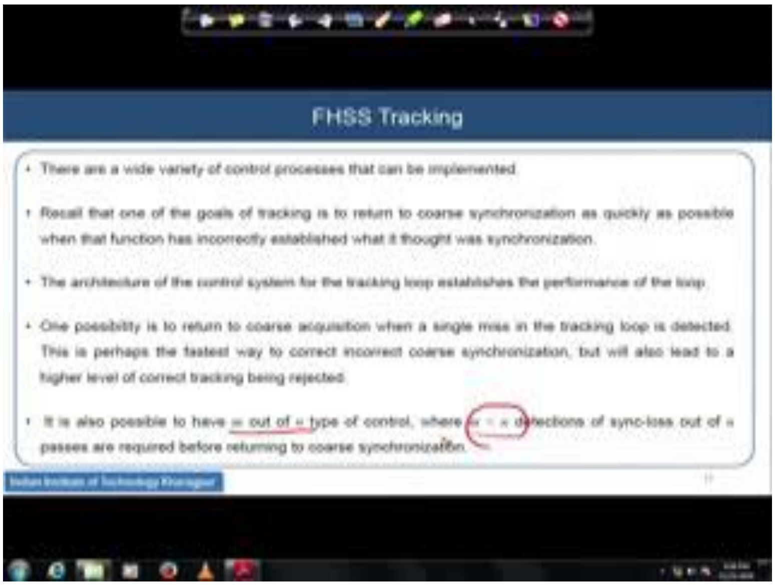

FHSS Tracking

- There are a wide variety of control processes that can be implemented.
- Recall that one of the goals of tracking is to return to coarse synchronization as quickly as possible when that function has incorrectly established what it thought was synchronization.
- The architecture of the control system for the tracking loop establishes the performance of the loop.
- One possibility is to return to coarse acquisition when a single miss in the tracking loop is detected. This is perhaps the fastest way to correct incorrect coarse synchronization, but will also lead to a higher level of correct tracking being rejected.
- It is also possible to have m out of n type of control, where $m < n$ detections of sync-loss out of n passes are required before returning to coarse synchronization.

So, they are will wide variety of the control processes is that can be implemented in this tracking. And recall that the goals of this tracking is to return to the code synchronization as quickly as possible if you find there is a gross error in the synchronization process already without entering into the tracking loop, you should go back and start the tracking mechanism code acquisition mechanism as fast as possible. And say actually, so for control for track a lot of the control stuff is involved in a tracking loop. And let us consider a situation that small m out of the capital N type of the controls to have we are having and m less than n detections of this a sync loss out of the passes and required before returning to the code synchronization. So, this is a one kind of logic that we have fixed, suppose at least n number of the directions of the sync loss we have to detect then only we will declare that there is no synchronization has been already happened in the coarse acquisition mechanism. So, we need to go back.

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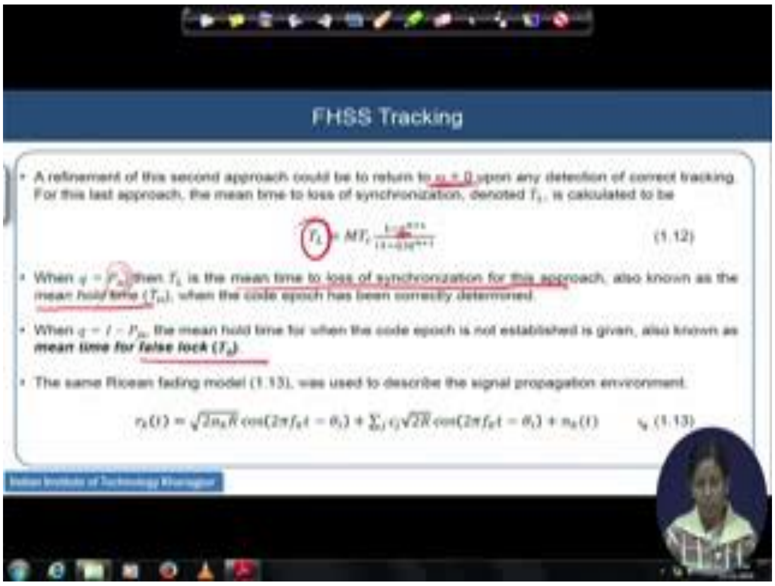

FHSS Tracking

- A refinement of this second approach could be to return to $m = 0$ upon any detection of correct tracking. For this last approach, the mean time to loss of synchronization, denoted T_L, is calculated to be

$$T_L = MT_c \frac{1-q^{N+1}}{(1-q)q^{N+1}} \qquad (1.12)$$

- When $q = P_m$ then T_L is the mean time to loss of synchronization for this approach, also known as the mean hold time (T_H), when the code epoch has been correctly determined.
- When $q = 1 - P_{fa}$ the mean hold time for when the code epoch is not established is given, also known as ***mean time for false lock*** **(T_{fl})**.
- The same Ricean fading model (1.13), was used to describe the signal propagation environment.

$$r_k(t) = \sqrt{2\alpha_k R}\cos(2\pi f_k t - \theta_i) + \textstyle\sum_j c_j\sqrt{2R}\cos(2\pi f_k t - \theta_j) + n_k(t) \qquad (1.13)$$

So, without seeing actually onetime loss sync loss, we should not go back. So, this kind of the logic is developed inside the FHSS tracking mechanism. To detect whether we should go back or to the code acquisition or not and refinement also if possible I mean how to detect actually whether m less than n whether we will go back or not. So, in that situation, what we do is where we can consider a situation when we will be setting m equal to 0 up on any detection of the correct tracking. And then for the last one, I mean for this kind of the one where actually at least one tracking mechanism we will continue and we will see try to measure what will be the typical means time to loss of the synchronization we will try to measure that quantity

Where actually this value of q, there is value of q and this measurement is given by the bigger expression. And this q, the q will be P m when actually this T L is the mean time to loss the synchronization, and also known as the mean hold time when the code epoch has been correctly determined. So, there is a loss suppose a situation is something that there is a loss sync loss and sync correct, sync loss and sync correct that is way it is going on. So, for a situation when a sync lock is there in that way in that situation, we are trying to calculate the hold time of the mean hold time for this lock. And we may put to the here actually the value of the q is equal 1 minus the probability of the false alarm which is the mean hold time for when the code epoch is not established at all I mean there is a sync loss.

So, the mean time for the falls lock also the code acquisition I mean the code tracking circuit can measure and quickly feed us a give us feedback. So, whether the hold means by the synchronization is hold for the meantime for holding the synchronization and the meantime for giving the false lock both can be quantified; and based on that study also you can decide whether we shall go back for the code acquisition or not. The same Ricean fading model if I consider and the signal propagation environment that we have considered earlier also given in 1.13 if I go ahead.

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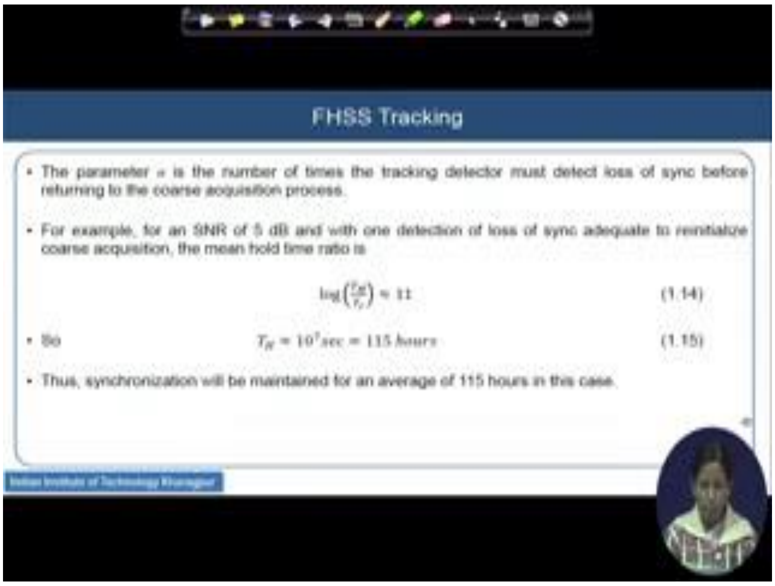

FHSS Tracking

- The parameter n is the number of times the tracking detector must detect loss of sync before returning to the coarse acquisition process.
- For example, for an SNR of 5 dB and with one detection of loss of sync adequate to reinitialize coarse acquisition, the mean hold time ratio is

$$\log\left(\frac{T_H}{T_c}\right) \approx 11 \qquad (1.14)$$

- So $$T_H = 10^7 sec = 115\, hours \qquad (1.15)$$
- Thus, synchronization will be maintained for an average of 115 hours in this case.

Then you are then actually we will see that the parameter in the last expression that n q to the power n this is a number of the times that tracking detector is running basically. And on that environment that we have already taken over the Ricean channel over the Ricean channel, if I take an example suppose it is actually found and also the experiment it is found that for an SNR of say 5 dB with one detection of the loss of the sync adequate to reinitialize the coarse acquisition. The mean holed time approximately will be is found to be around log value of the mean hold time to the correspond to the T c time ratio of this can be a proximity of 11, and which are leads as that the hold time will be 115 hours. So, if we can show actually some value for SNR of 5 dB, if we can keep a value of a round close to 11, so for 115 hours it is guaranteed that the synchronization will be hold good.

So, fundamentally this is the ratio of with respect to the chip duration, what will be the how much time actually the hold time is possible to keep, and you need not to go back to the coarse acquisition, once acquisition and tracking both are done. And based on the several situation because we have considered it is the Ricean environment, but we have not considered that the Doppler effect happening inside. We have not considered the interfere are profile of the interference how it is changing over the network. We have not considered the adder contained receiver in impairments that are coming into picture.

And any other change in the velocity of the transmitter as well as receiver whether they are happening or not in such change of the Doppler frequency. If everything is perfect then once you are getting it, and this is the expression that we are giving us and we are can get at SNR of 5 dB with only under the noise acting on it; for 115 hours, you can keep the holding time of the synchronized situation. But this is highly actually idealistic situation in practice, we never get this much amount of the time for.