Spread Spectrum Communications and Jamming
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Lecture - 36
Rapid Acquisition Using Matched Filter - Part II

Hello students. In continuation of our last class in the last module, what we were discussing about the matched filter architecture to expedite the acquisition time for a synchronize design inside the direct sequence specific type communication receiver. Today we will see little bit more and try to get the final expression what exactly is the final acquisition time and we will quantify that with respect to the non matched filter based technique, how much we could gain in terms of acquisition time in the matched filter design and how to implement this matched filter architecture also in practice.

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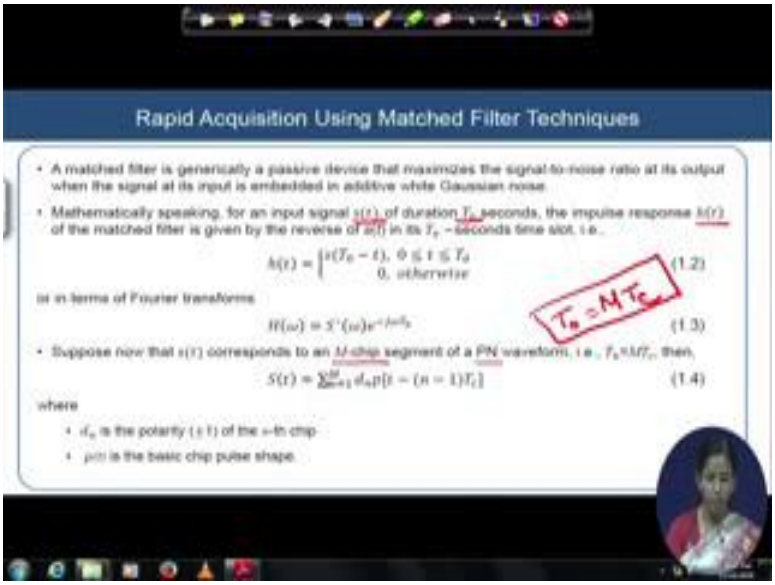

Let us revisit to the matched filter architecture once again. A matched filter is generally a passive device, who maximizes the output signal to noise ratio when the signal is present at the input and embedded with WGN noise; additive white Gaussian noise and we understand that if we are having a signal s t and which is having a period of t 0 seconds. We will, if it is having a t 0 seconds then the impulse response of the filter should be given by s T 0 minus t which is a reverse of S t.

We have discussed this in the last module and if this is the impulse response of the filter its key valiant transfer function will be obtained by taking the Fourier transform of this equation 1.2 and we will be ending up with equation 1.3 where, the deviation the delay in the time delay in the equation 1.2 will be reflected as the phase offset and we also discussed that the kind of the signal.

Now, we are dealing with in the point of our context. We have thought that suppose we are dealing with a capital M chip segment of a PN waveform and such that actually within this t 0, we are having capital M number of the chips which are having T c duration and. So, t 0 is equal to M into T c in our case and d n. So, the signal will be written like this equation 1.4 where, the d n is nothing, but the polarity of each and every chip and it can take a value of plus or minus 1. It is the basic reform of the chip and n minus 1 into T c this is the delay that each and every chip is associated with respect to the first chip.

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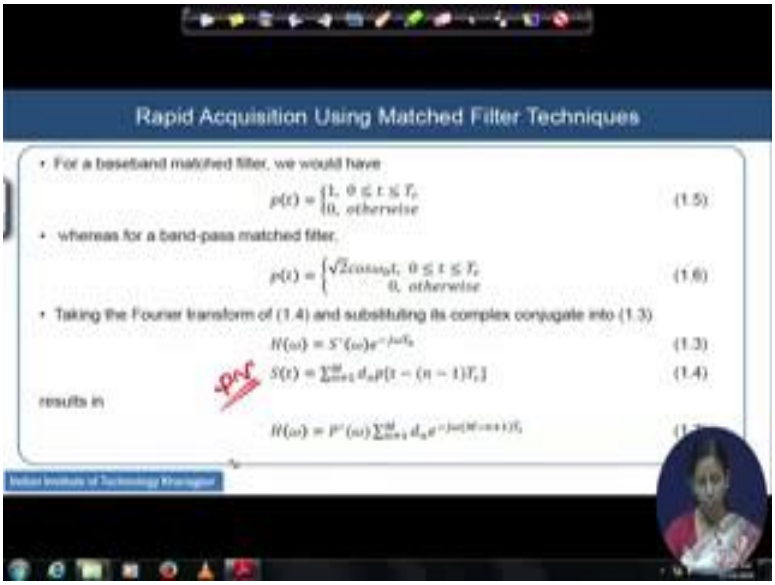

And next we try to see that the kind of the matched filter, it we will have if it is a in the baseband or if it is in the pass band. In the case of the baseband the p t should be designed in such a way that p t will be equal to 1 for baseband matched filter over the duration of our interest and it will be 0 otherwise; if it is a band pass. Actually it should be square multiplied with square root of 2 cos omega naught t over the duration of our interest and it is a chip duration basically.

And we also took the Fourier transform, we saw in the last module that if this is a point of our if it is a signal, of our interest this is a PN sequence that is we are interested in and if I take the Fourier transform of this sequence, how we can and if we substitute it inside the equation 1.3? How we get the transfer function of the filter now?

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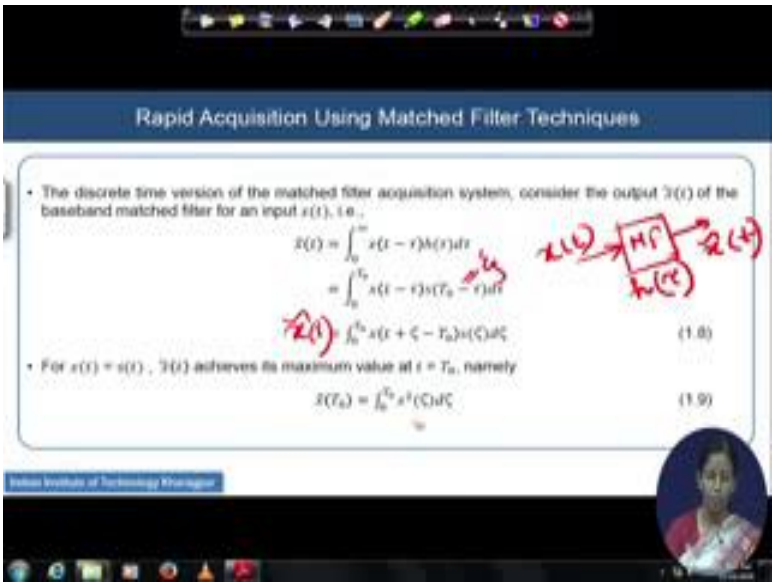

It was done in the last class. So, after this recap let us proceed, we are interested to get the discreet time version of this matched filter acquisition system because we wish to actually put them in the, put the circuit inside the discreet time domain for easy handling. And let us consider the fact that, we are having a matched filter where the output is whether input is given as x t and we are getting at the output of this matched filter a signal which is called x tilde t say. So, from the fundamentals of the matched filter we understand that x tilde t, will be giving by x t minus tau multiplied by h tau d tau, if h tau is the impulse response of the matched filter.

Now we are not interested really over the whole interval intervention interval from 0 to infinite time because our signal is having a duration of T 0. So, we will be integrating it from 0 to T 0 and. So, x t minus tau and this h tau we understand that it is matched with the signal x T 0 minus tau from the equation number 1, 1.1. And by substituting that and we get here and if I now do the further substitution of tau 0, T 0 minus tau this is equal to psi. We will be ending up with the equation 1.8.

So, now what is, this is saying that this is the output finally at the output of the matched filter the signal that is coming out. Now if I try to see that what will happen this output, when this output will be maximized because we understand that matched filter output can give us a maximum signal to noise ratio value, given certain condition. It will give actually the maximum value, if this x t exactly matches with my s psi and if I consider that actually at t is equal to T 0, they are exactly matching then it will be simply S square psi substituting small t equal to T 0.

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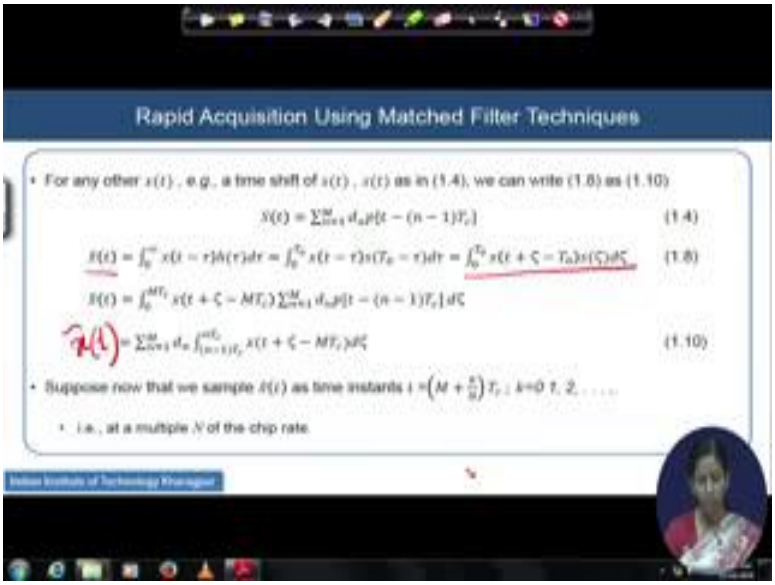

You will be getting exactly S square psi. So, output at T 0 will be given by the expression 1.9 following the matched filter fundamentals. Now, if that is a situation if they both of them exactly matched with each other, what if they are not? So, the there is the time shift of this s t suppose such a way that in our case we are having, we are coming we are dealing with capital M number of the chips. Each and every chips from the second on wards where, all the chips are having some times shifted option they are coming in a shifted version, time shifted version given by a fixed time interval given by the T c.

And so in such a situation the equation the earlier equation of x tilde t which ended here, now actually look like how, look like what? It will look like this instead of our s psi, now there is no chance that it will get at t equal to T 0. You will suddenly get S square psi rather this s psi will be now replaced by his expression. Whereas, actually a this d n, if I can bring out in the summation and d n I have brought out actually its changing the

summation and integration operation and over one chip duration I mean n minus 1 T c to M T c the value of the p will be either 1 or minus 1 and this will be ending up with actually x t plus psi minus M into T c.

Remember, here actually instead of T 0, we are substituted the value of capital M into T c and the integration is that is why an interval 0 to capital M into T c. And this integration once actually we are bringing inside. So, as a sum, as addition is there output as outside; so is this integration is sufficient to run over one chip interval. Now this is the output of the matched filter in our case of interest. If I, now sample the output of this matched filter at an instant which is capital M plus small K by N. So, 1 by N was the chip rate. So, at a multiple of some chip rate I am sampling it. So, if this is the situation into T c is the; obviously, there because T c is the duration after which the samples are expected to come and this K value can be 0, 1, 2, 3, 4 like that. So, if K is increasing. So, keep on increasing K.

That means I am increasing the sampling instant at a multiple of the chip rate, if this is the situation then, where I will end up?

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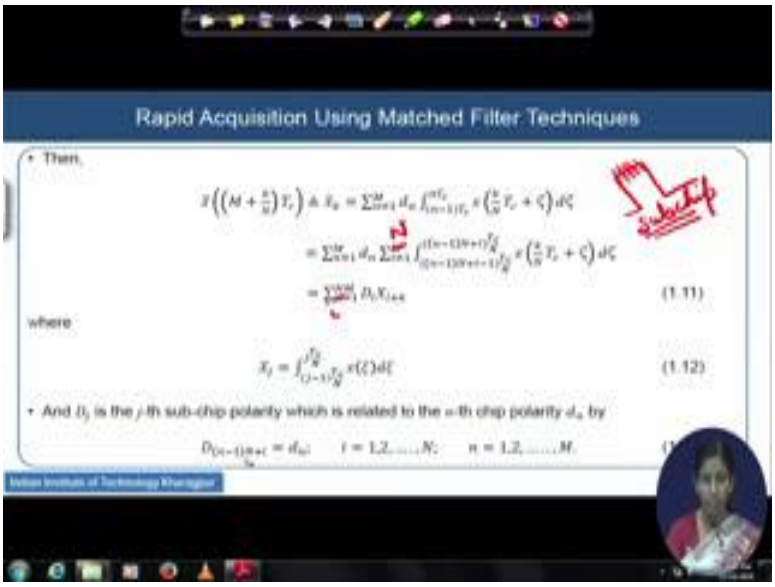

I will now substitute the x tilde t, this small t I will substitute by M plus K by N into T c. Everywhere that is the only part done here and this will excite x delta M plus K by N into T c can be now approximately called as x tilde K and this is the simple substitution that

we have done there and plus N T c minus N T c is gone. Now consider a situation that within a chip duration when the acquisition is going on actually we are not within a chip duration we will be really talking about half chip duration one-fourth chip duration. So, there is, as if there is a concept of sub chip levels.

We are talking in the acquisition having during synchronization; we talk about the sub chip levels. To introduce the concept of this sub chip level remember here we have introduced another quantity of i another variable i. Say i is also having from varying from 1 to capital N. So, within the I had capital N number of the chips and within that I have actually say, capital inside that I am having the capital N number of the sub chips. You make it you make it capital N.

So, I have capital N number of the sub chips and. So, what is happening? Now this integration is now is not only over the chip duration. So, this integration if I keep the summation once again outside over the all sub chips then, this inner integration now can run over a sub chip level, sub chip duration. And hence actually this whole equation which is coming inside if I can substitute it by X i plus k where, the X j is given by this line. So, this equation we are ending up with that the output, the sampled output of the matched filter will be governed by this.

Remember this D is nothing, but the summation of M plus 1 d n all that and double summation is coming up for the i also and what the i actually, if I consider this n is moving from 1 to M and the sub chip is running from i to capital N. So, if I now transfer everything in terms of the sub chips. So, totally sub chips are running your searching is running over the duration of capital N into capital M sub chip time period. So, your n is moving from basically 1 to capital N into M and it is not n it is your i, i is moving from 1 to capital N into capital M. And your D i into X i plus k is the final expression you are ending up with. And remember the relation between D j the jth sub chip polarity with the nth chip polarity d n.

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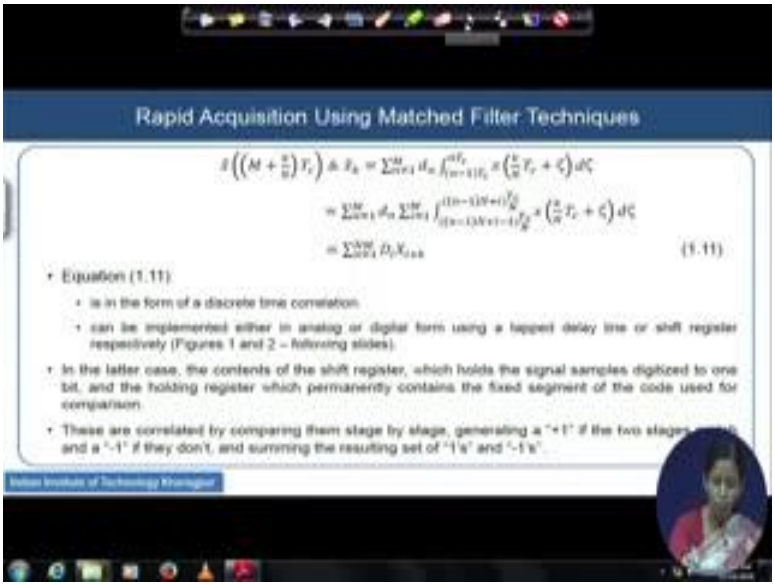

So, there is a sub chip polarity and there is nth chip polarity right. So, the relation will be given by this and. So, we ended here in the last slide what does it mean? This will not be n this will be i remember please remember. So, what does it mean? It means that first of all this look at this architecture, this architecture has already brought us down in the sub chip level and this is the discreet time correlation going on. And it can be implemented either in the analog domain or in the digital domain and either through the tab dealer line architecture or by the shift register architecture that we will discuss immediately next.

And if I do it in the shift register architecture there is a shift register who is holding actually the replica of the replica of a PN segment permanently and it is a fixed segment over which actually the over which is a continuously getting compared with the running segment of the incoming PN sequences. And they are correlated and in this shift it is a sequence are correlated with each other.

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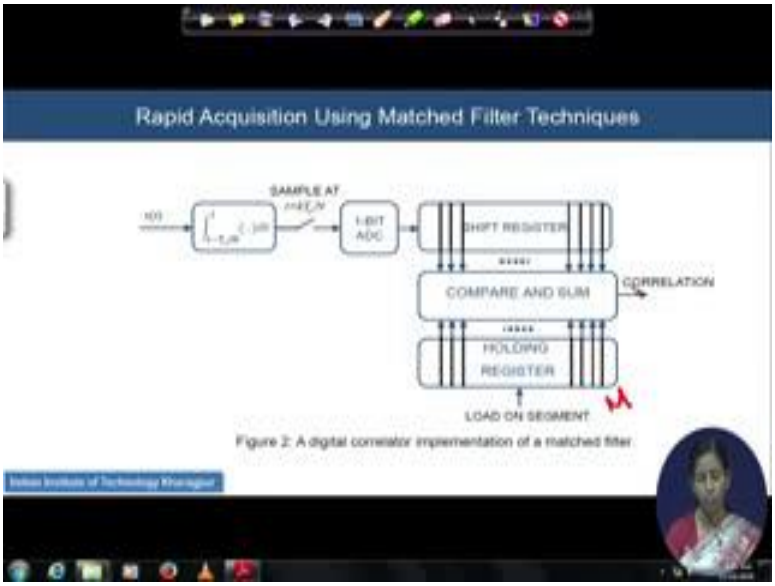

Let us go to the next slide and then discuss. And this is a analog correlator implementation of the matched filter where, actually this matched filter architecture was expressed by the tab dealer lines that we have shown in the last module and the D js are fed here as the code weights. We have seen that the d 1 to d capital Ms are there and there instead of capital M, you are we will having capital N into capital M number of the weights and capital N into capital M number of the weights as well as the tabs inside it and we will be doing the changing the values of them. And after summation of that the correlation output will be coming up. So, that was the structure of the matched filter there and it is sampling at K T c by N.

We are more interested in this shift register architecture which is a digital implementation of the matched filter where we are having two register; one is the holding register another is the shift register. Inside this holding register we first load a segment of the PN chip segment well say actually they are having the capital M number of the chips. And the incoming signals are sampled by an one bit ADC at the rate of K T c by N like the analog architecture. And here part symbol you are getting 1 bit and inside the shift register whenever a new bit is entering the last bit is going out.

And this shift register all the bits stored in the shift register, they are getting compared inside this comparator block one by one and in this it is a corresponding comparison going on. And if both of them are 1, then you are generating a plus 1. When they are not

matching they are generating a minus 1 and at the M you are adding actually over all those number of the chips, all those number of the chips here and finally, the output is found here.

Remember one thing actually T actually we are not satisfied under things are not going across a threshold, is holding register value we are not going to change.

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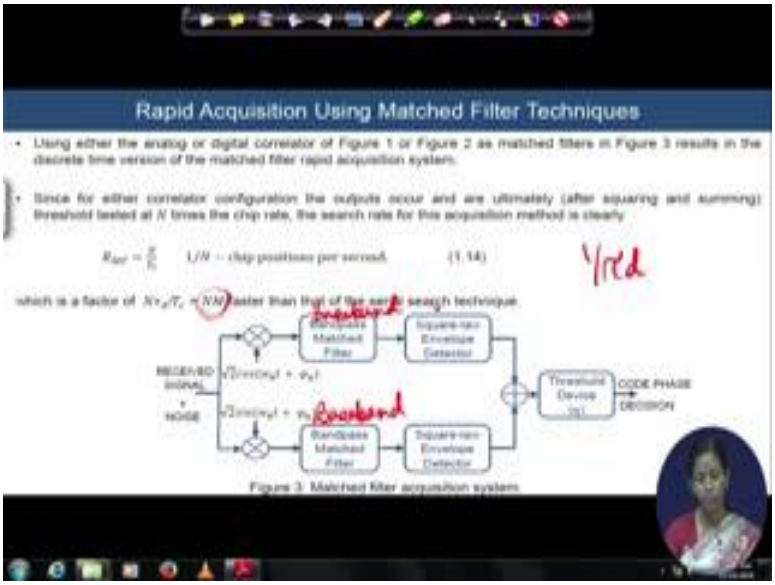

And remember this structure of this digital or analog correlated that we have seen in the last two figures, that will be actually they were will work as a matched filter and that is matched filter will be placed now inside this blocks. And this matched filter they are truly Bandpass filter if it is as I told you if it is IF, otherwise they will be base band matched filter. If you are dealing with the base band frequencies and now the fundamental question is to be answered now.

This, whether you are in the analog or you are in the digital correlator architecture, any one of them you look into the thing is happening like this. For either correlated configuration the output you are getting and are ultimately threshold testing is going on at capital N times the chip rate going on. Because the chip rate and that is why actually the rate at which the acquisition is possible, the rate at which you are taking the decision that is the N times the chip rate and because you have done the sampling in that fashion and that is why actually all the processing is going on at the one capital N by T c rate.

And now actually the total acquisition rate with the matched filter is now given by N by capital T c of 1 by N chip position per second. Now this N by capital T c an earlier we got it is 1 by tau d in the normal case. So, now, what is the improvement in the factor? Improvement is a factor will be N into capital N into tau divide T c with respect to this, if I compare these two I am gaining at a gap of capital N into tau d divide by T c and.

If this is a situation then fundamentally this tau d by T c is given by capital M. So, your capital N into M times faster becoming compared to the serial search techniques that earlier you are integration multiplier and integrated dump circuit based acquisition systems where giving you. So, there is a gain that a matched filter based acquisition can give you. That is why the name says justify that it is a rapid acquisition mechanism and this architecture also capable to give you a very rapid acquisition mechanism by replacing the multiplier and followed by an integration and changing actually the search mechanisms at the sub chip levels matched filter is expediting your acquisition time.

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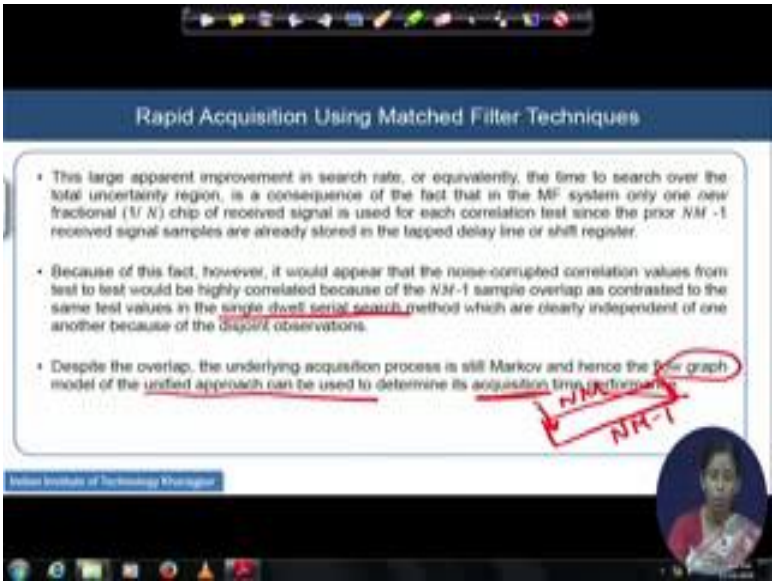

So, it may seem actually to anybody that we are searching at a rate of 1 by capital N chip intervals and at each and every moment what is happening; whenever a new bit is entering into the shift register it is not shifting all the bits, remaining bits of the shift (Refer Time: 19:16) there are something was there already stored in the shift register. You are every time you are entering a new bit only one single bit only.

So, if it is a N into capital M number of the chip, some shift register you have seen on the top. In the shift register based architecture there is a storage capacity of capital N into capital num M number of the sub chips and that you what you are having instead inside that every single bit is getting changed for every instant.

For with every clock walls, but remaining capital N into M minus 1 chips are remaining as it is like the earlier circle. Only one chip at every moment is entering as a new chip inside the shift register. So, it may happen than it may actually one can argue on the fact that, the noise corrupted correlation correlated values which were there for capital N into M minus 1 samples they will be now getting highly correlated over the time duration because they are not changing every time only one bit is changing. So, you that part is not changing with respect to the single dwell serial search technique. Where every time you are getting a completely new set of the incoming signal as well as the new set of the PN sequences. So, there is no situation of carrying over the cross relation, noise corrupted correlated value samples over the next time zone.

We understand there is a overlap, but in spite of this overlap the under living acquisition process of the matched filter actually it follows the mark of distilled you can show that it is a mark of model and it follows the mark of model and hence it the flow graph of this model of this unified approach, we can be used to determine the acquisition time and acquisition time performance nicely. So, it does not valid actually the fundamental mark of chain model and. So, we can actually still utilize this matched filter and that already promised gain in terms of that rapid acquisition can be obtained.

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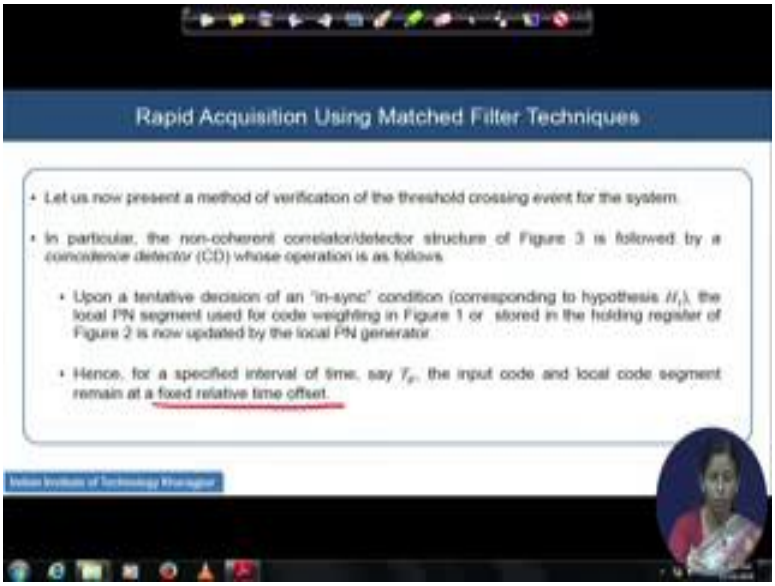

Now let us actually put some comment on the verification mechanism that is kind of matched filter architecture, takes place because we have just done the filtering correlation operation and. So, how is it going on and at the output how the decision is now going on. Inside the threshold detector let us see little bit. We have seen that in the architecture of the figure 3; let us go back. In this architecture of the figure 3, after the addition we are having a threshold device eta, we are actually the eta is the threshold point over which actually there is verification algorithm is running inside the threshold device. Actually inside that structure this detector architecture correlated detector architecture is follow.

It is it followed by another detector which is called a coincidence detector. This coincide the task of this coincidence detector is to declare whether you are in the in sync condition or not. Upon, a tentative decision that you are in sync condition corresponding say the hypothesis H 1. H 1 says that you are in sync, the local PN segment which was loaded inside this holding register with i n coming back here. So, whatever you are storing in segment inside the holding register or actually the equivalently inside the figure 1, whatever you are storing in the code weighting that will be now updated.

So, once the synchronization is done. So, then it will be updated and it will be for a specific interval of the time say equal to T p, it will be continuously holding that segment of the PN generator and the input code will be continuously getting correlated with this relative set of the PN segment selected where the declaration was there, that there is a in

sync. And hence actually for that time interval we understand that input is. So, continuously maintaining a fixed relative time offset with respect to the incoming with respect to the hold signal on hold inside the holding shift register.

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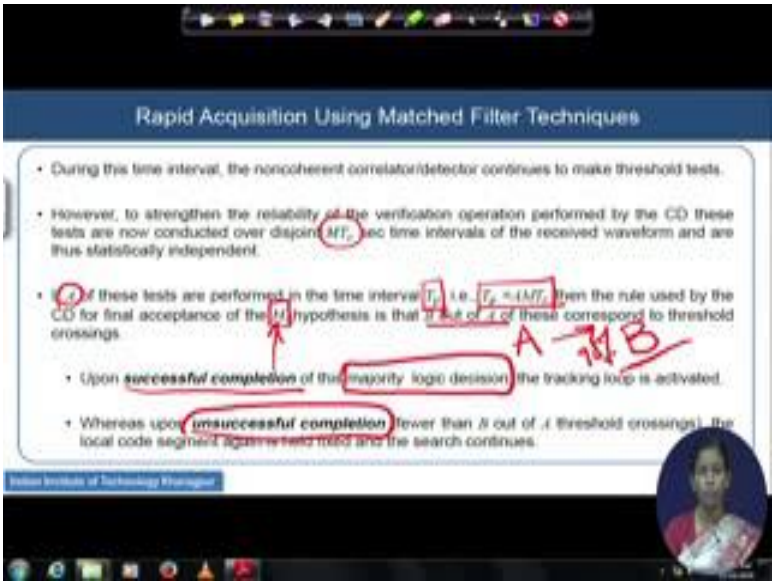

And during this time interval, the non coherent correlator detector it continuous to make the threshold tests; if such multiple threshold tests are going on then, we may have actually aiming to T c number of the second time intervals, we are going on over this multiple tests. Remember for all this M into T c intervals where, the tests are independent and individually will be statistically independent, if we are running it actually over this multiple disjoint time intervals. And how actually this CD is working? CD is working hence this way. Suppose out of this A of this tests that we are performing over the time interval T p, if I am doing a type of, a times the tests are running over the time interval T p. So, T p is basically nothing, but in times of T c multiplied by A times you are running the test.

So, A into M into T c will be the time given by the observation interval. Then the rule that is used inside the CD to finally acceptance for final acceptance of the H 1 hypothesis that, there is a heat is that the B out of A of this corresponds to threshold crossings. So, then the CD will declare that there is a heat; the algorithm will say that I have run the test capital A times. Out of that capital A times, capital B times I have got the heat. I have (Refer Time: 25:47) I have seen that the correlated output has crossed the threshold level

eta. So, logic is a priori set that you run on a capital A number of test and you find that the how many times it is crossing the threshold? If you see that for the capital B number of the times it is successfully crossing. So, then successful completion you can declare and hence you declare that there is a heat.

So, that is a majority it is, this logic is called the majority logic decision. So, for majority of the times which is declared here or if we define here as the number capital B, for majority of the times we have found that the output has crossed the threshold inside the CD and then CD has declared that it is a logically it is a successful completion of the getting the heat so, most of the cases synchronization will happen.

An unsuccessful completion; that means, fewer than B times you are seeing that there is a decision output is crossing; the correlated output is crossing the threshold. The local code segment we need to be again is held fixed and the search technique starts once again. So, that is an unsuccessful completion that, if we find that less than the time it is going on. So, we will be actually changing the segment or we actually we will keep on it holding and for new segment we will try to continuously check on. So, checking is and how the checking is going on actually how the decision is leading to change the PN segment there is a one guideline actually for you and CD is one critical example where, actually the majority logic decision based decision is getting declared for the synchronization heat.

But it may be also some other logic for example, you may be very straight about thinking that out of the A tests if all the cases the there, if there is a not a heat I mean the level is not getting crossed by the threshold level is not getting crossed, but the correlated output then we would not be declaring that logic is also possible. Another point is how will you select this capital B? It depends actually how many times, how many percentage of the time you are asking actually out of this capital A.

To expecting the correlated output to cross the position, cross the threshold and you will be declaring sometimes it will be a 90 percent of the cases of the capital A that we are thinking that it is a heat. Sometimes it may this percentage may vary actually from 80 to 99 say any value you feel that it is fixed for your typical synchronize and design and your kind of the system design, how crucial it is to be synchronized with the incoming signal? That also reflects actually how good you are system performance is in terms of the bit

error rate if your synchronization is not properly obtained.

Hence a code would not be properly aligned and the dispreading process will be heavily hampered and output of the dispread signal will be not properly correct and hence you would not be able to get a good bit error rate at the output of the detected output. And once actually that is the measure that will you can feed back from the output of the detector, final demodulation and detection of the bits you can actually bring the decision back, feed it back to readjust the level of this capital B inside the synchronizer, inside the CD that. So, that actually the performance can be further improved.

Your target is to finally, get very nice bit error rate and so with the very minimal amount of the error in the decoded bits. That is the final target of any system design. So, you in keep on improving, but remember one thing, more stringent you are in this decision in their verification logic more time you will be elapsing in the in taking the decision and more time you are taking the decision actually it may happen that it is not liable for the kind of application for which you are designing the system.

So, there is a tie there is a compromise and there is a crucial decision you have to take as a system engineer that how good synchronizer should be? And how much time I am having in my hand? So, how strict I should be in the taking the decision and. So, that I can how much time I should elapse? And how what is the error level of final error level of the detected bits i am actually happy with?

So, it is the level of the quality of service in terms of the bit error rate that is fixed, that is predefined from the customer point and from a design point. That will lead back to select the value of the capital B inside your precision device.